



# 3 V to 5 V Single Supply, 200 kSPS 12-Bit Sampling ADC

## AD7854/AD7854L\*

### FEATURES

Specified for  $V_{DD}$  of 3 V to 5.5 V

Read-Only Operation

AD7854—200 kSPS; AD7854L—100 kSPS

System and Self-Calibration with Autocalibration on Power-Up

Low Power

AD7854: 15 mW ( $V_{DD} = 3$  V)

AD7854L: 5.5 mW ( $V_{DD} = 3$  V)

Automatic Power-Down After Conversion (25  $\mu$ W)

Flexible Parallel interface

12-Bit Parallel / 8-Bit Parallel (AD7854)

28-Pin DIP, SOIC and SSOP Packages (AD7854)

### APPLICATIONS

Battery-Powered Systems (Personal Digital Assistants,

Medical Instruments, Mobile Communications)

Pen Computers

Instrumentation and Control Systems

High Speed Modems

### GENERAL DESCRIPTION

The AD7854/AD7854L is a high speed, low-power, 12-bit ADC which operates from a single 3 V or 5 V power supply, the AD7854 being optimized for speed and the AD7854L for low power. The ADC powers up with a set of default conditions at which time it can be operated as a read-only ADC. The ADC contains self-calibration and system calibration options to ensure accurate operation over time and temperature and has a number of power-down options for low power applications.

The AD7854 is capable of 200 kHz throughput rate while the AD7854L is capable of 100 kHz throughput rate. The input track-and-hold acquires a signal in 500 ns and features a pseudo-differential sampling scheme. The AD7854 and AD7854L input voltage range is 0 to  $V_{REF}$  (unipolar) and  $-V_{REF}/2$  to  $+V_{REF}/2$ , centered at  $V_{REF}/2$  (bipolar). The coding is straight binary in unipolar mode and twos complement in bipolar mode. Input signal range is to the supply and the part is capable of converting full-power signals to 100 kHz.

CMOS construction ensures low power dissipation of typically 5.4 mW for normal operation and 3.6  $\mu$ W in power-down mode. The part is available in 28-pin, 0.3 inch wide dual-in-line package (DIP), 28-lead small outline (SOIC) and 28-lead small shrink outline (SSOP) packages.

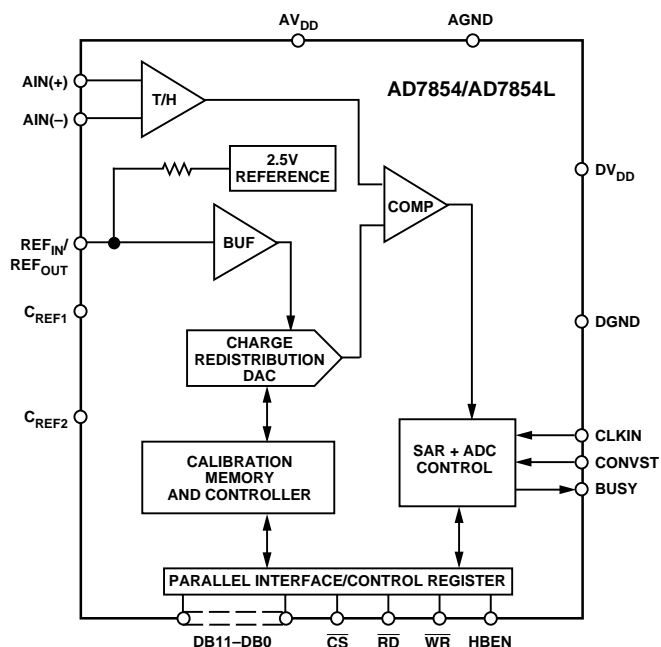
\*Patent pending.

See Page 35 for data sheet index.

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### FUNCTIONAL BLOCK DIAGRAM



### PRODUCT HIGHLIGHTS

1. Operation with either 3 V or 5 V power supplies.
2. Automatic calibration on power-up.
3. Flexible power management options including automatic power-down after conversion.
4. Operates with reference voltages from 1.2 V to  $A_{VDD}$ .
5. Analog input ranges from 0 V to  $A_{VDD}$ .
6. Self- and system-calibration.
7. Versatile parallel I/O port.
8. Lower power version AD7854L.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.  
Tel: 617/329-4700 Fax: 617/326-8703

# AD7854/AD7854L—SPECIFICATIONS<sup>1, 2</sup>

( $AV_{DD} = DV_{DD} = +3.0\text{ V to }+5.5\text{ V}$ ,  $REF_{IN}/REF_{OUT} = 2.5\text{ V}$

External Reference,  $f_{CLKIN} = 4\text{ MHz}$  (1.8 MHz for L Version);  $f_{SAMPLE} = 200\text{ kHz}$  (AD7854), 100 kHz (AD7854L); SLEEP = Logic High;  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.) Specifications in ( ) apply to the AD7854L.

Parameter	A Version <sup>1</sup>	B Version <sup>1</sup>	S Version <sup>1</sup>	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Signal to Noise + Distortion Ratio <sup>3</sup> (SNR)	70	71	70	dB min	Typically SNR is 72 dB V <sub>IN</sub> = 10 kHz Sine Wave, f <sub>SAMPLE</sub> = 200 kHz (100 kHz)
Total Harmonic Distortion (THD)	-78	-80	-78	dB max	V <sub>IN</sub> = 10 kHz Sine Wave, f <sub>SAMPLE</sub> = 200 kHz (100 kHz)
Peak Harmonic or Spurious Noise	-78	-80	-78	dB max	V <sub>IN</sub> = 10 kHz Sine Wave, f <sub>SAMPLE</sub> = 200 kHz (100 kHz)
Intermodulation Distortion (IMD) Second Order Terms	-78	-80	-78	dB typ	f <sub>a</sub> = 9.983 kHz, f <sub>b</sub> = 10.05 kHz, f <sub>SAMPLE</sub> = 200 kHz (100 kHz)
Third Order Terms	-78	-80	-78	dB typ	f <sub>a</sub> = 9.983 kHz, f <sub>b</sub> = 10.05 kHz, f <sub>SAMPLE</sub> = 200 kHz (100 kHz)
DC ACCURACY					
Resolution	12	12	12	Bits	5 V Reference V <sub>DD</sub> = 5 V Guaranteed No Missed Codes to 12 Bits
Integral Nonlinearity	±1	±1	±1	LSB max	
	±1	±0.5	±1	LSB max	
Differential Nonlinearity	±1	±0.5	±1	LSB max	
Total Unadjusted Error	±1	±1	±1	LSB typ	
Unipolar Offset Error	±1	±0.5	±1	LSB max	
Positive Full-Scale Error	±2	±1	±1	LSB max	
Negative Full-Scale Error	±2	±1	±1	LSB max	
Bipolar Zero Error	±1	±0.5	±1	LSB max	
ANALOG INPUT					
Input Voltage Ranges	0 to V <sub>REF</sub>	0 to V <sub>REF</sub>	0 to V <sub>REF</sub>	Volts	i.e., AIN(+) – AIN(–) = 0 to V <sub>REF</sub> , AIN(–) can be biased up but AIN(+) cannot go below AIN(–). i.e., AIN(+) – AIN(–) = –V <sub>REF</sub> /2 to +V <sub>REF</sub> /2, AIN(–) should be biased to +V <sub>REF</sub> /2 and AIN(+) can go below AIN(–) but cannot go below 0 V.
	±V <sub>REF</sub> /2	±V <sub>REF</sub> /2	±V <sub>REF</sub> /2	Volts	
Leakage Current	±1	±1	±1	µA max	
Input Capacitance	20	20	20	pF typ	
REFERENCE INPUT/OUTPUT					
REF <sub>IN</sub> Input Voltage Range	2.3/V <sub>DD</sub>	2.3/V <sub>DD</sub>	2.3/V <sub>DD</sub>	V min/max	Functional from 1.2 V
Input Impedance	150	150	150	kΩ typ	
REF <sub>OUT</sub> Output Voltage	2.3/2.7	2.3/2.7	2.3/2.7	V min/max	
REF <sub>OUT</sub> Tempco	20	20	20	ppm/°C typ	
LOGIC INPUTS					
Input High Voltage, V <sub>INH</sub>	2.4	2.4	2.4	V min	AV <sub>DD</sub> = DV <sub>DD</sub> = 4.5 V to 5.5 V AV <sub>DD</sub> = DV <sub>DD</sub> = 3.0 V to 3.6 V
	2.1	2.1	2.1	V min	
Input Low Voltage, V <sub>INL</sub>	0.8	0.8	0.8	V max	AV <sub>DD</sub> = DV <sub>DD</sub> = 4.5 V to 5.5 V AV <sub>DD</sub> = DV <sub>DD</sub> = 3.0 V to 3.6 V
	0.6	0.6	0.6	V max	
Input Current, I <sub>IN</sub>	±10	±10	±10	µA max	Typically 10 nA, V <sub>IN</sub> = 0 V or V <sub>DD</sub>
Input Capacitance, C <sub>IN</sub> <sup>4</sup>	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V <sub>OH</sub>	4	4	4	V min	I <sub>SOURCE</sub> = 200 µA AV <sub>DD</sub> = DV <sub>DD</sub> = 4.5 V to 5.5 V AV <sub>DD</sub> = DV <sub>DD</sub> = 3.0 V to 3.6 V
	2.4	2.4	2.4	V min	
Output Low Voltage, V <sub>OL</sub>	0.4	0.4	0.4	V max	I <sub>SINK</sub> = 1.6 mA
Floating-State Leakage Current	±10	±10	±10	µA max	
Floating-State Output Capacitance <sup>4</sup>	10	10	10	pF max	Unipolar Input Range Bipolar Input Range
Output Coding	Straight (Natural) Binary				
	Twos Complement				
CONVERSION RATE					
Conversion Time	4.5 (9)	4.5 (9)	4.5 (9)	µs max	(L Versions Only)
Track/Hold Acquisition Time	0.5 (1)	0.5 (1)	0.5 (1)	µs min	(L Versions Only)

Parameter	A Version <sup>1</sup>	B Version <sup>1</sup>	S Version <sup>1</sup>	Units	Test Conditions/Comments
<b>POWER REQUIREMENTS</b>					
AV <sub>DD</sub> , DV <sub>DD</sub>	+3.0/+5.5	+3.0/+5.5	+3.0/+5.5	V min/max	
I <sub>DD</sub>					
Normal Mode <sup>5</sup>	5.5 (1.8)	5.5 (1.8)	5.5 (1.8)	mA max	AV <sub>DD</sub> = DV <sub>DD</sub> = 4.5 V to 5.5 V. Typically 4.5 mA (1.5mA);
	5.5 (1.8)	5.5 (1.8)	5.5 (1.8)	mA max	AV <sub>DD</sub> = DV <sub>DD</sub> = 3.0 V to 3.6 V. Typically 4.0 mA (1.5 mA).
Sleep Mode <sup>6</sup>					
With External Clock On	10	10	10	μA typ	Full power down. Power management bits in control register set as PMGT1 = 1, PMGT0 = 0.
	400	400	400	μA typ	Partial power down. Power management bits in control register set as PMGT1 = 1, PMGT0 = 1.
With External Clock Off	5	5	5	μA max	Typically 1 μA. Full power down. Power management bits in control register set as PMGT1 = 1, PMGT0 = 0.
	200	200	200	μA typ	Partial Power Down. Power management bits in control register set as PMGT1 = 1, PMGT0 = 1.
Normal Mode Power Dissipation	30 (10) 20 (6.5)	30 (10) 20 (6.5)	30 (10) 20 (6.5)	mW max mW max	V <sub>DD</sub> = 5.5 V: Typically 25 mW (8); $\overline{\text{SLEEP}}$ = V <sub>DD</sub> V <sub>DD</sub> = 3.6 V: Typically 15 mW (5.4); $\overline{\text{SLEEP}}$ = V <sub>DD</sub>
Sleep Mode Power Dissipation					
With External Clock On	55 36	55 36	55 36	μW typ μW typ	V <sub>DD</sub> = 5.5 V; $\overline{\text{SLEEP}}$ = 0 V V <sub>DD</sub> = 3.6 V; $\overline{\text{SLEEP}}$ = 0 V
With External Clock Off	27.5	27.5	27.5	μW max	V <sub>DD</sub> = 5.5 V: Typically 5.5 μW; $\overline{\text{SLEEP}}$ = 0 V
	18	18	18	μW max	V <sub>DD</sub> = 3.6 V: Typically 3.6 μW; $\overline{\text{SLEEP}}$ = 0 V
<b>SYSTEM CALIBRATION</b>					
Offset Calibration Span <sup>7</sup>	$+0.05 \times V_{\text{REF}}/-0.05 \times V_{\text{REF}}$			V max/min	Allowable Offset Voltage Span for Calibration
Gain Calibration Span <sup>7</sup>	$+0.025 \times V_{\text{REF}}/-0.025 \times V_{\text{REF}}$			V max/min	Allowable Full-Scale Voltage Span for Calibration

## NOTES

<sup>1</sup>Temperature ranges as follows: A, B Versions, -40°C to +85°C, S Version, -55°C to +125°C.

<sup>2</sup>Specifications apply after calibration.

<sup>3</sup>SNR calculation includes distortion and noise components.

<sup>4</sup>Sample tested @ +25°C to ensure compliance.

<sup>5</sup>All digital inputs @ DGND except for CONVST,  $\overline{\text{SLEEP}}$ , CAL, and SYNC @ DV<sub>DD</sub>. No load on the digital outputs. Analog inputs @ AGND.

<sup>6</sup>CLKIN @ DGND when external clock off. All digital inputs @ DGND except for CONVST,  $\overline{\text{SLEEP}}$ , CAL, and SYNC @ DV<sub>DD</sub>. No load on the digital outputs. Analog inputs @ AGND.

<sup>7</sup>The offset and gain calibration spans are defined as the range of offset and gain errors that the AD7853/AD7853L can calibrate. Note also that these are voltage spans and are not absolute voltages (i.e., the allowable system offset voltage presented at AIN(+) for the system offset error to be adjusted out will be AIN(-)  $\pm 0.05 \times V_{\text{REF}}$ , and the allowable system full-scale voltage applied between AIN(+) and AIN(-) for the system full-scale voltage error to be adjusted out will be  $V_{\text{REF}} \pm 0.025 \times V_{\text{REF}}$  (unipolar mode) and  $V_{\text{REF}}/2 \pm 0.025 \times V_{\text{REF}}$  (bipolar mode)). This is explained in more detail in the calibration section of the data sheet.

Specifications subject to change without notice.

# AD7854/AD7854L

## TIMING SPECIFICATIONS<sup>1</sup> ( $AV_{DD} = DV_{DD} = +3.0\text{ V to }+5.5\text{ V}$ ; $f_{CLKIN} = 4\text{ MHz}$ for AD7854 and $1.8\text{ MHz}$ for AD7854L; $T_A = T_{MIN}$ to $T_{MAX}$ , unless otherwise noted)

Parameter	Limit at $T_{MIN}$ , $T_{MAX}$ (A, B, S Versions)		Units	Description
	5 V	3 V		
$f_{CLKIN}$ <sup>2</sup>	500 4	500 4	kHz min MHz max	Master Clock Frequency
$t_1$ <sup>3</sup>	1.8	1.8	MHz max	L Version
$t_2$	100	100	ns min	$\overline{CONVST}$ Pulse Width
$t_{CONVERT}$	50	50	ns max	$\overline{CONVST}$ to $BUSY \uparrow$ Propagation Delay
	4.5	4.5	$\mu s$ max	Conversion Time = $18 t_{CLKIN}$
	10	10	$\mu s$ max	L Version 1.8 MHz $CLKIN$ . Conversion Time = $18 t_{CLKIN}$
$t_3$	15	15	ns min	$HBEN$ to $\overline{RD}$ Setup Time
$t_4$	5	5	ns min	$HBEN$ to $\overline{RD}$ Hold Time
$t_5$	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
$t_6$	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
$t_7$	100	100	ns min	$\overline{RD}$ Pulse Width
$t_8$ <sup>4</sup>	50	50	ns max	Data Access Time after $\overline{RD}$
$t_9$ <sup>5</sup>	5	5	ns min	Bus Relinquish Time after $\overline{RD}$
	50	50	ns max	
$t_{10}$	100	100	ns min	Minimum Time Between Reads
$t_{11}$	15	15	ns min	$HBEN$ to $\overline{WR}$ Setup Time
$t_{12}$	5	5	ns max	$HBEN$ to $\overline{WR}$ Hold Time
$t_{13}$	15	15	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
$t_{14}$	5	5	ns max	$\overline{CS}$ to $\overline{WR}$ Hold Time
$t_{15}$	100	100	ns min	$\overline{WR}$ Pulse Width
$t_{16}$	40	40	ns min	Data Setup Time Before $\overline{WR}$
$t_{17}$	5	5	ns min	Data Hold Time After $\overline{WR}$
$t_{18}$ <sup>4</sup>	40	40	ns min	New Data Valid Before Falling Edge of $BUSY$
$t_{19}$	60	60	ns min	$HBEN$ Low Pulse Duration
$t_{20}$	60	60	ns min	$HBEN$ High Pulse Duration
$t_{21}$	60	60	ns min	Propagation Delay from $HBEN$ Falling to Data Valid
$t_{22}$	60	60	ns min	Propagation Delay from $HBEN$ Rising to Data Valid
$t_{23}$	$2.5 t_{CLKIN}$	$2.5 t_{CLKIN}$	ns max	$CS \uparrow$ to $BUSY \uparrow$ in Calibration Sequence
$t_{CAL}$ <sup>6</sup>	31.25	31.25	ms typ	Full Self-Calibration Time, Master Clock Dependent ( $125013 t_{CLKIN}$ )
$t_{CAL1}$ <sup>6</sup>	27.78	27.78	ms typ	Internal DAC Plus System Full-Scale Cal Time, Master Clock Dependent ( $111114 t_{CLKIN}$ )
$t_{CAL2}$ <sup>6</sup>	3.47	3.47	ms typ	System Offset Calibration Time, Master Clock Dependent ( $13899 t_{CLKIN}$ )

### NOTES

<sup>1</sup>Sample tested at +25°C to ensure compliance. All input signals are specified with  $t_r = t_f = 5\text{ ns}$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of 1.6 V. See Table TBD and timing diagrams for different interface modes and calibration.

<sup>2</sup>Mark/Space ratio for the master clock input is 40/60 to 60/40.

<sup>3</sup>The  $\overline{CONVST}$  pulse width here only applies for normal operation. When the part is in power-down mode, a different  $\overline{CONVST}$  pulse width applies (see Power-Down section).

<sup>4</sup>Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.4 V.

<sup>5</sup> $t_9$  is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time,  $t_9$ , quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

<sup>6</sup>The typical time specified for the calibration times is for a master clock of 4 MHz. For the L version the calibration times will be longer than those quoted here due to the 1.8 MHz master clock.

Specifications subject to change without notice.

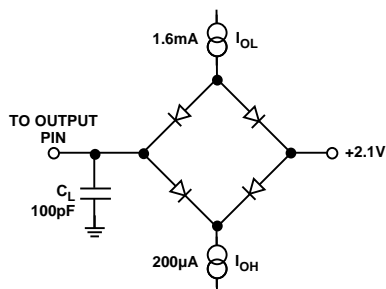


Figure 1. Load Circuit for Digital Output Timing Specifications

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = +25°C unless otherwise noted)

AV <sub>DD</sub> to AGND	−0.3 V to +7 V
DV <sub>DD</sub> to DGND	−0.3 V to +7 V
AV <sub>DD</sub> to DV <sub>DD</sub>	−0.3 V to +0.3 V
Analog Input Voltage to AGND	−0.3 V to AV <sub>DD</sub> + 0.3 V
Digital Input Voltage to DGND	−0.3 V to DV <sub>DD</sub> + 0.3 V
Digital Output Voltage to DGND	−0.3 V to DV <sub>DD</sub> + 0.3 V
REF <sub>IN</sub> /REF <sub>OUT</sub> to AGND	−0.3 V to AV <sub>DD</sub> + 0.3 V
Input Current to Any Pin Except Supplies <sup>2</sup>	±10 mA
Operating Temperature Range	
Commercial (A, B Versions)	−40°C to +85°C
Commercial (S Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
Plastic DIP Package, Power Dissipation	450 mW
θ <sub>JA</sub> Thermal Impedance	75°C/W
θ <sub>JC</sub> Thermal Impedance	25°C/W
Lead Temperature, (Soldering, 10 secs)	+260°C
SOIC, SSOP Package, Power Dissipation	450 mW
θ <sub>JA</sub> Thermal Impedance	75°C/W (SOIC) 115°C/W (SSOP)
θ <sub>JC</sub> Thermal Impedance	25°C/W (SOIC) 35°C/W (SSOP)
Lead Temperature, Soldering	
Vapor Phase (60 secs)	+215°C
Infrared (15 secs)	+220°C
ESD	>? kV

## NOTES

<sup>1</sup>Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<sup>2</sup>Transient currents of up to 100 mA will not cause SCR latchup.

## ORDERING GUIDE

Model	Linearity Error (LSB) <sup>1</sup>	Power Dissipation (mW)	Package Option <sup>2</sup>
AD7854AQ	±1	20	N-24
AD7854SQ	±1/2	20	N-24
AD7854AR	±1	20	R-24
AD7853BR	±1/2	20	R-24
AD7854ARS	±1	6.85	RS-24
AD7854LAR <sup>3</sup>	±1	6.85	R-24
AD7854LARS <sup>3</sup>	±1	6.85	RS-24
EVAL-AD7854CB <sup>4</sup>			
EVAL-CONTROL BOARD <sup>5</sup>			

## NOTES

<sup>1</sup>Linearity error refers to the integral linearity error.

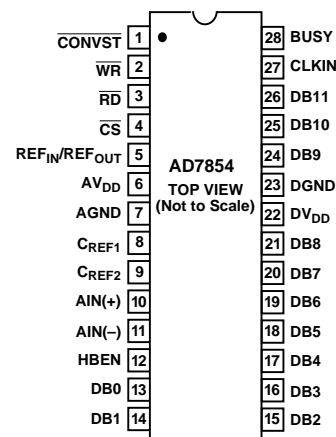
<sup>2</sup>N = Plastic DIP; R = SOIC; RS = SSOP.

<sup>3</sup>L signifies the low power version.

<sup>4</sup>This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.

<sup>5</sup>This board is a complete unit allowing a PC to control and communicate with all Analog Devices, Inc. evaluation boards ending in the CB designator.

## PINOUT FOR DIP, SOIC AND SSOP



# AD7854/AD7854L

## TERMINOLOGY

### Integral Nonlinearity

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

### Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

### Total Unadjusted Error

This is the deviation of the actual code from the ideal code taking all errors into account (*Gain, Offset, Integral Nonlinearity, and other errors*) at any point along the transfer function.

### Unipolar Offset Error

This is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal AIN(+) voltage (AIN(−) + 1/2 LSB) when operating in the unipolar mode.

### Positive Full-Scale Error

This applies to the unipolar and bipolar modes and is the deviation of the last code transition from the ideal AIN(+) voltage after the offset error has been adjusted out. For unipolar mode, the ideal AIN(+) voltage is (AIN(−) +  $V_{REF}$  − 1.5 LSB). For bipolar mode, the ideal AIN(+) voltage is (AIN(−) +  $V_{REF}/2$  − 1.5 LSB).

### Negative Full-Scale Error

This applies to the bipolar mode only and is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal AIN(+) voltage (AIN(−) −  $V_{REF}/2$  + 0.5 LSB).

### Bipolar Zero Error

This is the deviation of the midscale transition (all 0s to all 1s) from the ideal AIN(+) voltage (AIN(−) − 1/2 LSB).

### Track/Hold Acquisition Time

The track/hold amplifier returns into track mode and the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

### Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ( $f_s/2$ ), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\text{Signal to (Noise + Distortion)} = (6.02 N + 1.76) \text{ dB}$$

Thus for a 12-bit converter, this is 74 dB.

### Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7853/AD7853L, it is defined as:

$$\text{THD (dB)} = 20 \log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}$$

where  $V_1$  is the rms amplitude of the fundamental and  $V_2$ ,  $V_3$ ,  $V_4$ ,  $V_5$  and  $V_6$  are the rms amplitudes of the second through the sixth harmonics.

### Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to  $f_s/2$  and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

### Intermodulation Distortion

With inputs consisting of sine waves at two frequencies,  $f_a$  and  $f_b$ , any active device with nonlinearities will create distortion products at sum and difference frequencies of  $m f_a \pm n f_b$  where  $m, n = 0, 1, 2, 3$ , etc. Intermodulation distortion terms are those for which neither  $m$  nor  $n$  are equal to zero. For example, the second order terms include  $(f_a + f_b)$  and  $(f_a - f_b)$ , while the third order terms include  $(2f_a + f_b)$ ,  $(2f_a - f_b)$ ,  $(f_a + 2f_b)$  and  $(f_a - 2f_b)$ .

Testing is performed using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

## PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	$\overline{\text{CONVST}}$	Convert Start. Logic input. A low to high transition on this input puts the track/hold into its hold mode and starts conversion. When this input is not used, it should be tied to $\text{DV}_{\text{DD}}$ .
2	$\overline{\text{RD}}$	Read Input. Active low logic input. Used in conjunction with $\overline{\text{CS}}$ and HBEN to read from internal registers.
3	$\overline{\text{WR}}$	Write Input. Active low logic input. Used in conjunction with $\overline{\text{CS}}$ and HBEN to write to internal registers.
4	$\overline{\text{CS}}$	Chip Select Input. Active low logic input. The device is selected when this input is active.
5	$\text{REF}_{\text{IN}}/\text{REF}_{\text{OUT}}$	Reference Input/Output. This pin is connected to the internal reference through a series resistor and is the reference source for the analog-to-digital converter. The nominal reference voltage is 2.5 V and this appears at the pin. This pin can be overdriven by an external reference and can be taken as high as $\text{AV}_{\text{DD}}$ . When this pin is tied to $\text{AV}_{\text{DD}}$ , then the $\text{C}_{\text{REF1}}$ pin should also be tied to $\text{AV}_{\text{DD}}$ .
6	$\text{AV}_{\text{DD}}$	Analog Positive Supply Voltage, +3.0 V to +5.5 V.
7	AGND	Analog Ground. Ground reference for track/hold, reference and DAC.
8	$\text{C}_{\text{REF1}}$	Reference Capacitor (0.1 $\mu\text{F}$ multilayer ceramic). This external capacitor is used as a charge source for the internal DAC. The capacitor should be tied between the pin and AGND.
9	$\text{C}_{\text{REF2}}$	Reference Capacitor (0.01 $\mu\text{F}$ ceramic disc). This external capacitor is used in conjunction with the on-chip reference. The capacitor should be tied between the pin and AGND.
10	$\text{AIN}(+)$	Analog Input. Positive input of the pseudo-differential analog input. Cannot go below AGND or above $\text{AV}_{\text{DD}}$ at any time, and cannot go below $\text{AIN}(-)$ when the unipolar input range is selected.
11	$\text{AIN}(-)$	Analog Input. Negative input of the pseudo-differential analog input. Cannot go below AGND or above $\text{AV}_{\text{DD}}$ at any time.
12	HBEN	High Byte Enable Input. The AD7854 operates in byte mode only but outputs 12 bits of data during a read cycle with HBEN low. When HBEN is high then the high byte of data that is written to or read from the part is on DB0 to DB7. When HBEN is low then the lowest byte of data being written to the part is on DB0 to DB7. If reading from the part with HBEN low then the lowest 12 bits of data appear on pins DB0 to DB11. This allows a single read from the ADC or from the control register in a 16-bit bus system. However, two reads are needed to access the calibration registers. Also, two writes are necessary to write to any of the registers.
13–21	DB0–DB8	Data Bits 0 to 8. Three state data I/O pins that are controlled by $\overline{\text{CS}}$ , $\overline{\text{RD}}$ , $\overline{\text{WR}}$ and HBEN. Data output is straight binary (unipolar mode) or twos complement (bipolar mode).
22	$\text{DV}_{\text{DD}}$	Digital Supply Voltage, +3.0 V to +5.5 V.
23	DGND	Digital Ground. Ground reference point for digital circuitry.
24–26	DB9–DB11	Data Bits 9 to 11. Three state data I/O pins that are controlled by $\overline{\text{CS}}$ , $\overline{\text{RD}}$ , $\overline{\text{WR}}$ and HBEN. Data output is straight binary (unipolar mode) or twos complement (bipolar mode).
27	CLKIN	Master Clock Signal for the device (4 MHz for AD7854, 1.8 MHz for AD7854L). Sets the conversion and calibration times.
28	BUSY	Busy Output. The busy output is triggered high by the falling edge of $\overline{\text{CONVST}}$ and remains high until conversion is completed. BUSY is also used to indicate when the AD7854/AD7854L has completed its on-chip calibration sequence.



# AD7854/AD7854L

## AD7854/AD7854L ON-CHIP REGISTERS

The AD7854/AD7854L powers up with a set of default conditions, and the user need not ever write to the device. In this case the AD7854/AD7854L will operate as a read-only ADC. The  $\overline{WR}$  pin should be tied to  $DV_{DD}$  for operating the AD7854/AD7854L as a read-only ADC.

Extra features and flexibility such as performing different power-down options, different types of calibrations including system calibration, and software conversion start can be selected by writing to the part.

The AD7854/AD7854L contains a **control register**, **ADC output data register**, **status register**, **test register** and **10 calibration registers**. The control register is write-only, the ADC output data register and the status register are read-only, and the test and calibration registers are both read/write registers. The test register is used for testing the part and should not be written to.

### Addressing the On-Chip Registers

#### Writing

To write to the AD7854/AD7854L, a 16-bit word of data must be transferred. This transfer consists of two 8-bit writes. The first 8 bits of data that are written *must* consist of the 8 LSBs of the 16-bit word and the second 8 bits that are written *must* consist of the 8 MSBs of the 16-bit word. For each of these 8-bit writes, the data is placed on Pins DB0 to DB7, Pin DB0 being the LSB of each transfer and Pin DB7 being the MSB of each transfer. The two MSBs of the 16-bit word, ADDR1 and ADDR0, are decoded to determine which register is addressed, and the 14 LSBs are written to the addressed register. Table I shows the decoding of the address bits, while Figure 2 shows the overall write register hierarchy.

**Table I. Write Register Addressing**

ADDR1	ADDR0	Comment
0	0	This combination does not address any register.
0	1	This combination addresses the <b>TEST REGISTER</b> . The 14 LSBs of data are written to the test register.
1	0	This combination addresses the <b>CALIBRATION REGISTER</b> . The 14 least significant data bits are written to the selected calibration register.
1	1	This combination addresses the <b>CONTROL REGISTER</b> . The 14 least significant data bits are written to the control register.

#### Reading

To read from the various registers the user must first write to Bits 6 and 7 in the Control Register, RDSLT0 and RDSLT1. These bits are decoded to determine which register is addressed during a read operation. Table II shows the decoding of the read address bits while Figure 3 shows the overall read register hierarchy. The power-up status of these bits is 00 so that the default read will be from the ADC output data register.

Once the read selection bits are set in the control register all subsequent read operations that follow are from the selected register until the read selection bits are changed in the control register.

**Table II. Read Register Addressing**

RDSLT1	RDSLT0	Comment
0	0	All successive read operations are from the <b>ADC OUTPUT DATA REGISTER</b> . This is the default power-up setting. There is always four leading zeros when reading from the ADC output data register.
0	1	All successive read operations are from the <b>TEST REGISTER</b> .
1	0	All successive read operations are from the <b>CALIBRATION REGISTERS</b> .
1	1	All successive read operations are from the <b>STATUS REGISTER</b> .

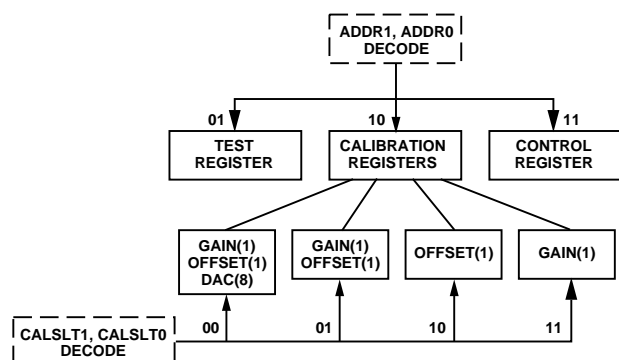


Figure 2. Write Register Hierarchy/Address Decoding

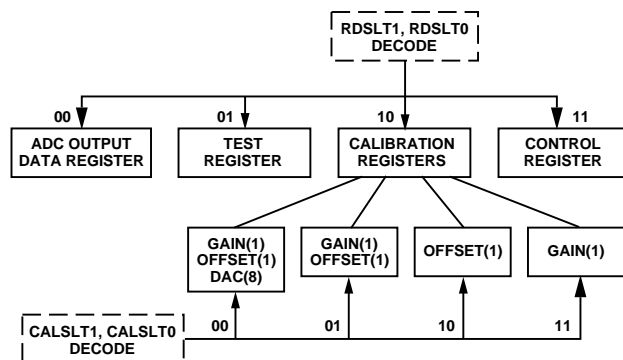


Figure 3. Read Register Hierarchy/Address Decoding



**CONTROL REGISTER**

The arrangement of the control register is shown below. The control register is a write only register and contains 14 bits of data. The control register is selected by putting two 1s in ADDR1 and ADDR0. The function of the bits in the control register is described below. The power-up status of all bits is 0.

**MSB**

ZERO	ZERO	ZERO	ZERO	PMGT1	PMGT0	RDSLT1
------	------	------	------	-------	-------	--------

RDSLT0	AMODE	CONVST	CALMD	CALSLT1	CALSLT0	STCAL
--------	-------	--------	-------	---------	---------	-------

**LSB****Control Register Bit Function Description**

Bit	Mnemonic	Comment
13	ZERO	These four bits must be set to 0 when writing to the control register.
12	ZERO	
11	ZERO	
10	ZERO	
9	PMGT1	Power Management Bits. These two bits are used with the $\overline{\text{SLEEP}}$ pin for putting the part into various power-down modes (See <i>Power-Down</i> section for more details).
8	PMGT0	
7	RDSLT1	These two bits determine which register is addressed for the read operations. See Table II.
6	RDSLT0	
5	AMODE	Analog Mode Bit. This pin allows two different analog input ranges to be selected. A logic 0 in this bit position selects range 0 to $V_{\text{REF}}$ (i.e., $\text{AIN}(+) - \text{AIN}(-) = 0$ to $V_{\text{REF}}$ ). In this range $\text{AIN}(+)$ cannot go below $\text{AIN}(-)$ and $\text{AIN}(-)$ cannot go below AGND and data coding is straight binary. A logic 1 in this bit position selects range $-V_{\text{REF}}/2$ to $+V_{\text{REF}}/2$ (i.e., $\text{AIN}(+) - \text{AIN}(-) = -V_{\text{REF}}/2$ to $+V_{\text{REF}}/2$ ). $\text{AIN}(+)$ cannot go below AGND, so for this range, $\text{AIN}(-)$ needs to be biased to at least $+V_{\text{REF}}/2$ to allow $\text{AIN}(+)$ to go as low as $\text{AIN}(-) - V_{\text{REF}}/2$ V. Data coding is two's complement for this range.
4	CONVST	Conversion Start Bit. A logic one in this bit position starts a single conversion, and this bit is automatically reset to 0 at the end of conversion. This bit may also be used in conjunction with system calibration (see Calibration section).
3	CALMD	Calibration Mode Bit. A 0 here selects self-calibration and a 1 selects a system calibration (see Table III).
2	CALSLT1	Calibration Selection Bits and Start Calibration Bit. These bits have two functions. With the STCAL bit set to 1, the CALSLT1 and CALSLT0 bits determine the type of calibration performed by the part (see Table III). The STCAL bit is automatically reset to 0 at the end of calibration. With the STCAL bit set to 0, the CALSLT1 and CALSLT0 bits are decoded to address the calibration register for read/write of calibration coefficients (see section on the calibration registers for more details).
1	CALSLT0	
0	STCAL	

**Table III. Calibration Selection**

CALMD	CALSLT1	CALSLT0	Calibration Type
0	0	0	A <b>full internal calibration</b> is initiated. First the internal DAC is calibrated, then the internal gain error and finally the internal offset error are removed. This is the default setting.
0	0	1	First the <b>internal gain error</b> is removed, then the <b>internal offset error</b> is removed.
0	1	0	The <b>internal offset error</b> only is calibrated out.
0	1	1	The <b>internal gain error</b> only is calibrated out.
1	0	0	A <b>full system calibration</b> is initiated. First the internal DAC is calibrated, followed by the system gain error calibration, and finally the system offset error calibration.
1	0	1	First the <b>system gain error</b> is calibrated out followed by the <b>system offset error</b> .
1	1	0	The <b>system offset error</b> only is removed.
1	1	1	The <b>system gain error</b> only is removed.

# AD7854/AD7854L

## STATUS REGISTER

The arrangement of the status register is shown below. The status register is a read-only register and contains 16 bits of data. The status register is selected by writing to the control register and putting two 1s in RDSLT1 and RDSLT0. The function of the bits in the status register are described below. The power-up status of all bits is 0.

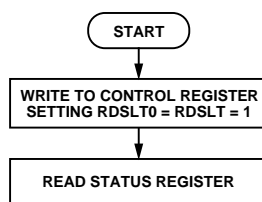


Figure 4. Flowchart for Reading the Status Register

MSB

ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	PMGT1	PMGT0
------	------	------	------	------	------	-------	-------

ONE	ONE	AMODE	BUSY	CALMD	CALSLT1	CALSLT0	STCAL
-----	-----	-------	------	-------	---------	---------	-------

LSB

### Status Register Bit Function Description

Bit	Mnemonic	Comment
15	ZERO	These six bits are always 0.
14	ZERO	
13	ZERO	
12	ZERO	
11	ZERO	
10	ZERO	
9	PMGT1	Power Management Bits. These bits along with the $\overline{\text{SLEEP}}$ pin will indicate if the part is in a power-down mode or not. See Table VI in Power-Down Section for description.
8	PMGT0	
7	ONE	Both these bits are always 1.
6	ONE	
5	AMODE	Analog Mode Bit. When this bit is a 0, the device is set up for the unipolar analog input range. When this bit is a 1, the device is set up for the bipolar analog input range.
4	BUSY	Conversion/Calibration Busy Bit. When this bit is 1, this indicates that there is a conversion or calibration in progress. When this bit is 0, there is no conversion or calibration in progress.
3	CALMD	Calibration Mode Bit. A 0 in this bit indicates a self-calibration is selected, and a 1 in this bit indicates a system calibration is selected (see Table III).
2	CALSLT1	Calibration Selection Bits and Start Calibration Bit. The STCAL bit is read as a 1 if a calibration is in progress and as a 0 if there is no calibration in progress. The CALSLT1 and CALSLT0 bits indicate which of the calibration registers are addressed for reading and writing (see section on the Calibration Registers for more details).
1	CALSLT0	
0	STCAL	

## CALIBRATION REGISTERS

The AD7854/AD7854L has 10 calibration registers in all, 8 for the DAC, 1 for offset and 1 for gain. Data can be written to or read from all 10 calibration registers. In self and system calibration, the part automatically modifies the calibration registers; only if the user needs to modify the calibration registers should an attempt be made to read from and write to the calibration registers.

### Addressing the Calibration Registers

The calibration selection bits in the control register CALSLT1 and CALSLT0 determine which of the calibration registers are addressed (See Table IV). The addressing applies to both the read and write operations for the calibration registers. The user should not attempt to read from and write to the calibration registers at the same time.

Table IV. Calibration Register Addressing

CALSLT1	CALSLT0	Comment
0	0	This combination addresses the <b>Gain (1), Offset (1) and DAC Registers (8)</b> . Ten registers in total.
0	1	This combination addresses the <b>Gain (1) and Offset (1) Registers</b> . Two registers in total.
1	0	This combination addresses the <b>Offset Register</b> . One register in total.
1	1	This combination addresses the <b>Gain Register</b> . One register in total.

### Writing to/Reading from the Calibration Registers

When writing to the calibration registers a write to the control register is required to set the CALSLT0 and CALSLT1 bits. When reading from the calibration registers a write to the control register is required to set the CALSLT0 and CALSLT1 bits and also to set the RDSLT1 and RDSLT0 bits to 10 (this addresses the calibration registers for reading). The calibration register pointer is reset on writing to the control register setting the CALSLT1 and CALSLT0 bits, or upon completion of all the calibration register write/read operations. When reset it points to the first calibration register in the selected write/read sequence. The calibration register pointer points to the gain calibration register upon reset in all but one case, this case being where the offset calibration register is selected on its own (CALSLT1 = 1, CALSLT0 = 0). Where more than one calibration register is being accessed, the calibration register pointer is automatically incremented after each calibration register write/read operation. The order in which the 10 calibration registers are arranged is shown in Figure 5. Read/Write operations may be aborted at any time before all the calibration registers have been accessed, and the next control register write operation resets the calibration register pointer. The flowchart in Figure 6 shows the sequence for writing to the calibration registers. Figure 7 shows the sequence for reading from the calibration registers.

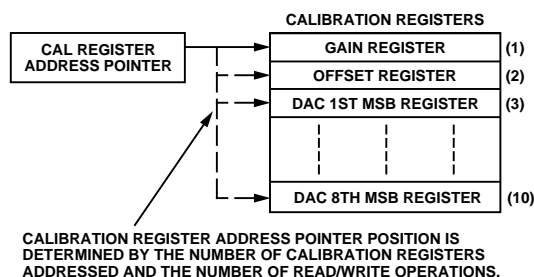


Figure 5. Calibration Register Arrangement

When reading from the calibration registers there are always two leading zeros for each of the registers.

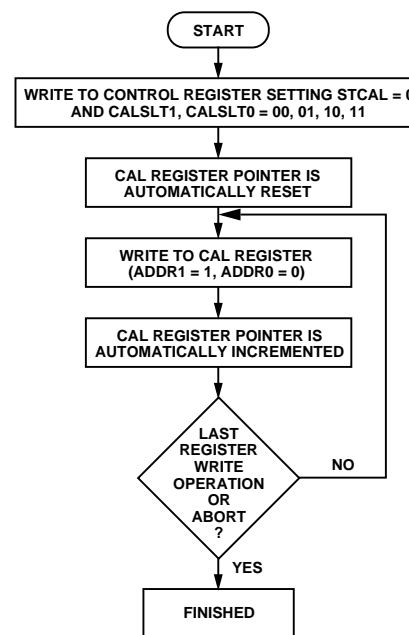


Figure 6. Flowchart for Writing to the Calibration Registers

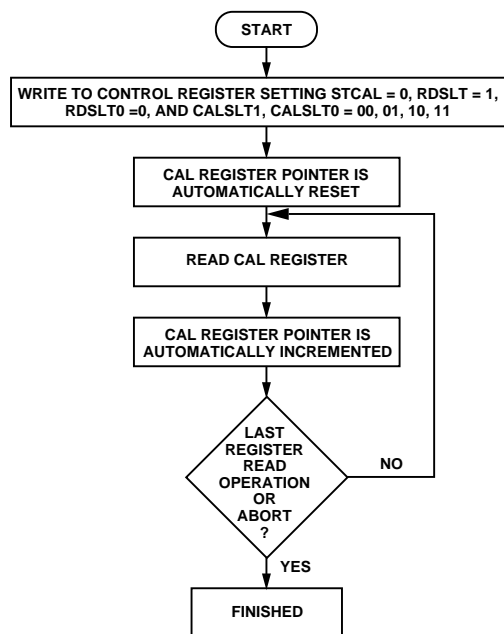


Figure 7. Flowchart for Reading from the Calibration Registers

#### Adjusting the Offset Calibration Register

The offset calibration register contains 16 bits. The two MSBs are zero and the 14 LSBs contain offset data. By changing the contents of the offset register, different amounts of offset on the analog input signal can be compensated for. Increasing the number in the offset calibration register compensates for negative offset on the analog input signal, and decreasing the number in the offset calibration register compensates for positive offset on the analog input signal. The default value of the offset calibration register is 0010 0000 0000 0000 approximately. This is not the exact value, but the value in the offset register should be close to this value. Each of the 14 data bits in the offset register is binary weighted; the MSB has a weighting of 5% of the reference voltage, the MSB-1 has a weighting of 2.5%, the MSB-2 has a weighting of 1.25%, and so on down to the LSB which has a weighting of 0.0006%. This gives a resolution of

$\pm 0.0006\%$  of  $V_{REF}$  approximately. The resolution can also be expressed as  $\pm (0.05 \times V_{REF})/2^{13}$  volts. This equals  $\pm 0.015$  mV, with a 2.5 V reference. The maximum offset that can be compensated for is  $\pm 5\%$  of the reference voltage, which equates to  $\pm 125$  mV with a 2.5 V reference and  $\pm 250$  mV with a 5 V reference.

*Q. If a +20 mV offset is present in the analog input signal and the reference voltage is 2.5 V, what code needs to be written to the offset register to compensate for the offset ?*

*A. 2.5 V reference implies that the resolution in the offset register is  $5\% \times 2.5 \text{ V}/2^{13} = 0.015$  mV.  $+20 \text{ mV}/0.015 \text{ mV} = 1310.72$ ; rounding to the nearest number gives 1311. In binary terms this is 00 0101 0001 1111, therefore decrease the offset register by 00 0101 0001 1111.*

This method of compensating for offset in the analog input signal allows for fine tuning the offset compensation. If the offset on the analog input signal is known, there is no need to apply the offset voltage to the analog input pins and do a system calibration. The offset compensation can take place in software.

#### Adjusting the Gain Calibration Register

The gain calibration register contains 16 bits. The two MSBs are zero and the 14 LSBs contain gain data. As in the offset calibration register the data bits in the gain calibration register are binary weighted, with the MSB having a weighting of 2.5% of the reference voltage. The gain register value is effectively multiplied by the analog input to scale the conversion result over the full range. Increasing the gain register compensates for a smaller analog input range and decreasing the gain register compensates for a larger input range. The maximum analog input range that the gain register can compensate for is 1.025 times the reference voltage, and the minimum input range is 0.975 times the reference voltage.

**CIRCUIT INFORMATION**

The AD7854/AD7854L is a fast, 12-bit single supply A/D converter. The part requires an external 4 MHz/1.8 MHz master clock (CLKIN), two  $C_{REF}$  capacitors, a  $\overline{CONVST}$  signal to start conversion and power supply decoupling capacitors. The part provides the user with track/hold, on-chip reference, calibration features, A/D converter and parallel interface logic functions on a single chip. The A/D converter section of the AD7854/AD7854L consists of a conventional successive-approximation converter based around a capacitor DAC. The AD7854/AD7854L accepts an analog input range of 0 to  $+V_{REF}$ .  $V_{REF}$  can be tied to  $V_{DD}$ . The reference input to the part connected via a 150 k $\Omega$  resistor to the internal 2.5 V reference and to the on-chip buffer.

A major advantage of the AD7854/AD7854L is that a conversion can be initiated in software as well as applying a signal to the  $\overline{CONVST}$  pin. Another innovative feature of the AD7854/AD7854L is self-calibration on power-up to give superior dc accuracy. The part should be allowed some time after power-up and after the  $\overline{CONVST}$  signal is applied to perform this automatic calibration before any reading or writing takes place. The part is available in a 28-pin SSOP package and this offers the user considerable spacing saving advantages over alternative solutions. The AD7854L version typically consumes only 5.5 mW making it ideal for battery-powered applications.

**CONVERTER DETAILS**

The master clock for the part is applied to the CLKIN pin. Conversion is initiated on the AD7854/AD7854L by pulsing the  $\overline{CONVST}$  input or by writing to the control register and setting the  $\overline{CONVST}$  bit to 1. On the rising edge of  $\overline{CONVST}$  (or at the end of the control register write operation), the on-chip

track/hold goes from track to hold mode. The falling edge of the CLKIN signal which follows the rising edge of  $\overline{CONVST}$  initiates the conversion, provided the rising edge of  $\overline{CONVST}$  (or  $\overline{WR}$  when converting via the control register) occurs typically at least 10 ns before this CLKIN edge. The conversion takes 16.5 CLKIN periods from this CLKIN falling edge. If the 10 ns setup time is not met, the conversion takes 17.5 CLKIN periods.

The time required by the AD7854/AD7854L to acquire a signal depends upon the source resistance connected to the AIN(+) input. Please refer to the Acquisition Time section for more details.

When a conversion is completed, the BUSY output goes low, and the result of the conversion can be read by accessing the data through the data bus. To obtain optimum performance from the part, read or write operations should not occur during the conversion or less than 200 ns prior to the next  $\overline{CONVST}$  rising edge. Reading/writing during conversion typically degrades the Signal to (Noise + Distortion) by less than 0.5 dBs. The AD7854 can operate at throughput rates of over 200 kSPS (up to 100 kSPS for the AD7854L).

With the AD7854L, 100 kSPS throughput can be obtained as follows: the CLKIN and  $\overline{CONVST}$  signals are arranged to give a conversion time of 16.5 CLKIN periods as described above and 1.5 CLKIN periods are allowed for the acquisition time. With a 1.8 MHz clock, this gives a full cycle time of 10  $\mu$ s, which equates to a throughput rate of 100 kSPS.

When using the software conversion start for maximum throughput, the user must ensure the control register write operation extends beyond the falling edge of BUSY. The falling edge of BUSY resets the  $\overline{CONVST}$  bit to 0 and allows it to be reprogrammed to 1 to start the next conversion.

*Figure 8. Typical Circuit*

# AD7854/AD7854L

## TYPICAL CONNECTION DIAGRAM

Figure 8 shows a typical connection diagram for the AD7854/AD7854L. The AGND and the DGND pins are connected together at the device for good noise suppression. The first  $\overline{\text{CONVST}}$  applied after power-up starts the automatic calibration sequence. The  $\overline{\text{WR}}$  line is tied to  $\text{DV}_{\text{DD}}$  to ensure that there is no writing to the device. Applying the RD and CS signals causes the conversion result to be output on the 12 data pins. Note that after power is applied to  $\text{AV}_{\text{DD}}$  and  $\text{DV}_{\text{DD}}$ , and the  $\overline{\text{CONVST}}$  signal is applied, the part requires (70 ms + 1/sample rate) for the internal reference to settle and for the automatic calibration on power-up to be completed.

For applications where power consumption is a major concern, the power-down options can be programmed by writing to the part. See Power-Down section for more detail on low power applications.

## ANALOG INPUT

The equivalent analog input circuit is shown in Figure 9. During the acquisition interval the switches are both in the track position and the AIN(+) charges the 20 pF capacitor through the 125  $\Omega$  resistance. On the rising edge of  $\overline{\text{CONVST}}$  switches SW1 and SW2 go into the hold position retaining charge on the 20 pF capacitor as a sample of the signal on AIN(+). The AIN(-) is connected to the 20 pF capacitor, and this unbalances the voltage at Node A at the input of the comparator. The capacitor DAC adjusts during the remainder of the conversion cycle to restore the voltage at Node A to the correct value. This action transfers a charge, representing the analog input signal, to the capacitor DAC which in turn forms a digital representation of the analog input signal. The voltage on the AIN(-) pin directly influences the charge transferred to the capacitor DAC at the hold instant. If this voltage changes during the conversion period, the DAC representation of the analog input voltage is altered. Therefore it is most important that the voltage on the AIN(-) pin remains constant during the conversion period. Furthermore, it is recommended that the AIN(-) pin is always connected to AGND or to a fixed dc voltage.

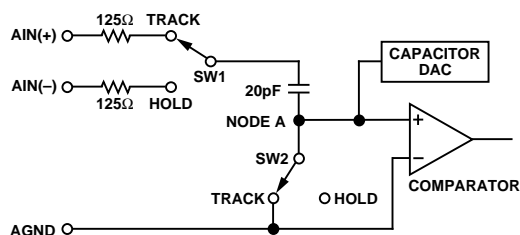


Figure 9. Analog Input Equivalent Circuit

## Acquisition Time

The track-and-hold amplifier enters its tracking mode on the falling edge of the BUSY signal. The time required for the track-and-hold amplifier to acquire an input signal depends on how quickly the 20 pF input capacitance is charged. There is a minimum acquisition time of 400 ns. For large source impedances, >2 k $\Omega$ , the acquisition time is calculated using the formula:

$$t_{ACQ} = 9 \times (R_{IN} + 125 \Omega) \times 20 \text{ pF}$$

where  $R_{IN}$  is the source impedance of the input signal, and 125  $\Omega$ , 20 pF is the input R, C.

## DC/AC Applications

For dc applications, high source impedances are acceptable, provided there is enough acquisition time between conversions to charge the 20 pF capacitor. For example with  $R_{IN} = 5 \text{ k}\Omega$ , the required acquisition time is 922 ns.

For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC low-pass filter on the AIN(+) pin, as shown in Figure 11. In applications where harmonic distortion and signal to noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. They may require the use of an input buffer amplifier. The choice of the amplifier is a function of the particular application.

The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases. Figure 10 shows a graph of the total harmonic distortion vs. analog input signal frequency for different source impedances. With the setup as in Figure 11, the THD is at the -90 dB level. With a source impedance of 1 k $\Omega$  and no capacitor on the AIN(+) pin, the THD increases with frequency.

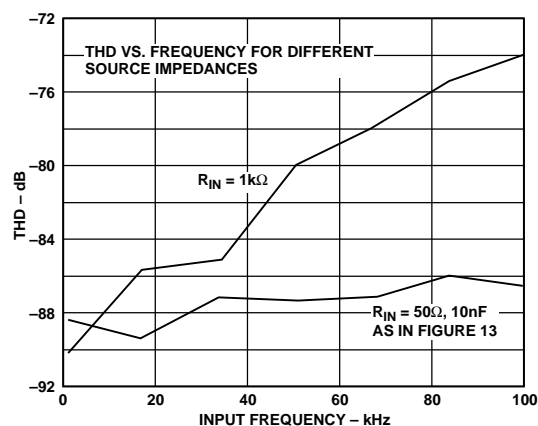


Figure 10. THD vs. Analog Input Frequency

In a single supply application (both 3 V and 5 V), the V+ and V- of the op amp can be taken directly from the supplies to the AD7854/AD7854L which eliminates the need for extra external power supplies. When operating with rail-to-rail inputs and outputs at frequencies greater than 10 kHz, care must be taken in selecting the particular op amp for the application. In particular, for single supply applications the input amplifiers should be connected in a gain of -1 arrangement to get the optimum performance. Figure 11 shows the arrangement for a single supply application with a 50  $\Omega$  and 10 nF low-pass filter (cutoff frequency 320 kHz) on the AIN(+) pin. Note that the 10 nF is a capacitor with good linearity to ensure good ac performance. Recommended single supply op amps are the AD820 and the AD820-3V.



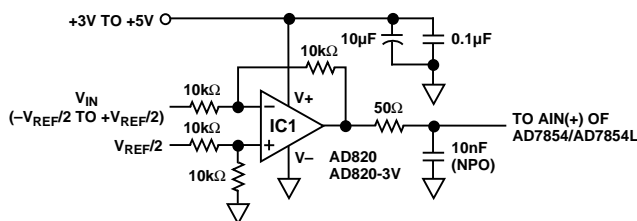


Figure 11. Analog Input Buffering

## Input Ranges

The analog input range for the AD7854/AD7854L is 0 V to  $V_{REF}$  in both the unipolar and bipolar ranges.

The only difference between the unipolar range and the bipolar range is that in the bipolar range the  $AIN(-)$  should be biased up to at least  $+V_{REF}/2$  and the output coding is twos complement (See Table V and Figures 14 and 15).

Table V. Analog Input Connections

Analog Input Range	Input Connections	Connection Diagram
0 V to $V_{REF}$ <sup>1</sup>	$V_{IN}$ AGND	Figure 12
$\pm V_{REF}/2$ <sup>2</sup>	$V_{IN}$ $V_{REF}/2$	Figure 13

## NOTES

<sup>1</sup>Output code format is straight binary.

<sup>2</sup>Range is  $\pm V_{REF}/2$  biased about  $V_{REF}/2$ . Output code format is twos complement.

Note that the  $AIN(-)$  pin on the AD7854/AD7854L can be biased up above AGND in the unipolar mode, or above  $V_{REF}/2$  in bipolar mode if required. The advantage of biasing the lower end of the analog input range away from AGND is that the analog input does not have to swing all the way down to AGND. Thus, in single supply applications the input amplifier does not have to swing all the way down to AGND. The upper end of the analog input range is shifted up by the same amount. Care must be taken so that the bias applied does not shift the upper end of the analog input above the  $AV_{DD}$  supply. In the case where the reference is the supply,  $AV_{DD}$ , the  $AIN(-)$  should be tied to AGND in unipolar mode or to  $AV_{DD}/2$  in bipolar mode.

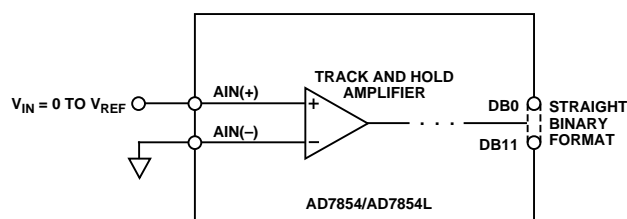


Figure 12. 0 to  $V_{REF}$  Unipolar Input Configuration

## Transfer Functions

For the unipolar range the designed code transitions occur midway between successive integer LSB values (i.e.,  $1/2$  LSB,  $3/2$  LSBs,  $5/2$  LSBs . . .  $FS - 3/2$  LSBs). The output coding is

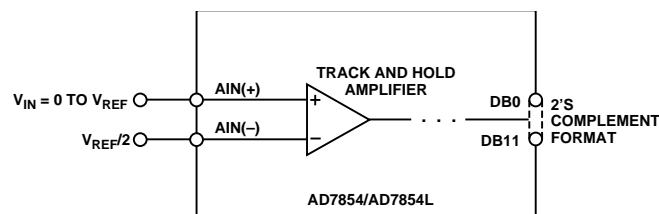


Figure 13.  $\pm V_{REF}/2$  about  $V_{REF}/2$  Bipolar Input Configuration

straight binary for the unipolar range with  $1 \text{ LSB} = FS/4096 = 3.3 \text{ V}/4096 = 0.8 \text{ mV}$  when  $V_{REF} = 3.3 \text{ V}$ . The ideal input/output transfer characteristic for the unipolar range is shown in Figure 14.

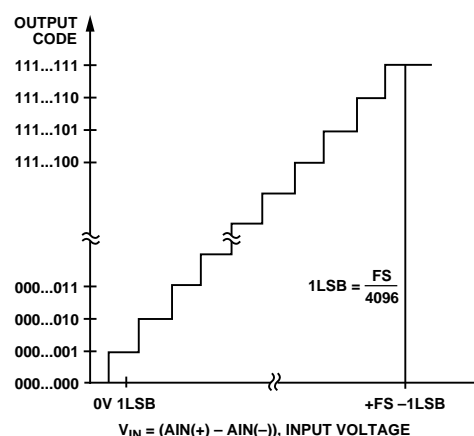


Figure 14. AD7853/AD7853L Unipolar Transfer Characteristic

Figure 13 shows the AD7854/AD7854L's  $\pm V_{REF}/2$  bipolar analog input configuration.  $AIN(+)$  cannot go below 0 V, so for the full bipolar range,  $AIN(-)$  should be biased to at least  $+V_{REF}/2$ . Once again the designed code transitions occur midway between successive integer LSB values. The output coding is twos complement with  $1 \text{ LSB} = 4096 = 3.3 \text{ V}/4096 = 0.8 \text{ mV}$ . The ideal input/output transfer characteristic is shown in Figure 15.

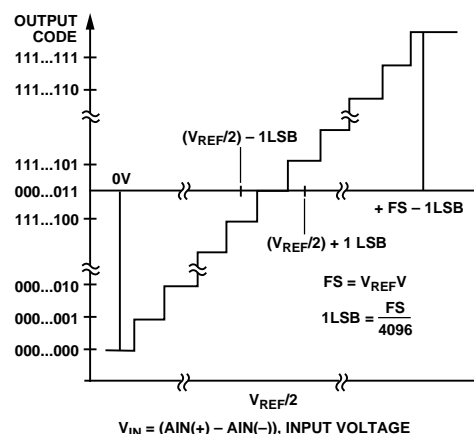


Figure 15. AD7854/AD7854L Bipolar Transfer Characteristic



# AD7854/AD7854L

## REFERENCE SECTION

For specified performance, it is recommended that when using an external reference, this reference should be between 2.3 V and the analog supply  $AV_{DD}$ . The connections for the reference pins are shown below. If the internal reference is being used, the  $REF_{IN}/REF_{OUT}$  pin should be decoupled with a 10 nF capacitor to AGND very close to the  $REF_{IN}/REF_{OUT}$  pin. These connections are shown in Figure 16.

If the internal reference is required for use external to the ADC, it should be buffered at the  $REF_{IN}/REF_{OUT}$  pin and a 10 nF capacitor should be connected from this pin to AGND. The typical noise performance for the internal reference, with 5 V supplies is 150 nV/ $\sqrt{\text{Hz}}$  @ 1 kHz and dc noise is 100  $\mu\text{V}$  p-p.

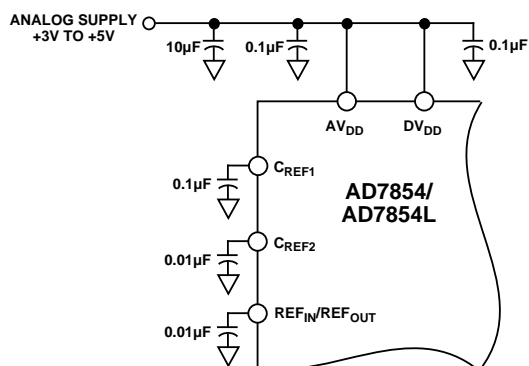


Figure 16. Relevant Connections Using Internal Reference

The  $REF_{IN}/REF_{OUT}$  pin may be overdriven by connecting it to an external reference. This is possible due to the series resistance from the  $REF_{IN}/REF_{OUT}$  pin to the internal reference. This external reference can be in the range 2.3 V to  $AV_{DD}$ . When using  $AV_{DD}$  as the reference source, the 10 nF capacitor from the  $REF_{IN}/REF_{OUT}$  pin to AGND should be as close as possible to the  $REF_{IN}/REF_{OUT}$  pin, and also the  $C_{REF1}$  pin should be connected to  $AV_{DD}$  to keep this pin at the same voltage as the reference. The connections for this arrangement are shown in Figure 17. When using  $AV_{DD}$  it may be necessary to add a resistor in series with the  $AV_{DD}$  supply. This has the effect of filtering the noise associated with the  $AV_{DD}$  supply.

Note that when using an external reference, the voltage present at the  $REF_{IN}/REF_{OUT}$  pin is determined by the external reference source resistance and the series resistance of 150  $\text{k}\Omega$  from the  $REF_{IN}/REF_{OUT}$  pin to the internal 2.5 V reference. Thus, a low source impedance external reference is recommended.

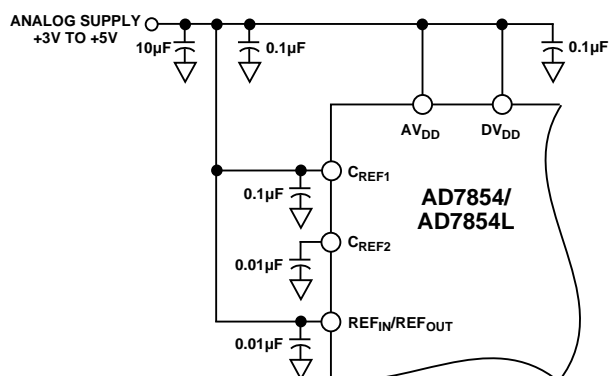


Figure 17. Relevant Connections,  $AV_{DD}$  as the Reference

## AD7854/AD7854L PERFORMANCE CURVES

Figure 18 shows a typical FFT plot for the AD7854 at 200 kHz sample rate and 10 kHz input frequency.

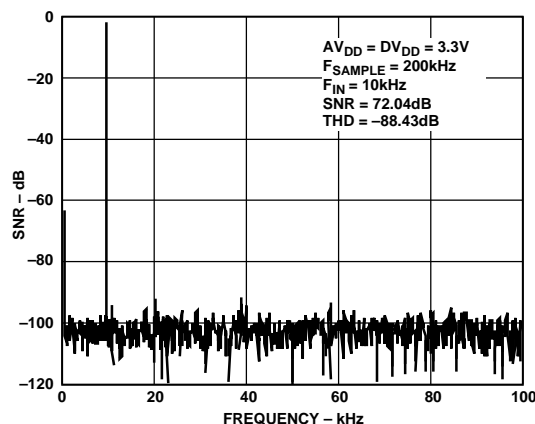


Figure 18. FFT Plot

Figure 19 shows the SNR versus frequency for different supplies and different external references.

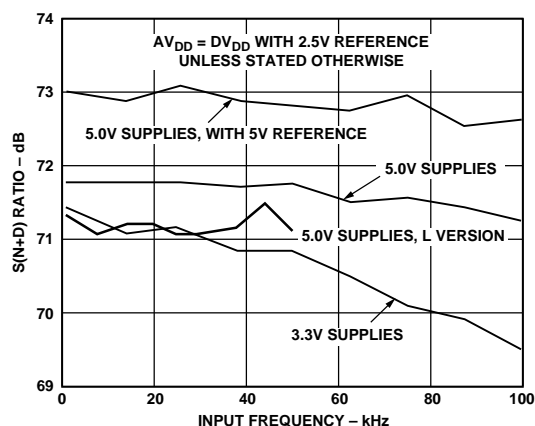


Figure 19. SNR vs. Frequency

Figure 20 shows the power supply rejection ratio versus frequency for the part. The power supply rejection ratio is defined as the ratio of the power in ADC output at frequency  $f$  to the power of a full-scale sine wave.

$$PSRR \text{ (dB)} = 10 \log (P_f/P_{fs})$$

$P_f$  = Power at frequency  $f$  in ADC output,  $P_{fs}$  = power of a full-scale sine wave. Here a 100 mV peak-to-peak sine wave is coupled onto the  $AV_{DD}$  supply while the digital supply is left unaltered. Both the 3.3 V and 5.0 V supply performances are shown.

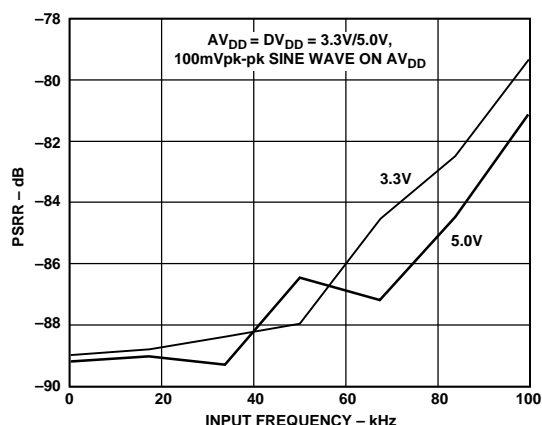


Figure 20. PSRR vs. Frequency

### POWER-DOWN OPTIONS

The AD7854/AD7854L should be left idle for (70 ms + 1/sample rate) typically after the  $AV_{DD}$  and the  $DV_{DD}$  power-up, and the first  $\overline{CONVST}$  signal is applied, to allow the internal reference to settle and the automatic calibration on power-up to be completed. The SLEEP pin can be hardwired to DGND before power-up as the part disables the function of the SLEEP pin while the automatic calibration on power-up is being performed.

The AD7854/AD7854L provides two power-down methods of operation. These methods are full power-down and partial power-down. These power-down methods are controlled by the

PMGT1 and PMGT0 bits in the control register. When both these bits are 0 (default status on power-up), the AD7854/AD7854L is in normal mode of operation. With these bits at 0, 1 the AD7854/AD7854L enters a full power-down mode after every conversion. With these bits at 1, 0 the part enters a full power-down mode, whether a conversion is in progress or not. Finally, with these bits at 1, 1 the part enters partial power-down after every conversion.

The advantage of partial power-down is that the part requires significantly less time to “power-up” than from full power-down. In partial power-down, the reference voltage stays powered up, so if this is being used external to the AD7854/AD7854L it is still available even though the rest of the AD7854/AD7854L is powered down. Table VI summarizes the power management options while Table VII shows typical power-up times when using the 2.5 V internal reference. The capacitor values between  $C_{REF1}$ ,  $C_{REF2}$ ,  $REF_{IN}/REF_{OUT}$  and AGND are also listed. The power-up time is defined as the time taken for the output code to settle to within  $\pm 0.5$  LSBs of its final value. If a power-up time shorter than that quoted in Table VII is used, the error associated with the output code increases. For a power-up time of 10  $\mu$ s from partial power-down mode, the output code settles to within  $\pm 3$  LSBs typically of its final value. When using an external reference, the power-up time required is less than the figures quoted in Table VII.

A typical connection diagram for a low power application is shown in Figure 21.

Figure 21. Typical Low Power Circuit

# AD7854/AD7854L

**Table VI. Power Management Options**

PMGT1 Bit	PMGT0 Bit	Comment
0	0	<b>Normal Operation</b> (Default Condition After Power-On)
0	1	<b>Full Power-Down</b> if Not Calibrating or Converting
1	0	<b>Full Power-Down</b>
1	1	<b>Partial Power-Down</b> if Not Converting

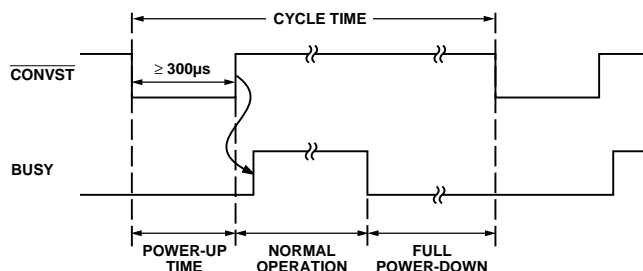
**Table VII. Power-Up Times**

C <sub>REF1</sub> (nF)	C <sub>REF2</sub> (nF)	Reference Capacitor (nF)	Power-Down Mode	Power-Up Delay (μs)
100	10	0.1	Full	300
100	10	0.1	Partial	50
10	1	0.1	Full	300
10	1	0.1	Partial	50

## POWER-UP/DOWN SEQUENCE

Power-up times and throughput rates quoted in this section are based on using the 2.5 V internal reference. If an external reference is used and is powered on constantly, or if AV<sub>DD</sub> is used as the reference, then the power-up times are shorter and the throughput rates higher.

The  $\overline{\text{CONVST}}$  pin may be used to wake the part from two of the power down modes (full power-down if not converting and partial power-down if not converting), rather than writing to the control register to wake up the part. First, the part should be put into one of these two power down modes by writing to the device (setting PMGT1 = 0 and PMGT0 = 1, or setting both PMGT1 and PMGT0 = 1). When using  $\overline{\text{CONVST}}$  to wake the part, it is the falling edge of the  $\overline{\text{CONVST}}$  signal that “wakes” it.  $\overline{\text{CONVST}}$  must remain low for at least the power up time quoted in Table VII when using the internal reference ( $\overline{\text{CONVST}}$  need only remain low for 50 μs when using an external reference). This allows the part to settle before the start of the next conversion. Figure 22 shows the timing of  $\overline{\text{CONVST}}$  for bringing the part out of full power down when using the internal reference.



**Figure 22. Timing for using  $\overline{\text{CONVST}}$  to “wake-up” the AD7854/AD7854L**

## Writing to AD7854/AD7854L

The sequence of events here uses the  $\overline{\text{CONVST}}$  bit in the control register to start the conversion. Alternatively the  $\overline{\text{CONVST}}$  pin may be used as in Figure 22. When writing to the AD7854/AD7854L there are a number of different ways to utilize the power-down options. For applications which require throughput rates of less than 2 kHz, a full/partial power-down mode combination, or a full power-down mode on its own, may be used. For higher throughput rates the partial power-down mode should be used. Table VIII shows the recommended power-down mode to obtain the lowest current at a given throughput rate.

**Table VIII. Recommended Power-Down Mode for Lowest I<sub>DD</sub>**

Power-Down Mode	Maximum Throughput Rate
Full/Partial Combination	2 kHz
Partial	16 kHz

## Using Full and Partial Power-Down Combination

Using a full/partial power-down combination has the benefits of the low current associated with a full power-down and the speed of powering up from a partial power-down. It also gives the lowest current for a given throughput rate, one third of the current when using the full power-down mode on its own. Figure 23 shows the timing diagram for the full/partial power-down combination and Figure 24 shows the flowchart for the sequence of events. For the all 0s write operation described in the sequence, only the two MSBs need to be 0 to ensure that the rest of the data write is ignored. The supply current versus throughput rate for this power up/power down sequence is shown in Figure 25.

**Figure 23. Timing Sequence for Full/Partial Power-Down Combination**

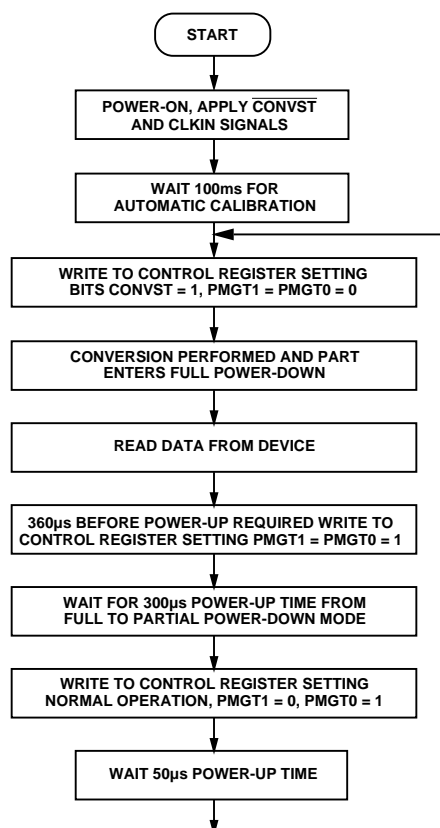


Figure 24. Flowchart for Full/Partial Power-Down Mode Combination

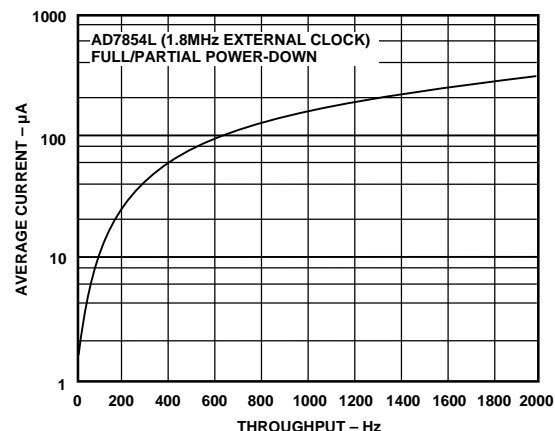


Figure 25. Supply Current vs. Throughput Rate with Full/Partial Power-Down Combination (Sequence as Illustrated in Figures 25 and 26)

#### Full Power-Down or Partial Power-Down

In some applications it may not be feasible to use a combination of full and partial power-down as shown in Figures 25 and 26. This may be for software overhead reasons or for applications requiring throughput rates greater than 2 kHz.

Using full power-down only allows for a maximum throughput rate of 2 kHz, but the supply current is three times or greater than for the full/partial power-down combination sequence described in Figures 25 and 26.

Using partial power-down allows for throughput rates up to 16 kHz (if  $AV_{DD}$  is used as the reference, the throughput rates can be > 16 kHz). Figures 28 and 29 show the timing/flowchart for power-up/down when using the partial power-down mode only. Figure 28 shows the Supply Current vs. Throughput rate for this sequence.

Figure 26. Timing Sequence for Partial Power-Down Only

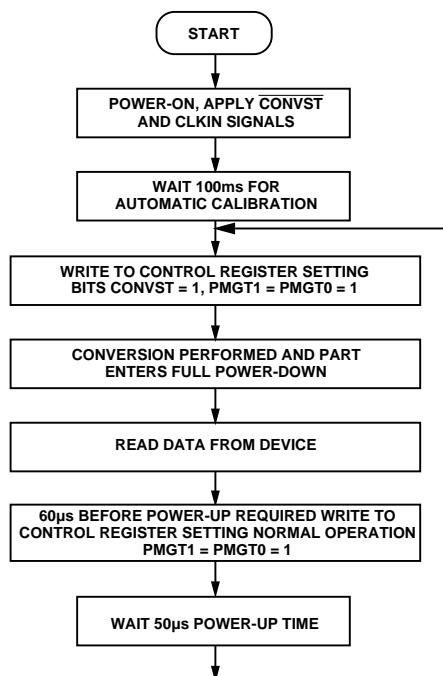


Figure 27. Flowchart for Partial Power-Down Only

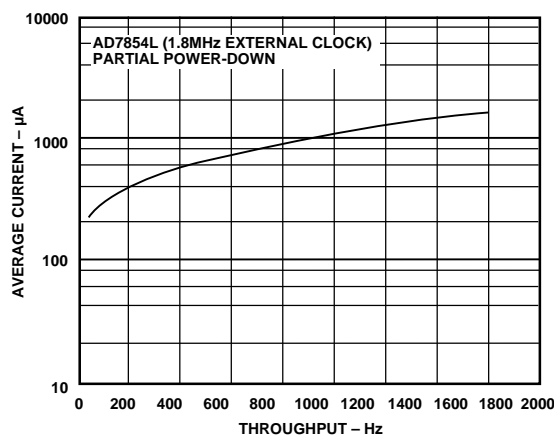


Figure 28. Supply Current vs. Throughput Rate with Partial Power-Down Only (Sequence as Illustrated in Figures 26 and 27)

## CALIBRATION SECTION

### Calibration Overview

The automatic calibration that is performed on power-up ensures that the calibration options covered in this section are not required in a significant amount of applications. A calibration does not have to be initiated unless the operating conditions change (CLKIN frequency, analog input mode, reference voltage, temperature, and supply voltages). The AD7854/AD7854L has a number of calibration features that may be required in some applications and there are a number of advantages in performing these different types of calibration. First, the internal errors in the ADC can be reduced significantly to give superior dc performance; and second, system offset and gain errors can be removed. This allows the user to remove reference errors (whether it be internal or external reference) and to make use of the full dynamic range of the AD7854/AD7854L by adjusting the analog input range of the part for a specific system.

There are two main calibration modes on the AD7854/AD7854L, self-calibration and system calibration. There are various options in both self-calibration and system calibration as outlined previously in Table III. All the calibration functions are initiated by writing to the control register and setting the STCAL bit to 1.

The duration of each of the different types of calibration is given in Table IX for the AD7854 with a 4 MHz master clock. These calibration times are master clock dependent. Therefore the calibration times for the AD7854L (CLKIN = 1.8 MHz) are larger than those quoted in Table IX.

Table IX. Calibration Times (AD7854 with 4 MHz CLKIN)

Type of Self- or System Calibration	Time
Full	31.25 ms
Gain + Offset	6.94 ms
Offset	3.47 ms
Gain	3.47 ms

### Automatic Calibration on Power-On

The automatic calibration on power-on is initiated by the first  $\overline{\text{CONVST}}$  pulse after the  $\text{AV}_{\text{DD}}$  and  $\text{DV}_{\text{DD}}$  power on. From the  $\overline{\text{CONVST}}$  pulse the part internally sets a 32/72 ms (4 MHz/1.8 MHz CLKIN) timeout. This time is large enough to ensure that the internal reference has settled before the calibration is performed. However, if an external reference is being used, this reference must have stabilized before the automatic calibration is initiated. This first  $\overline{\text{CONVST}}$  pulse also triggers the BUSY signal high and once the 32/72 ms has elapsed the BUSY signal goes low. At this point the next  $\overline{\text{CONVST}}$  pulse that is applied initiates the automatic full self calibration. This  $\overline{\text{CONVST}}$  pulse again triggers the BUSY signal high and after 32/72 ms (4 MHz/1.8 MHz CLKIN) the calibration is completed and the BUSY signal goes low. This timing arrangement is shown in Figure 29. The times in Figure 29 assume a 4 MHz / 1.8 MHz CLKIN signal.

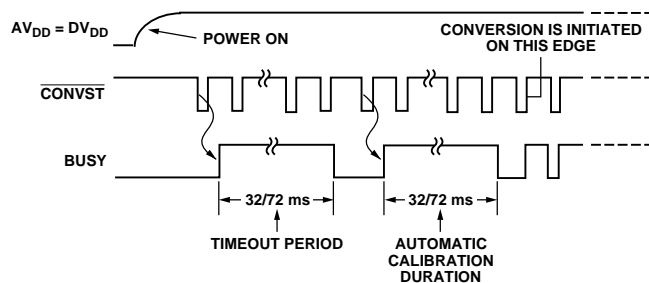


Figure 29. Timing arrangement for autocalibration on power-on.

The  $\overline{\text{CONVST}}$  signal is gated with the  $\text{BUSY}$  internally so that as soon as the timeout is initiated by the first  $\overline{\text{CONVST}}$  pulse all subsequent  $\overline{\text{CONVST}}$  pulses are ignored until the  $\text{BUSY}$  signal goes low, 32/72 ms later. The  $\overline{\text{CONVST}}$  pulse that follows after the  $\text{BUSY}$  signal goes low initiates an automatic full self calibration. This takes a further 32/72 ms. After calibration, the part is accurate to the 12-bit level and the specifications quoted on the data sheet apply, and all subsequent  $\overline{\text{CONVST}}$  pulses initiate conversions. There is no need to perform another calibration unless the operating conditions change or unless a system calibration is required.

This autocalibration at power-on is disabled if the user writes to the control register before the autocalibration is initiated. If the control register write operation occurs during the first 32/72 ms timeout period, then the  $\text{BUSY}$  signal stays high for the 32/72 ms and the  $\overline{\text{CONVST}}$  pulse that follows the  $\text{BUSY}$  going low does not initiate an automatic full self calibration. It initiates a conversion and all subsequent  $\overline{\text{CONVST}}$  pulses initiate conversions as well. If the control register write operation occurs when the automatic full self calibration is in progress, then the calibration is not aborted; the  $\text{BUSY}$  signal remains high until the automatic full self calibration is complete.

#### Self-Calibration Description

There are four different calibration options within the self-calibration mode. There is a full self-calibration where the DAC, internal offset, and internal gain errors are removed. There is the (Gain + Offset) self-calibration which removes the internal gain error and then the internal offset errors. The internal DAC is not calibrated here. Finally, there are the self-offset and self-gain calibrations which remove the internal offset errors and the internal gain errors respectively.

The internal capacitor DAC is calibrated by trimming each of the capacitors in the DAC. It is the ratio of these capacitors to each other that is critical, and so the calibration algorithm ensures that this ratio is at a specific value by the end of the calibration routine. For the offset and gain there are two separate capacitors, one of which is trimmed during offset calibration and one of which is trimmed during gain calibration.

In bipolar mode the midscale error is adjusted by an offset calibration and the positive full-scale error is adjusted by the gain calibration. In unipolar mode the zero-scale error is adjusted by the offset calibration and the positive full-scale error is adjusted by the gain calibration.

#### Self-Calibration Timing

Figure 30 shows the timing for a software full self-calibration. Here the  $\text{BUSY}$  line stays high for the full length of the self-calibration. A self-calibration is initiated by writing to the control register and setting the  $\text{STCAL}$  bit to 1. The  $\text{BUSY}$  line goes high at the end of the write to the control register, and  $\text{BUSY}$  goes low when the full self-calibration is complete after a time  $t_{\text{CAL}}$  as show in Figure 30.

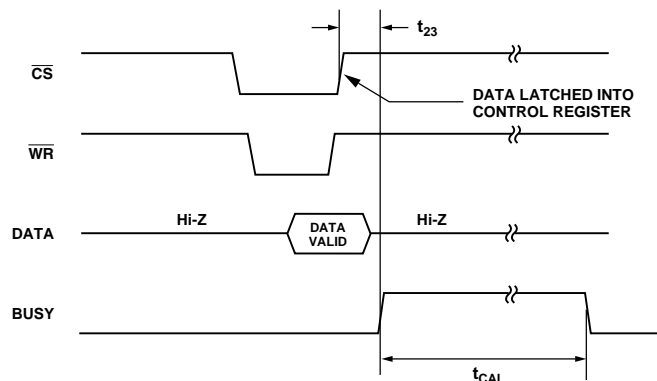


Figure 30. Timing Diagram for Full Self-Calibration

For the self-(gain + offset), self-offset and self-gain calibrations, the  $\text{BUSY}$  line is triggered high at the end of the write to the control register and stays high for the full duration of the self-calibration. The length of time for which  $\text{BUSY}$  is high depends on the type of self-calibration that is initiated. Typical values are given in Table IX. The timing diagram for the other self-calibration options is similar to that outlined in Figure 30.

#### System Calibration Description

System calibration allows the user to remove system errors external to the AD7854/AD7854L, as well as remove the errors of the AD7854/AD7854L itself. The maximum calibration range for the system offset errors is  $\pm 5\%$  of  $V_{\text{REF}}$  and for the system gain errors, it is  $\pm 2.5\%$  of  $V_{\text{REF}}$ . If the system offset or system gain errors are outside these ranges, the system calibration algorithm reduces the errors as much as the trim range allows.



# AD7854/AD7854L

Figures 33 through 35 illustrate why a specific type of system calibration might be used. Figure 31 shows a system offset calibration (assuming a positive offset) where the analog input range has been shifted upwards by the system offset after the system offset calibration is completed. A negative offset may also be removed by a system offset calibration.

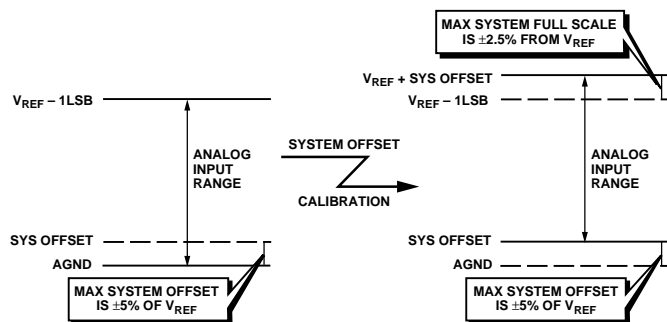


Figure 31. System Offset Calibration

Figure 32 shows a system gain calibration (assuming a system full scale greater than the reference voltage) where the analog input range has been increased after the system gain calibration is completed. A system full-scale voltage less than the reference voltage may also be accounted for by a system gain calibration.

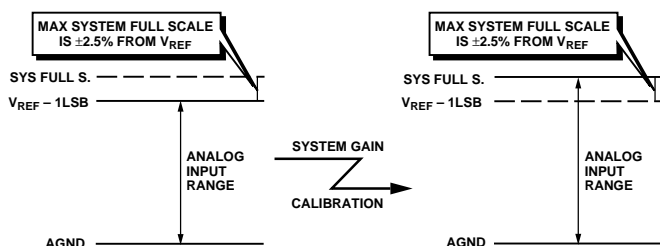


Figure 32. System Gain Calibration

Finally in Figure 33 both the system offset error and gain error are removed by the system offset followed by a system gain calibration. First the analog input range is shifted upwards by the positive system offset and then the analog input range is adjusted at the top end to account for the system full scale.

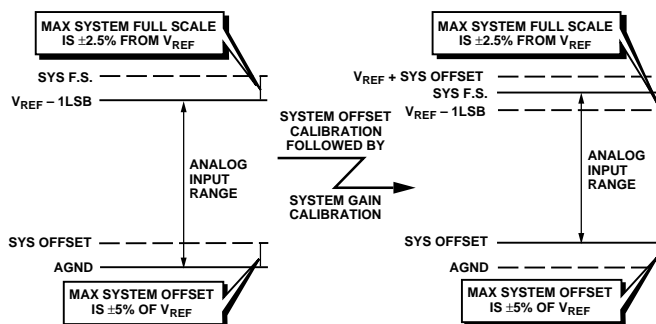


Figure 33. System (Gain + Offset) Calibration

## System Gain and Offset Interaction

The architecture of the AD7854/AD7854L leads to an interaction between the system offset and gain errors when a system calibration is performed. Therefore it is recommended to perform the cycle of a system offset calibration followed by a system gain calibration twice. When a system offset calibration is performed, the system offset error is reduced to zero. If this is followed by a system gain calibration, then the system gain error is now zero, but the system offset error is no longer zero. A second sequence of system offset error calibration followed by a system gain calibration is necessary to reduce system offset error to below the 12-bit level. The advantage of doing separate system offset and system gain calibrations is that the user has more control over when the analog inputs need to be at the required levels, and the  $\overline{\text{CONVST}}$  signal does not have to be used.

Alternatively, a system (gain + offset) calibration can be performed. At the end of one system (gain + offset) calibration, the system offset error is zero, while the system gain error is reduced from its initial value. Three system (gain + offset) calibrations are required to reduce the system gain error to below the 12-bit error level. There is never any need to perform more than three system (gain + offset) calibrations.

In bipolar mode the midscale error is adjusted for an offset calibration and the positive full-scale error is adjusted for the gain calibration; in unipolar mode the zero-scale error is adjusted for an offset calibration and the positive full-scale error is adjusted for a gain calibration.



### System Calibration Timing

The timing diagram in Figure 34 is for a software full system calibration. It may be easier in some applications to perform separate gain and offset calibrations so that the CONVST bit in the control register does not have to be programmed in the middle of the system calibration sequence. Once the write to the control register setting the bits for a full system calibration is completed, calibration of the internal DAC is initiated and the BUSY line goes high. The full-scale system voltage should be applied to the analog input pins, AIN(+) and AIN(–) at the start of calibration. The BUSY line goes low once the DAC and system gain calibration are complete. Next the system offset voltage should be applied across the AIN(+) and AIN(–) pins for a minimum setup time ( $t_{\text{SETUP}}$ ) of 100 ns before the rising edge of  $\overline{\text{CS}}$ . This second write to the control register sets the CONVST bit to 1 and at the end of this write operation the BUSY signal is triggered high (note that a  $\overline{\text{CONVST}}$  pulse can be applied instead of this second write to the control register). The BUSY signal is low after a time  $t_{\text{CAL2}}$  when the system offset calibration section is complete. The full system calibration is now complete.

The timing for a system (gain + offset) calibration is very similar to that of Figure 34, the only difference being that the time  $t_{\text{CAL1}}$  is replaced by a shorter time of the order of  $t_{\text{CAL2}}$  as the internal DAC is not calibrated. The BUSY signal signifies when the gain calibration is finished and when the part is ready for the offset calibration.

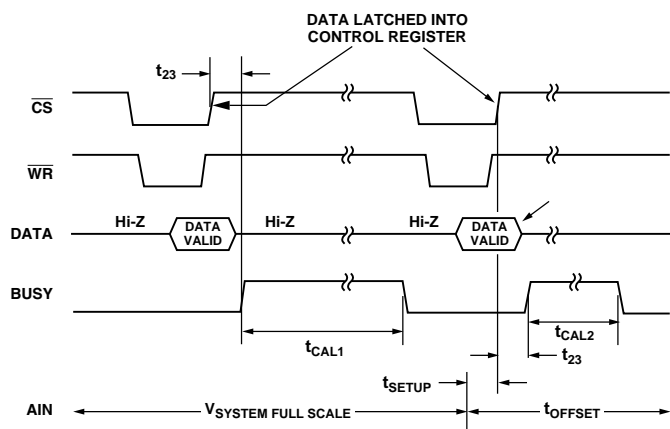


Figure 34. Timing Diagram for Full System Calibration

The timing diagram for a system offset or system gain calibration is shown in Figure 35. Here again a write to the control register initiates the calibration sequence. At the end of the control register write operation the BUSY line goes high and it stays high until the calibration sequence is finished. The analog input should be set at the correct level for a minimum setup time ( $t_{\text{SETUP}}$ ) of 100 ns before the CS rising edge and stay at the correct level until the BUSY signal goes low.

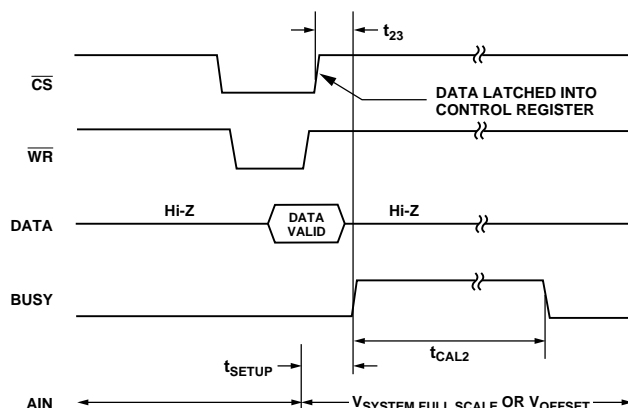


Figure 35. Timing Diagram for System Gain or System Offset Calibration

# AD7854/AD7854L

## PARALLEL INTERFACE

### Reading

The timing diagram for a read cycle is shown in Figure 36. The  $\overline{\text{CONVST}}$  and  $\text{BUSY}$  signals are not shown here as the read cycle may occur while a conversion is in progress or after the conversion is complete.

The  $\text{HBEN}$  signal is low for the first read and high for the second read. This ensures that it is the lower 12 bits of the 16-bit word are output in the first read and the 8 MSBs of the 16-bit word are output in the second read. If required, the  $\text{HBEN}$  signal may be high for the first read and low for the second read to ensure that the high byte is output in the first read and the lower byte in the second read. The  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  signals are gated together internally and level triggered active low. Both  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  may be tied together as the timing specification for  $t_5$  and  $t_6$  are both 0 ns min. The data is output a time  $t_8$  after both  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  go low. The  $\overline{\text{RD}}$  rising edge should be used to latch the data by the user and after a time  $t_9$  the data lines will go into their high impedance state.

In Figure 36, the first read outputs the 12 LSBs of the 16-bit word on pins  $\text{DB0}$  to  $\text{DB11}$  ( $\text{DB0}$  being the LSB of the 12-bit read). The second read outputs the 8 MSBs of the 16-bit word on pins  $\text{DB0}$  to  $\text{DB7}$  ( $\text{DB0}$  being the LSB of the 8-bit read). If the system has a 12-bit or a 16-bit data bus, only one read operation is necessary to obtain the 12-bit conversion result (12 bits are output in the first read). A second read operation is not required.

If the system has an 8-bit data bus then two reads are needed. Pins  $\text{DB0}$  to  $\text{DB7}$  should be connected the 8-bit data bus. Pins  $\text{DB8}$  to  $\text{DB11}$  should be tied to  $\text{DGND}$  or  $\text{DVDD}$  via 10 k $\Omega$  resistors. With this arrangement,  $\text{HBEN}$  is pulled low for the first read and the 8 LSBs of the 16-bit word are output on pins  $\text{DB0}$  to  $\text{DB7}$  (data on pins  $\text{DB8}$  to  $\text{DB11}$  will be ignored).  $\text{HBEN}$  is pulled high for the second read and now the 8 MSBs of the 16-bit word are output on pins  $\text{DB0}$  to  $\text{DB7}$ .

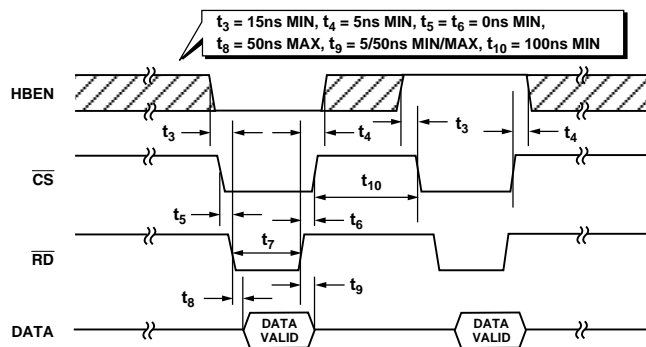


Figure 36. Read Cycle Timing Diagram Using  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$

In the case where the AD7854/AD7854L is operated as a read-only ADC, the  $\overline{\text{WR}}$  pin can be tied permanently high. The read operation need only consist of one read if the system has a 12-bit or a 16-bit data bus.

When both the  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  signals are tied permanently low a different timing arrangement results, as shown in Figure 37. Here the data is output a time  $t_{20}$  before the falling edge of the  $\text{BUSY}$  signal. This allows the falling edge of  $\text{BUSY}$  to be used for latching the data. Again if  $\text{HBEN}$  is low during the conversion the 12 LSBs of the 16-bit word will be output on pins  $\text{DB0}$  to  $\text{DB11}$ . Bringing  $\text{HBEN}$  high causes the 8 MSBs of the 16-bit word to be output on pins  $\text{DB0}$  to  $\text{DB7}$ . Note that with this arrangement the data lines are always active.

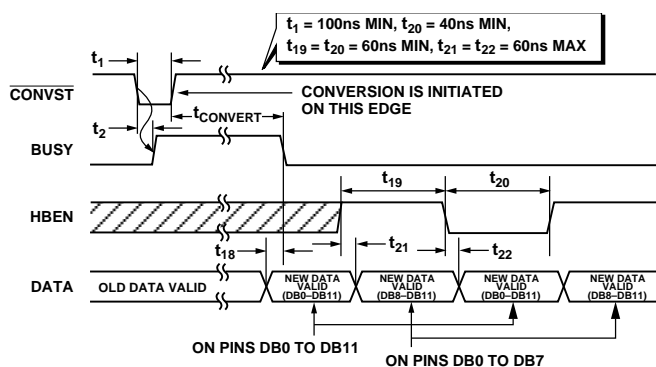


Figure 37. Read Cycle Timing Diagram with  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  Tied Low

### Writing

The timing diagram for a write cycle is shown in Figure 38. The  $\overline{\text{CONVST}}$  and  $\text{BUSY}$  signals are not shown here as the write cycle may occur while a conversion is in progress or after the conversion is complete.

To write a 16-bit word to the AD7854/AD7854L, two 8-bit writes are required. The  $\text{HBEN}$  signal must be low for the first write and high for the second write. This ensures that it is the lower 8 bits of the 16-bit word are latched in the first write and the 8 MSBs of the 16-bit word are latched in the second write. For both write operations the 8 bits of data should be present on pins  $\text{DB0}$  to  $\text{DB7}$  ( $\text{DB0}$  being the LSB of the 8-bit write). Any data on pins  $\text{DB8}$  to  $\text{DB11}$  is ignored when writing to the device. The  $\overline{\text{CS}}$  and  $\overline{\text{WR}}$  signals are gated together internally. Both  $\overline{\text{CS}}$  and  $\overline{\text{WR}}$  may be tied together as the timing specification for  $t_{13}$  and  $t_{14}$  are both 0 ns min. The data is latched on the rising edge of  $\overline{\text{WR}}$ . The data needs to be setup a time  $t_{16}$  before the  $\overline{\text{WR}}$  rising edge and held for a time  $t_{17}$  after the  $\overline{\text{WR}}$  rising edge.

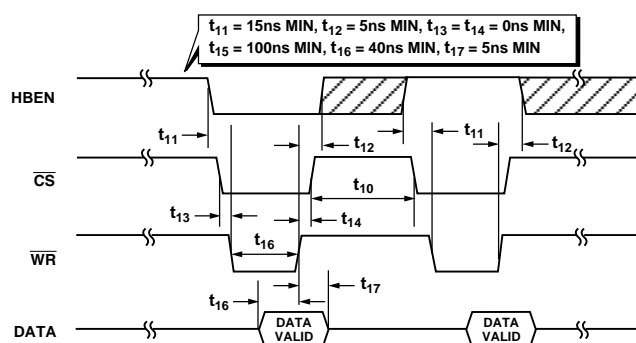


Figure 38. Write cycle timing diagram

### Resetting the Parallel Interface

If random data has been inadvertently written to the test register, it is necessary to write the 16-bit word 0100 0000 0000 0000 (in two 8-bit bytes) to restore the test register to its default value.

# AD7854/AD7854L

## PARALLEL INTERFACING

The parallel port on the AD7854/AD7854L allows the device to be interfaced to microprocessors or DSP processors as a memory mapped or I/O mapped device. The  $\overline{CS}$  and  $\overline{RD}$  inputs are common to all memory peripheral interfacing. Typical interfaces to different processors are shown in Figures 39 to 42.

In all the interfaces shown, an external timer controls the  $\overline{CONVST}$  input of the AD7854/AD7854L and the  $\overline{BUSY}$  output interrupts the host DSP. Also, the  $\overline{HBEN}$  pin is connected to address line A0 (XA0 in the case of the TMS320C30). This maps the AD7854/AD7854L to two locations in the processor memory space, ADCaddr and ADCaddr+1. Thus when writing to the ADC, first the 8 LSBs of the 16-bit are written to address location ADCaddr and then the 8 MSBs to location ADCaddr+1. All the interfaces use a 12-bit data bus, so only one read is needed from location ADCaddr to access the ADC output data register or the status register. To read from the other registers, the 8 MSBs must be read from location ADCaddr+1. Interfacing to 8-bit bus systems is similar, except that two reads are required to obtain data from all the registers.

### AD7854/AD7854L to ADSP-21xx

Figure 39 shows the AD7854/AD7854L interfaced to the ADSP-21xx series of DSPs as a memory mapped device. A single wait state may be necessary to interface the AD7854/AD7854L to the ADSP-21xx depending on the clock speed of the DSP. This wait state can be programmed via the data memory waitstate control register of the ADSP-21xx (please see *ADSP-2100 Family Users Manual* for details). The following instruction reads data from the AD7854/AD7854L:

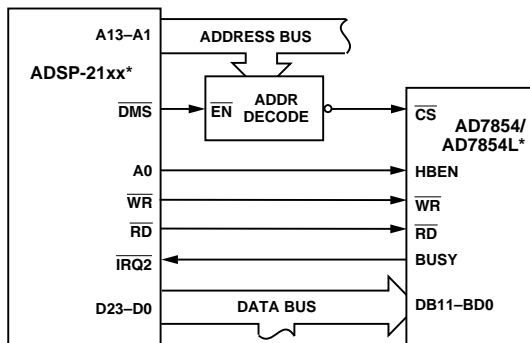
$AX0 = DM(ADCaddr)$

Data can be written to the AD7854/AD7854L using the instructions:

$DM(ADCaddr) = AY0$

$DM(ADCaddr+1) = AY1$

where ADCaddr is the address of the AD7854/AD7854L in ADSP-21xx data memory, AX0 contains the data read from the ADC, and AY0 contains the 8 LSBs and AY1 the 8 MSBs of data written to the AD7854/AD7854L.



\*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 39. AD7854/AD7854L to ADSP-21xx Parallel Interface

### AD7854/AD7854L to TMS32020, TMS320C25 and TMS320C5x

A parallel interface between the AD7854/AD7854L and the TMS32020, TMS320C25 and TMS320C5X family of DSPs are shown in Figure 40. The memory mapped addresses chosen for the AD7854/AD7854L should be chosen to fall in the I/O memory space of the DSPs.

The parallel interface on the AD7854/AD7854L is fast enough to interface to the TMS32020 with no extra wait states. In the TMS320C25 interface, data accesses may be slowed sufficiently when reading from and writing to the part to require the insertion of one wait state. In such a case, this wait state can be generated using the single OR gate to combine the  $\overline{CS}$  and  $\overline{MSC}$  signals to drive the  $\overline{READY}$  line of the TMS320C25, as shown in Figure 40. Extra wait states are necessary when using the TMS320C5x at their fastest clock speeds. Wait states can be programmed via the IOWSR and CWSR registers (please see TMS320C5x User Guide for details).

Data is read from the ADC using the following instruction:

$IN D, ADCaddr$

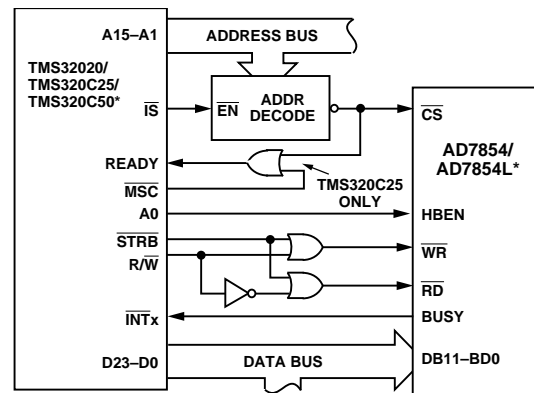
where  $D$  is the memory location where the data is to be stored and ADCaddr is the I/O address of the AD7854/AD7854L.

Data is written to the ADC using the following two instructions:

$OUT D8LSB, ADCaddr$

$OUT D8MSB, ADCaddr+1$

where D8LSB is the memory location where the 8 LSBs of data are stored, D8MSB is the location where the 8 MSBs of data are stored and ADCaddr and ADCaddr+1 are the I/O memory spaces that the AD7854/AD7854L is mapped into.



\*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 40. AD7854/AD7854L to TMS32020/C25/C5x Parallel Interface

## AD7854/AD7854L to TMS320C30

Figure 41 shows a parallel interface between the AD7854/AD7854L and the TMS320C3X family of DSPs. The AD7854/AD7854L is interfaced to the Expansion Bus of the TMS320C3X. Two wait states are required in this interface. These can be programmed using the WTCNT bits of the Expansion Bus Control register (see *TMS320C3X Users guide* for details). Data from the AD7854/AD7854L can be read using the following instruction:

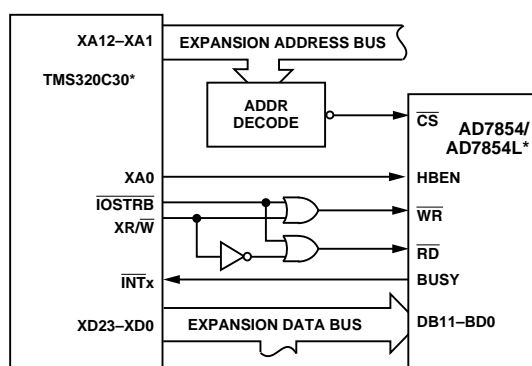
```
LDI *ARn,Rx
```

Data can be loaded into the AD7854/AD7854L using the instructions:

```
STI Ry,*ARn++
```

```
STI Rz,*ARn--
```

where *ARn* is an auxiliary register containing the lower 16 bits of the address of the AD7854/AD7854L in the TMS320C3X memory space, *Rx* is the register into which the ADC data is loaded during a load operation, *Ry* contains the 8 LSBs of data and *Rz* contains the 8 MSBs of data to be written to the AD7854/AD7854L.



\*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 41. AD7854/AD7854L to TMS320C30 Parallel interface

## AD7854/AD7854L to DSP5600X

Figure 42 shows a parallel interface between the AD7854/AD7854L and the DSP5600x series of DSPs. The AD7854/AD7854L should be mapped into the top 64 locations of Y data memory. If extra wait states are needed in this interface, they can be programmed using the Port A bus control register (please see *DSP5600x User's Manual* for details). Data can be read from the DSP5600x using the following instruction:

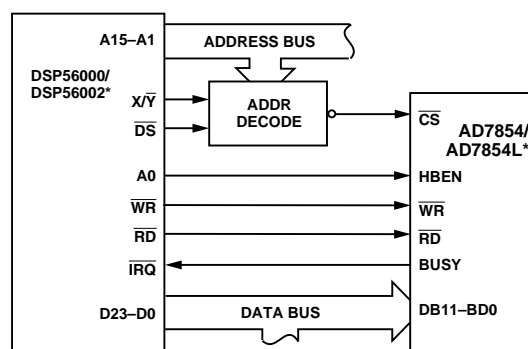
```
MOVE Y:ADCaddr, X0
```

Data can be written to the AD7854/AD7854L using the following two instructions:

```
MOVE X0, Y:ADCaddr
```

```
MOVE X1, Y:ADCaddr+1
```

Where *ADCaddr* is the address in the DSP5600X address space to which the AD7854/AD7854L has been mapped.



\*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 42. AD7854/AD7854L to DSP5600X Parallel Interface

# AD7854/AD7854L

## CONFIGURING THE AD7853/AD7853L

### AD7853/AD7853L as a Read-Only ADC

The AD7853/AD7853L contains fourteen on-chip registers which can be accessed via the serial interface. In the majority of applications it is not necessary to access all of these registers. Figure 23 outlines a flowchart of the sequence which is used to configure the AD7853/AD7853L as a Read-Only ADC. In this case there is no writing to the on-chip registers and only the conversion result data is read from the part. Interface Mode 1 cannot be used in this case as it is necessary to write to the control register to set Interface Mode 1. Here the CLKIN signal is applied directly after power-on, the CLKIN signal must be present to allow the part to perform a calibration. This automatic calibration is completed approximately 150 ms after power-on.

**APPLICATION HINTS****Grounding and Layout**

The analog and digital supplies of the AD7854/AD7854L are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The part has very good immunity to noise on the power supplies as can be seen by the PSRR versus frequency graph. However, care should still be taken with regard to grounding and layout.

The printed circuit board on which the AD7854/AD7854L is mounted should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined in one place. If the AD7854/AD7854L is the only device requiring an AGND to DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD7854/AD7854L. If the AD7854/AD7854L is in a system where multiple devices require AGND to DGND connections, the connection should still be made at one point only, a star ground point which should be established as close as possible to the AD7854/AD7854L.

Avoid running digital lines under the device as these couple noise onto the die. The analog ground plane should be allowed to run under the AD7854/AD7854L to avoid noise coupling. The power supply lines to the AD7854/AD7854L should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks and the data inputs should be shielded with digital ground to avoid radiating noise to other sections of the board and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with a 10  $\mu\text{F}$  tantalum capacitor in parallel with 0.1  $\mu\text{F}$  disc ceramic capacitor to AGND. All digital supplies should have a 0.1  $\mu\text{F}$  disc ceramic capacitor to DGND. To achieve the best performance from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. In systems where a common supply voltage is used to drive both the  $\text{AV}_{\text{DD}}$  and  $\text{DV}_{\text{DD}}$  of the AD7854/AD7854L, it is recommended that the system's  $\text{AV}_{\text{DD}}$  supply is used. In this case an optional 10  $\Omega$  resistor between the  $\text{AV}_{\text{DD}}$  pin and  $\text{DV}_{\text{DD}}$  pin can help to filter noise from digital circuitry. This supply should have the recommended analog supply decoupling capacitors between the  $\text{AV}_{\text{DD}}$  pin of the AD7854/AD7854L and AGND and the recommended digital supply decoupling capacitor between the  $\text{DV}_{\text{DD}}$  pin of the AD7854/AD7854L and DGND.

**Evaluating the AD7854/AD7854L Performance**

The recommended layout for the AD7854/AD7854L is outlined in the evaluation board for the AD7854/AD7854L. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the EVAL-CONTROL BOARD. The EVAL-CONTROL BOARD can be used in conjunction with the AD7854/AD7854L Evaluation board, as well as many other Analog Devices evaluation boards ending in the CB designator, to demonstrate/evaluate the ac and dc performance of the AD7854/AD7854L.

The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7854/AD7854L. It also gives full access to all the AD7854/AD7854L on-chip registers allowing for various calibration and power-down options to be programmed.

**AD785x Family**

All parts are 12 bits, 200 kSPS, 3.0 V to 5.5 V.

**AD7853 – Single Channel Serial****AD7854 – Single Channel Parallel****AD7858 – Eight Channel Serial****AD7859 – Eight Channel Parallel**



# AD7854/AD7854L

## PAGE INDEX

Topic	Page
FEATURES .....	1
GENERAL DESCRIPTION .....	1
PRODUCT HIGHLIGHTS .....	1
SPECIFICATIONS .....	2
TIMING SPECIFICATIONS .....	4
ABSOLUTE MAXIMUM RATINGS .....	5
ORDERING GUIDE .....	5
PINOUTS .....	5
TERMINOLOGY .....	6
PIN FUNCTION DESCRIPTION .....	7
AD7854/AD7854L ON-CHIP REGISTERS .....	8
Addressing the On-Chip Registers .....	8
Writing/Reading .....	8
CONTROL REGISTER .....	9
STATUS REGISTER .....	10
CALIBRATION REGISTERS .....	11
Addressing the Calibration Registers .....	11
Writing to/Reading from the Calibration Registers .....	11
Adjusting the Offset Calibration Register .....	12
Adjusting the Gain Calibration Registers .....	12
CIRCUIT INFORMATION .....	13
CONVERTER DETAILS .....	13
TYPICAL CONNECTION DIAGRAM .....	14
ANALOG INPUT .....	14
Acquisition Time .....	14
DC/AC Applications .....	14
Input Ranges .....	15
Transfer Functions .....	15
REFERENCE SECTION .....	16
AD7853/AD7853L PERFORMANCE CURVES .....	16
POWER-DOWN OPTIONS .....	17
POWER-UP/DOWN SEQUENCE .....	18
Writing to AD7854/AD7854L .....	18
Using Full and Partial Power-Down Combination .....	18
Full Power-Down or Partial Power-Down .....	19
CALIBRATION SECTION .....	20
Calibration Overview .....	20
Automatic Calibration on Power-On .....	20
Self-Calibration Description .....	21
Self-Calibration Timing .....	21
System Calibration Description .....	21
System Gain and Offset Interaction .....	22
System Calibration Timing .....	23
PARALLEL INTERFACE .....	24

Reading .....	24
Writing .....	25
Resetting the Parallel Interface .....	25
PARALLEL INTERFACING .....	26
AD7854/AD7854L to ADSP-21xx .....	26
AD7854/AD7854L to TMS32020, TMS320C25 and TMS320C5x .....	26
AD7854/AD7854L to TMS320C30 .....	26
AD7854/AD7854L to DSP5600x .....	27
CONFIGURING THE AD7853/AD7853L .....	28
AD7853/AD7853L as a Read-Only ADC .....	28
APPLICATIONS HINTS .....	29
Grounding and Layout .....	29
Evaluating the AD7854/AD7854L Performance .....	29
INDEX .....	30
OUTLINE DIMENSIONS .....	31

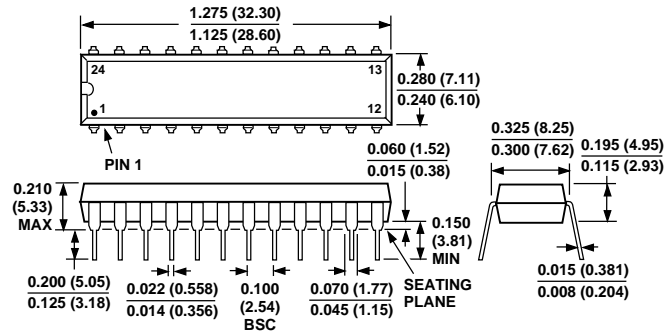
## TABLE INDEX

#	Title	Page
I	Write Register Addressing .....	8
II	Read Register Addressing .....	8
III	Calibration Selection .....	9
IV	Calibrating Register Addressing .....	11
V	Analog Input Connections .....	15
VI	Power Management Options .....	18
VII	Power-Up Times .....	18
VIII	Recommended Power-Down Modes for Lowest $I_{DD}$ ..	18
IX	Calibration Times .....	20

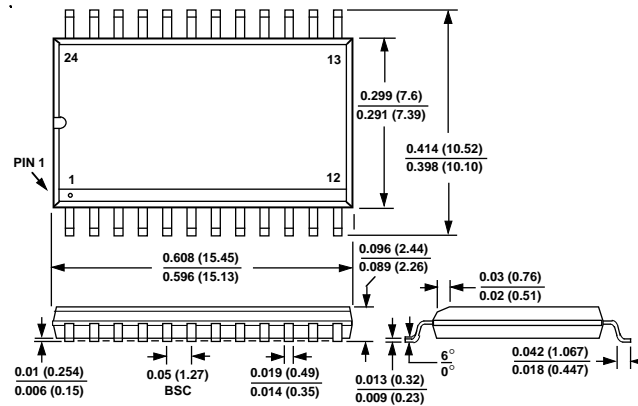
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 24-Pin Plastic DIP (N-24)

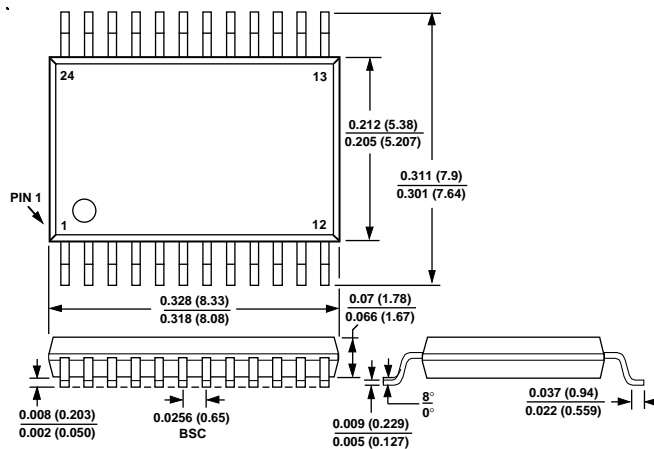


### 24-Pin Small Outline Package (R-24)



1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. SOIC LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

### 24-Pin Shrink Small Outline Package (RS-24)



1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

