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Application Note

User's Guide to the CDP1879 and CDP1879C1 CMOS Real-Time Clocks

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Introduction

The CDP1879 and CDP1879C1 Real-Time Clocks [1] are 24 pin devices, each consisting essentially of a long string of counters that supply standard clock time and date information in BCD format, Figure 1. In addition, the CDP1879 features an alarm circuit that activates the interrupt output pin and a separate clock output pin that provides a programmable square-wave output signal. Both the internal-alarm and clock-out signals can trigger the interrupt output pin, so that a status register is available to indicate the interrupt source. Users can supply a signal to the power-down pin that allows the interrupt-output pin level to control external power-down and wake-up circuits. Software generally required by other real-time clocks to prevent clock rollover is eliminated by a transparent "freeze" circuit that assures data integrity when accessing the clock. The clock's counters, plus a control register that regulates operation, are individually selectable using three address lines. Internal control signals governing read and write operations are selected through the IO/$\overline{MEM}$ pin, which places the device in a memory-mapped or I/O-mapped mode of operation.

The real time clocks were designed using Intersil PaCMOS standard-cell approach and are manufactured under a silicon-gate CMOS process. Both the CDP1879 and CDP1879C1 have guaranteed dc and dynamic parameters that allow operation at temperatures of -40^{o}C to +85^{o}C in a plastic package. In addition, both versions can operate in a ceramic package from -55^{o}C to 125^{o}C (see data sheet [1] for complete static and dynamic values).

The CDP1879 operates from a supply of 4V to 10.5V. It accepts a parallel resonant crystal or will keep time with an external clock source. Crystal frequencies are 1.048576MHz, 2.097152MHz, and 4.194304MHz. The CDP1879C1 is the lower voltage version with an operating voltage range of 4V to 6.5V. Like the CDP1879, it also operates with either an external clock source or at the same crystal frequencies. It can also run with a 32,768Hz crystal.

Interfacing - Hardware Considerations

I/O-Control and Device-Enable Pins

The real-time clocks, shown in block diagram form in Figure 1, are designed to interface directly to Intersil CDP1800-series processors (described briefly below). Therefore, pin labels on the clocks, Figure 2, match the pin names of these processors. Figure 3 indicates clock I/O control and direction pins; the functions of these pins are explained immediately below. Figure 4 is an I/O control and device-enabled schematic. Table 1 shows I/O pin connections.

TPA (Timing Pulse A) - TPA refers to a timing signal from the CDP1800-series processors that occurs early in the machine cycle, and that is used to latch the processor's multiplexed high-order address. In the real-time clock, this pin carries a strobe input used to latch the value of the CS pin. In memory-mapped operation, the pin may be tied high, requiring that CS be held for the duration of each read or write cycle. When the I/O-mapping mode is selected, this pin must be pulsed when the CS input is high.

CS (Chip Select) - The chip-select pin is an active high input that is used to enable the clock.

IO/$\overline{MEM}$ (I/O or Memory-Mode Select) - This pin is tied low to place the clock in the memory-mapped mode, and high when I/O operation is desired. Most processors will use the memory-mapped mode of operation.

$\overline{RD}$ (Read) - When the clock is in the memory-mapped mode, $\overline{RD}$ is an active low signal that enables data from the counters or status register to be placed on the data bus for the processor to read. When the clock is in the I/O mode, the read operation occurs when $\overline{RD}$ is high; a write operation occurs when $\overline{RD}$ is low and TPB/$\overline{WR}$ is high.

TPB/$\overline{WR}$ (Timing Pulse B/Write) - TPB refers to a timing signal from the CDP1800-series processors that appears late in each machine cycle and that is used to write data into accessed peripherals. When the clock is in the memory-mapped mode, TPB/$\overline{WR}$ is an active low signal used to write data into the clock's counters or control register. During I/O-mapping, a high level on this pin allows data latched on the trailing edge of the signal to be written into the counters or register.

CD1800-Series Interface

The clocks interface to CDP1800-series processors that use memory-mapping and I/O-mapping techniques to communicate with peripherals and memory. Memory-mapping implies address-line decoding to select memory locations and chip selects. With this technique, the real-time

clock's counters and registers are treated as memory locations. Read and write signals are active low. The CDP1800-series processors include three separate N-lines that are active during the 14 I/O instructions. These instructions are memory referenced so that data traveling in either direction is transferred between the peripherals and memory.

When I/O instructions are executed, the memory location is the reference for data transfer. Therefore, when an output instruction is performed (write cycle) the processor's $\overline{RD}$ line is activated and puts the data in memory onto the data bus. Late in the same cycle, the TPB from the processor is used to write data into the peripheral. An input instruction (read cycle) allows external data to be placed in memory. The processor's $\overline{WR}$ line is activated, and the data is written in.

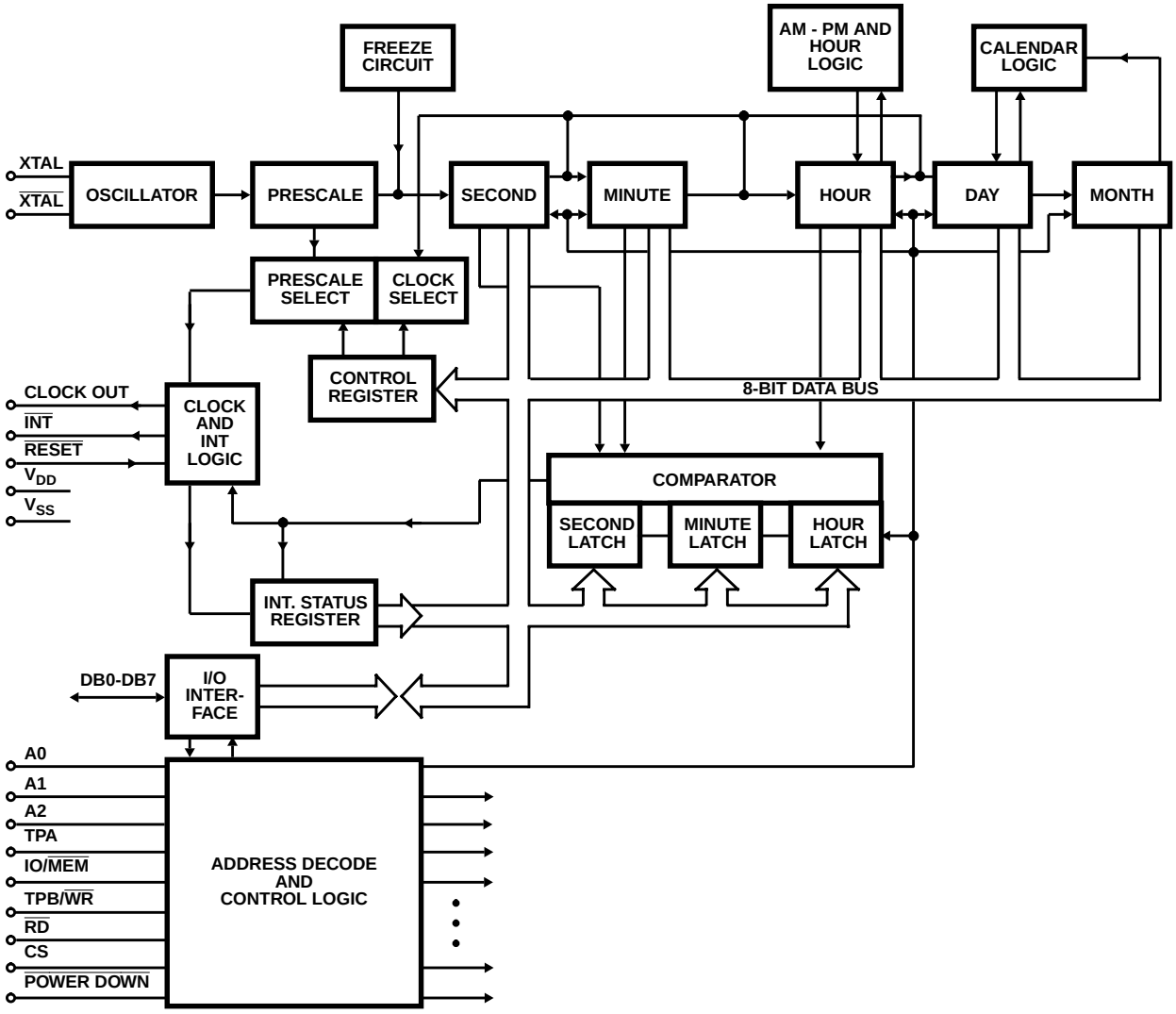


FIGURE 1. BLOCK DIAGRAM OF REAL-TIME CLOCK

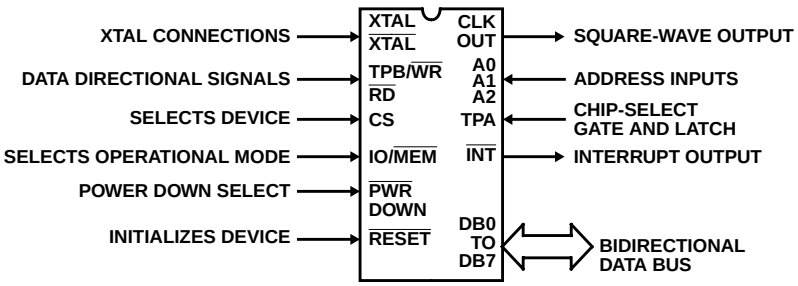


FIGURE 2. REAL-TIME-CLOCK PIN FUNCTIONS

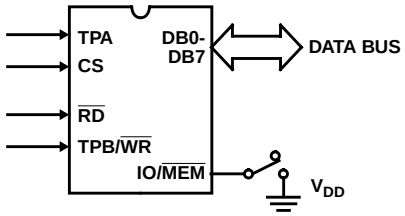


FIGURE 3. I/O CONTROL AND DIRECTION PINS

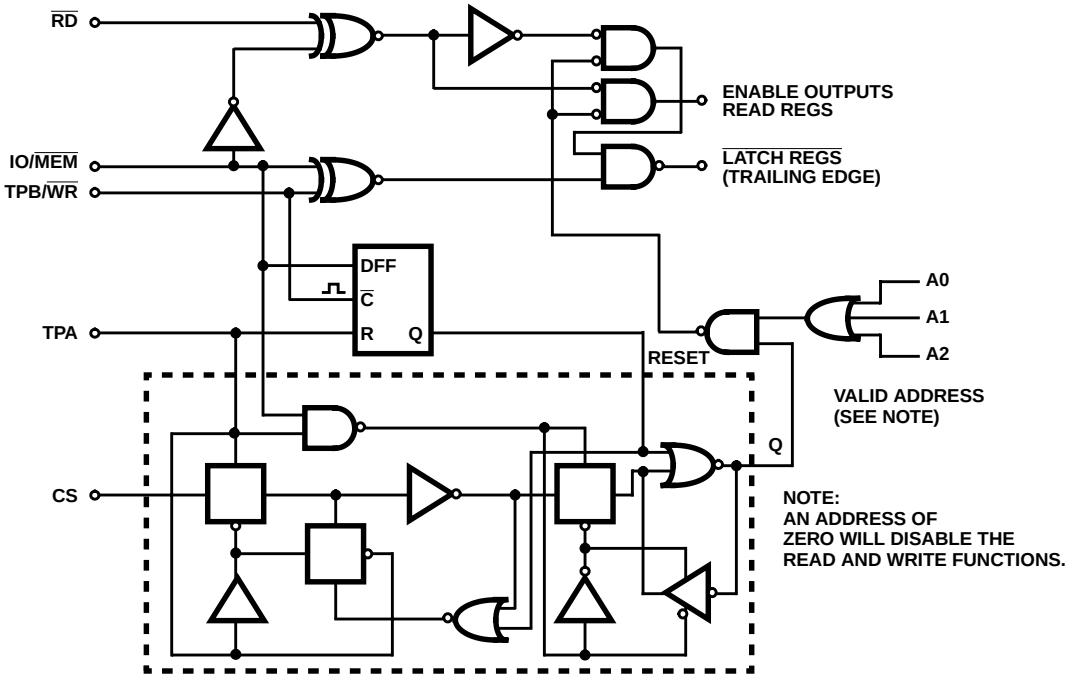


FIGURE 4. I/O CONTROL AND DEVICE ENABLE SCHEMATIC

TABLE 1. I/O PIN CONNECTIONS

PROCESSOR	CDP1879 PIN					
	TPA	CS	$\overline{RD}$	TPB/$\overline{WR}$	IO/$\overline{MEM}$	A0-A2
Intersil CDP1800-Series (Memory-Mapped)	TPA (Note 1)	Hi or Decoded Address	$\overline{MRD}$	$\overline{MWR}$	V_{SS}	MA0, MA1, MA2
Intersil CDP1800-Series (I/O mapped)	TPA	N or Decoded N Lines	$\overline{MRD}$	TPB	V_{DD}	N0, N1, N2
CDP6805	AS	Hi or Decoded Address	R/$\overline{W}$	DS	V_{DD}	B0 (Note 2), B1, B2
Zilog Corp. Z-80™	V_{DD}	Hi or Decoded Address	$\overline{RD}$	$\overline{WR}$	V_{SS}	A0, A1, A2
8085/NSC800	ALE (Note 1)	Hi or Decoded Address	$\overline{RD}$	$\overline{WR}$	V_{SS}	AD0 (Note 2), AD1, AD2

NOTES:

1. May be connected to V_{DD} when CS is externally latched.
2. Latch externally.

Z-80™ is a Trademark of Zilog Corporation.

Figure 5 shows a typical memory-mapped interface utilizing the CDP1802. This interface places the clock and counter-timer in selectable 4k memory blocks. Figure 6 shows the interface of the clock to an 8085 processor, Figure 7 the interface to a CDP6805, and Figure 8 the interface to a Zilog Corporation Z-80.

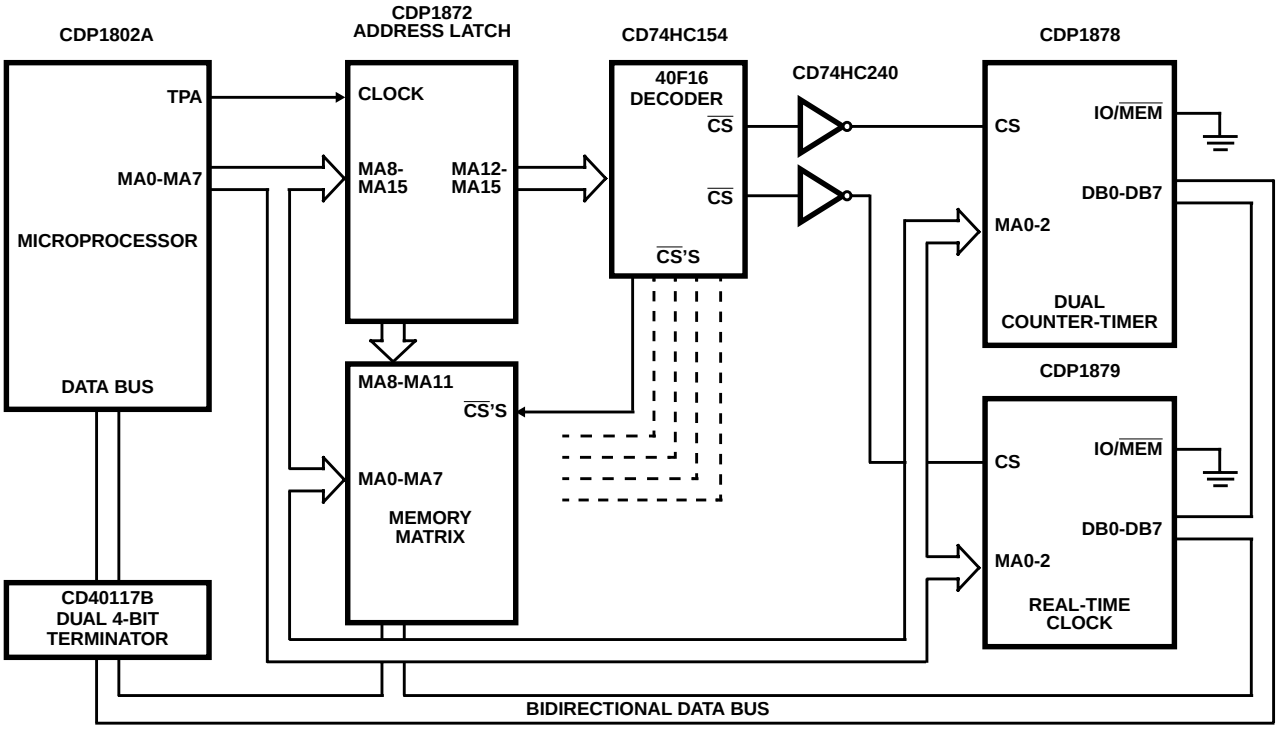


FIGURE 5. REAL-TIME CLOCK AND COUNTER-TIMER IN MEMORY-MAPPED INTERFACE

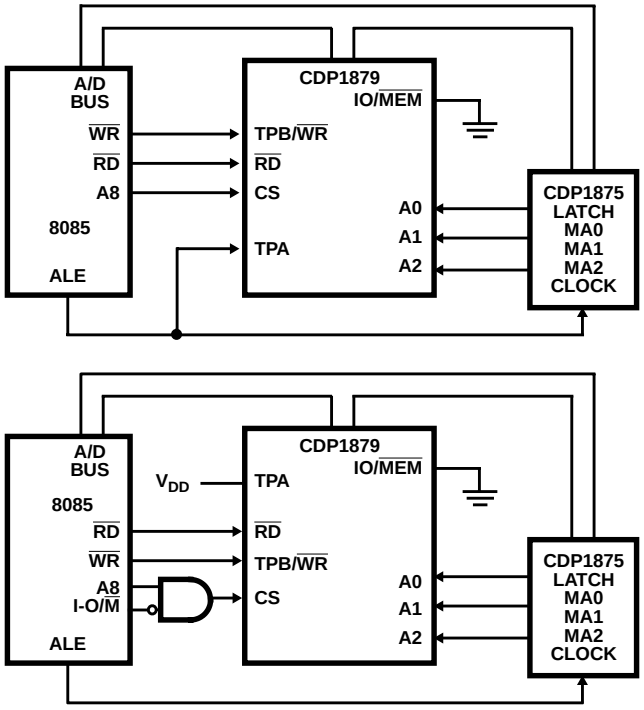


FIGURE 6A. MEMORY-MAPPED INTERFACE

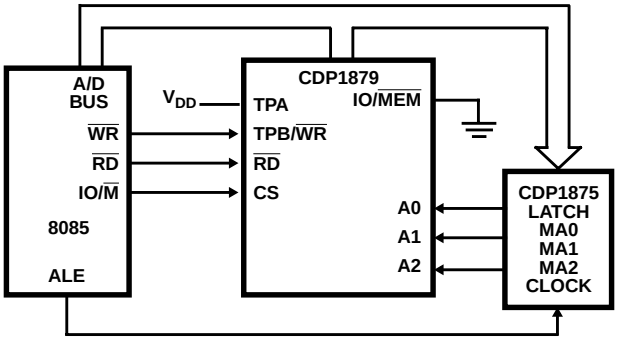


FIGURE 6B. I/O-MAPPED INTERFACE

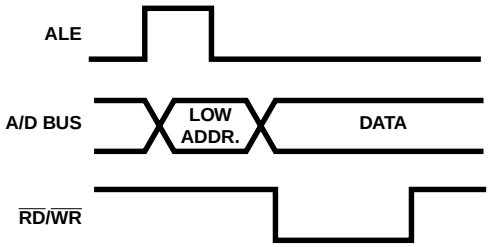


FIGURE 6C. TIMING CYCLES

FIGURE 6. 8085 INTERFACE AND TIMING

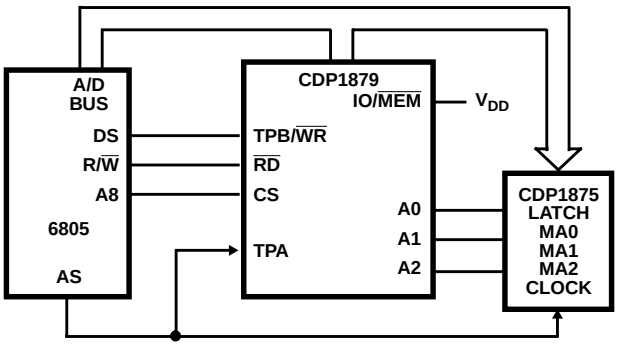


FIGURE 7A. CDP6805 I/O-MAPPED INTERFACE

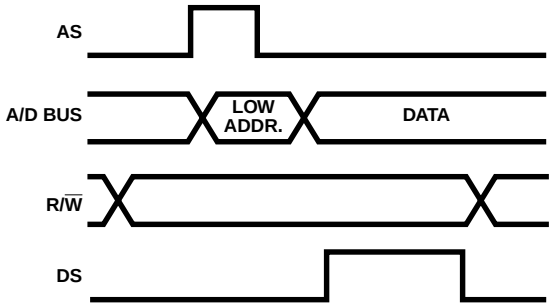


FIGURE 7B. TIMING DIAGRAM

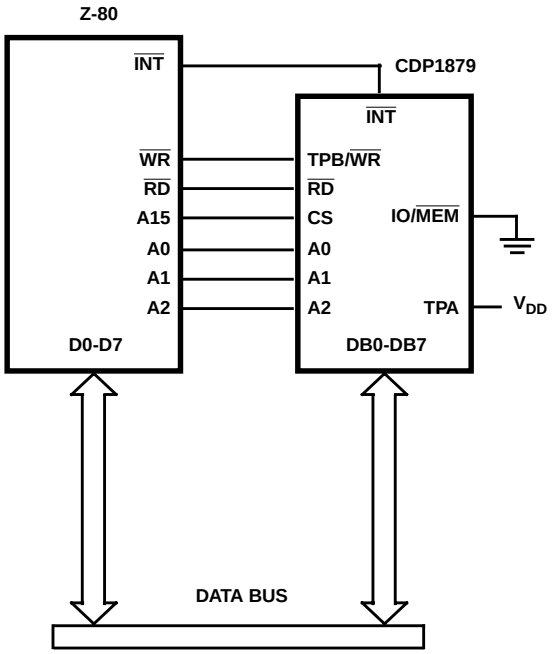


FIGURE 8. ZILOG CORPORATION Z-80 INTERFACE TO THE CDP1879

Timing Considerations

Figures 9 and 10 show read and write-cycle timing wave forms, respectively. The read and write limits shown must be observed to successfully access the clock. Three of the characteristics, hold after read and write, and read access time, may represent critical limit values when the clock is interfaced to processors operating at their maximum frequency limit.

TABLE 2. READ-CYCLE TIMING CHARACTERISTICS

READ CYCLE TIMES (NOTE 1)		**LIMITS (ns)**	
		MINIMUM (NOTE 2)	**MAXIMUM**
Data Access from Address	t_{DA}	-	400
Read Pulse Width	t_{RD}	270	-
Data Access from Read	t_{DR}	-	375
Address Hold After Read	t_{RH}	0	-
Output Hold After Read	t_{DH}	50	230
Chip Select Setup to TPA	t_{CS}	50	-

NOTES:
1. Characteristics at T_A = -40°C to +85°C; V_{DD} = 5V ±5%; Input t_R, t_F = 10ns; C_L = 50pF and 1 TTL load.
2. Time required by a limit device to allow for the indicated function.

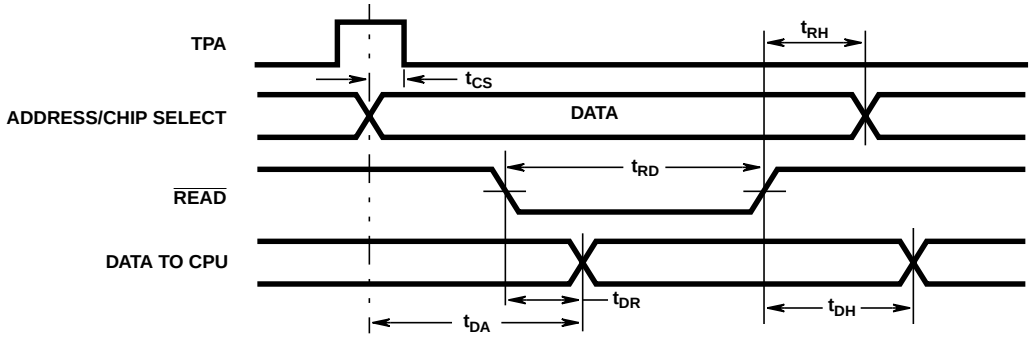


FIGURE 9. READ-CYCLE TIMING WAVEFORMS

TABLE 3. WRITE-CYCLE TIMING CHARACTERISTICS

WRITE CYCLE TIMES (NOTE 1)		**LIMITS (ns)**	
		MINIMUM (NOTE 2)	**MAXIMUM**
Address Setup to Write	t_{AS}	225	-
Write Pulse Width	t_{WR}	150	-
Data Setup to Write	t_{DS}	65	-
Address Hold After Write	t_{AH}	0	-
Data Hold After Write	t_{WH}	150	-
Chip Select Setup to TPA	t_{CS}	50	-

NOTES:
1. Characteristics at T_A = -40°C to +85°C; V_{DD} = 5V ±5%; Input t_R, t_F = 10ns; C_L = 50pF and 1 TTL load.
2. Time required by a limit device to allow for the indicated function.

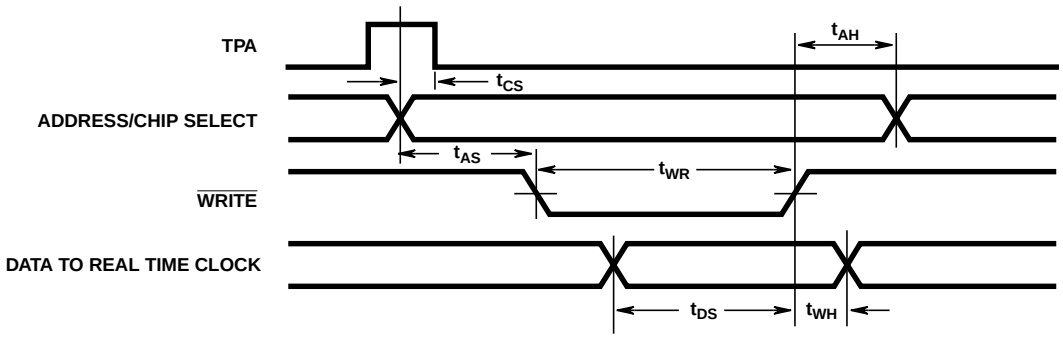


FIGURE 10. WRITE-CYCLE TIMING WAVEFORMS

Output Hold After Read (t_{DH})

When multiplexed bus processors, in which address and data share the same pins, are interfaced to the clock, the output-hold-after-read parameter (230ns) may cause bus contention. As an example, at 5MHz, the CDP6805 requires data to be off the bus within 160ns after data strobe. The 8085A operating with a 6MHz crystal requires 150ns after read. Since the clock may hold data for 230ns, bus contention may occur if these processors are interfaced to the clock at their maximum operating frequencies.

Data Hold After Write (t_{WH})

The real-time clocks require that data be held after the trailing edge of the write pulse for 150ns. Neither the 8085/NSC800, Z-80, nor CDP6805 meet this requirement at their maximum operating frequencies.

Data Access From Read (t_{DR})

The clock will supply data a maximum of 375ns from the leading edge of the read pulse. The data setup requirements for processors operating at their maximum frequencies may require faster access.

Hold and Access-Time Solutions

All of the above parameters are frequency dependent. Often, simply lowering the frequency when accessing the clock will solve any timing problems. Access times can be extended by inserting wait states. Write and read-hold-time problems are more difficult to correct; glue parts, such as latches and buffers, are required to meet the requirements of these timing parameters.

Interfacing - Software Considerations

Programming Model

Figure 11 illustrates the counters, alarm latches, and registers that must be accessed to write in and read out time and date information. The functions are selected through internal decoding of three address lines. Table 4 contains the register access codes for different combinations of address inputs. Figure 12, a programming model of the same registers, shows their read and/or write availability. These address lines and data lines, in conjunction with the I/O control pins, constitute the interface to the clock.

When the clock is configured for memory-mapped operation, it can be considered as six memory locations that reside in an area of memory determined by the definitive decoding of the upper address bits. The clock's I/O-mapped mode utilizes the N-lines (I/O lines) and I/O instructions of the CDP1800-series processor. The processor's N-lines are decoded for use as a chip select, and in a two-level scheme, are also used as the address input signals.

When other processors are interfaced to the clock, the clock will generally be placed in its memory-mapped mode. An exception is interface with the CDP6805, where the clock is usually wired for I/O operation.

Writing to and reading from the clock is as straightforward as accessing memory. Software considerations regarding clock rollover (when the one-second clock may pulse the counters during read or write cycles) are eliminated by utilizing the freeze circuit (described below), which requires only one additional instruction. Use of the freeze circuit eliminates the software burden of looking for a signal or register bit that guarantees valid data. A write cycle with address 1 and don't -care data before any series of counter accesses (read or write cycles) assures that the one-second clock has been held and will not interfere with accesses for 250ms.

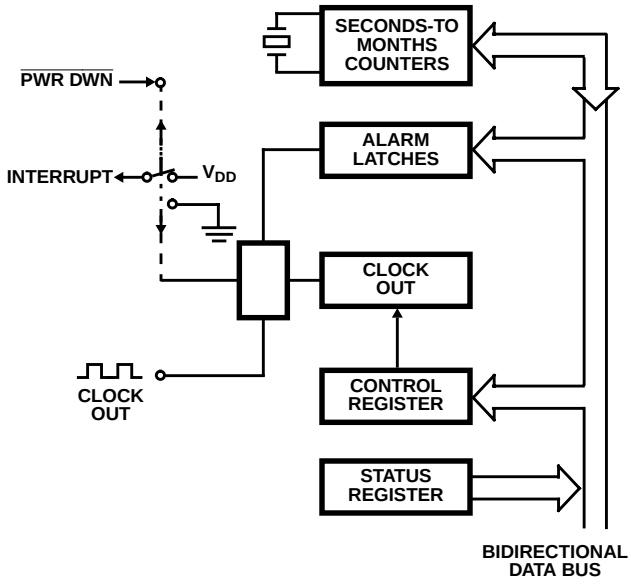


FIGURE 11. FUNCTIONS THAT MUST BE ACCESSED TO WRITE IN AND READ OUT TIME AND DATE INFORMATION

Freeze Circuit

The freeze circuit is designed to allow the user easy access to the real-time clock without the fear that clock rollover will cause erroneous time data. Clock rollover problems occur during counter reads while the asynchronous one-second clock input to the counter-divider chain is rippling through the counters.

As an example in Figure 13A, the one-second clock is about to set the time to 0 seconds, 0 minutes and 3 hours. A read is performed, and the hours counter indicates 2 hours. But before the second and minute counters are read, the one-second clock ripples through them, with the result that the counters hold the time shown in Figure 13B. When the seconds and minutes counters are read (Figure 13B), their values are correct, but the hours time, read before the ripple, is 1 hour off. It is apparent that this type of error can be a substantial problem, particularly if the date and month counters are involved.

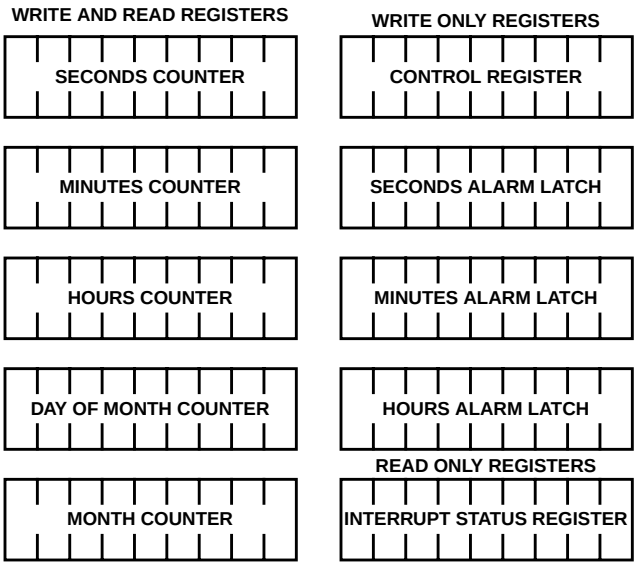


FIGURE 12. PROGRAMMER'S MODEL OF THE REGISTERS OF FIGURE 11

Operation

The counter-series string is clocked by the negative transition of the one-second clock. This clock transition must pass through the freeze circuit before toggling the counter-series string, as shown in Figure 14. The freeze circuit creates a "window" 250ms wide shown as time (A) in Figure 15. If the counter reads or writes (for addresses other than address 7) are performed during this window, the clock transition is held and is not allowed through the freeze circuit until time (C) Figure 15, when the transition is inserted into the counter series string. If counter accesses are initiated just before the one-second-clock transition, the clock would toggle the counters 250ms later. Therefore, a requirement when using the real-time clocks is to finish operations within 250ms of the initial access.

If the clock is accessed during time (A), Figure 15, and then accessed again at time (C), when the counter is allowed to toggle, ripple problems would occur. To preclude this problem, a second window is created by the freeze circuit during time (B). This window will allow a write to address 1 to immediately reset the freeze circuit and clock the counters. Subsequent accesses to the real-time clock will occur well after the clock has rippled through the counters.

If read or write operations are performed during time periods other than (A) or (B), the freeze circuit is not functional.

Figure 16 shows a simplified freeze circuit (a), and the sequence of freeze-circuit operation (b).

TABLE 4. REGISTER TRUTH TABLE

ADDRESS			ACTIVE SIGNAL		BIT 3 CONTROL REGISTER	REGISTER OPERATION
A2	A1	A0	TPB/$\overline{WR}$	RD		
0	1	0	X		0	Write Seconds Counter
0	1	0		X	0	Read Seconds Counter
0	1	1	X		0	Write Minutes Counter
0	1	1		X	0	Read Minutes Counter
1	0	0	X		0	Write Hours Counter
1	0	0		X	0	Read Hours Counter
1	0	1	X		0	Write Date Counter
1	0	1		X	0	Read Date Counter
1	1	0	X		0	Write Month Counter
1	1	0		X	0	Read Month Counter
0	1	0	X		1	Write Seconds Alarm Latch
0	1	1	X		1	Write Minutes Alarm Latch
1	0	0	X		1	Write Hours Alarm Latch
1	1	1	X			Write Control Register
1	1	1		X		Read Int. Status Register

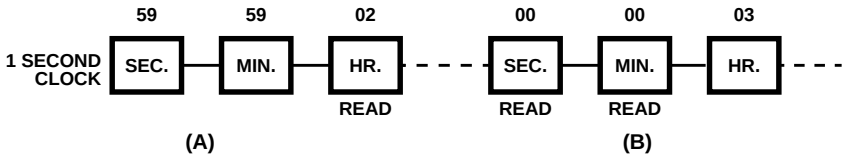


FIGURE 13. FREEZE-CIRCUIT READ EXAMPLE

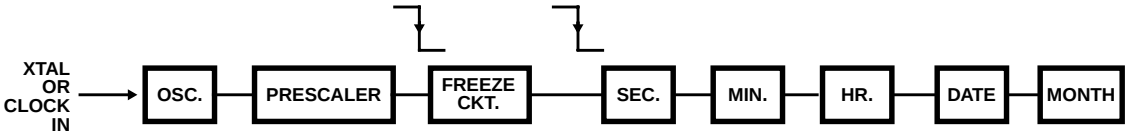


FIGURE 14. COUNTER SERIES STRING

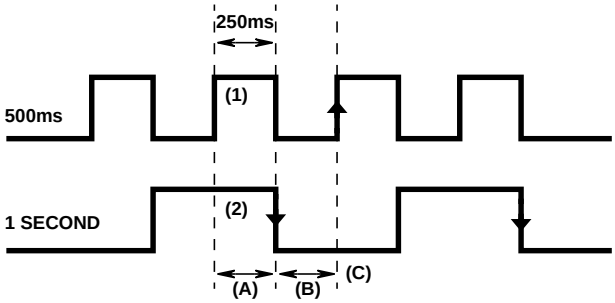


FIGURE 15. FREEZE-CIRCUIT TIMING WAVEFORMS

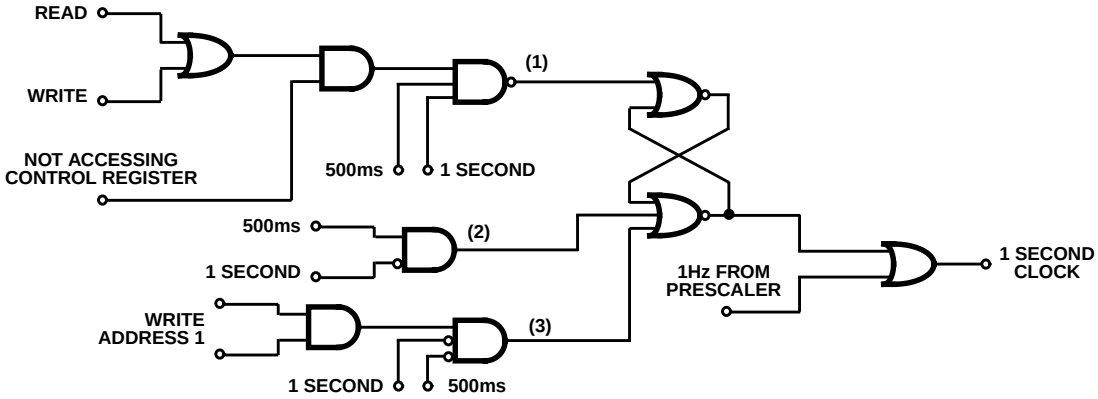


FIGURE 16. (A) SIMPLIFIED FREEZE CIRCUIT, AND (B) FREEZE-CIRCUIT OPERATION

NOTES:

1. Set freeze during time period A, (one second clock is held high)
2. Reset freeze at time period C,
3. or during time period B if address 1 is present during a write cycle.

Restrictions on Accuracy

The data sheet for the real-time clock states that when the seconds counter is written to, the last 7 stages of the prescaler are reset, resulting in a 10ms accuracy. Normally, the seconds counter will be clocked 1 second from the time of the write to the seconds counter. However, if the freeze circuit has been activated, this sequence may not occur, therefore, to assure the 10ms accuracy, the following procedure should be used:

1. Write to seconds counter - don't care data - address 2
2. Dummy write - don't care data - address 1
3. Write to seconds counter - valid data - address 2

The mild restrictions on accesses to the real-time clock require no additional software or hardware considerations to assure data integrity. In all other known clocks, software solutions to clock rollover problems range from reading and comparing the time data twice to sampling register values. Hardware solutions vary between stopping any internal clock updates to monitoring output-pin transitions. The addition of an address 1 write operation preceding accesses to the CDP1879 real-time clock in conjunction with the requirements to finish accesses in 250ms will guarantee stable and accurate time data.

Register Descriptions

The real-time clock contains a control register to configure its operation, and a status register to identify interrupts, five registers or counters to hold the time from seconds to months, and three additional registers that are referred to as alarm latches, which hold the alarm time.

Control Register

The control register is a write-only register that shares the same address as the status register, address 7. A brief explanation of the functions of the eight bits in the control register are shown in Figure 17; more detail is given in the paragraphs that follow.

Bits 0 and 1 - Frequency Select - The logic levels in bits 0 and 1 are decoded and used to select the appropriate input to the last 14 stages of the prescaler chain, Figure 18. Their selection must match the crystal or external clock source used to drive the oscillator selection of the real-time clock.

Bit 2 - Start/Stop - As shown in Figure 18, a 1 in bit 2 enables the input to last through 14 stages of the prescaler chain. A zero in this position inhibits counting.

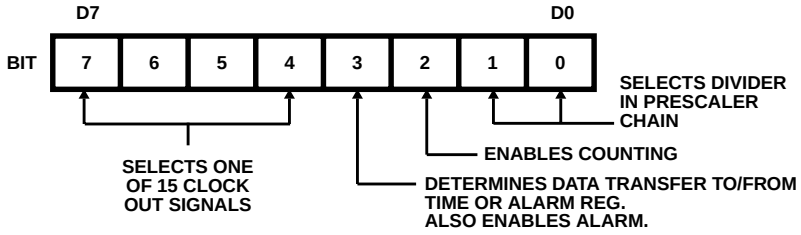
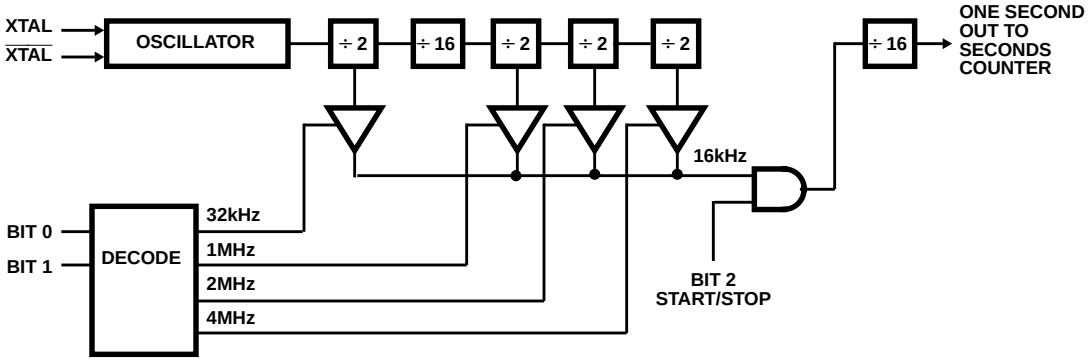


FIGURE 17. CONTROL REGISTER



BIT 0	BIT 1		BIT 2	
0	0	32,768Hz	0	Stop Counter
1	0	1.048576MHz	1	Start Counter
0	1	2.097152MHz		
1	1	4.194304MHz		

FIGURE 18. FREQUENCY-SELECT OPERATION

Bit 3 - Counter/Latch Control - Figure 19 is a simplified diagram of the counter/alarm latch access. Bit 3 has two functions. First, if set to zero, it directs written data to the time counters. If set to 1, data is written into the alarm latches. This bit function is necessary because the time counters and their comparable alarm latches have the same addresses. The second function of bit 3 is to enable the alarm-out signal. An alarm signal (interrupt output low and bit 7 set in the status register) will only appear if this bit (bit 3) is a logic 1.

Bits 4, 5, 6 and 7 - Clock Select - Figure 20 is a block diagram of the clock-out select function; Figure 21 is a table of clock-out selections. Bits 4, 5, 6, and 7 are decoded, and enable the required prescaler or time counter output to toggle the clock-out pin.

Status Register

The status register, Figure 22, is used to indicate the interrupt source. Bits 0 through 5 are held low. Bit 6 high indicates that a programmed negative clock-out transition has occurred, and bit 7 high identifies the alarm circuit as the interrupt source. These bits are reset by an external reset or by writing to the control register. Note, in Figure 23, the delay of approximately 30ms before the alarm signal sets bit 7.

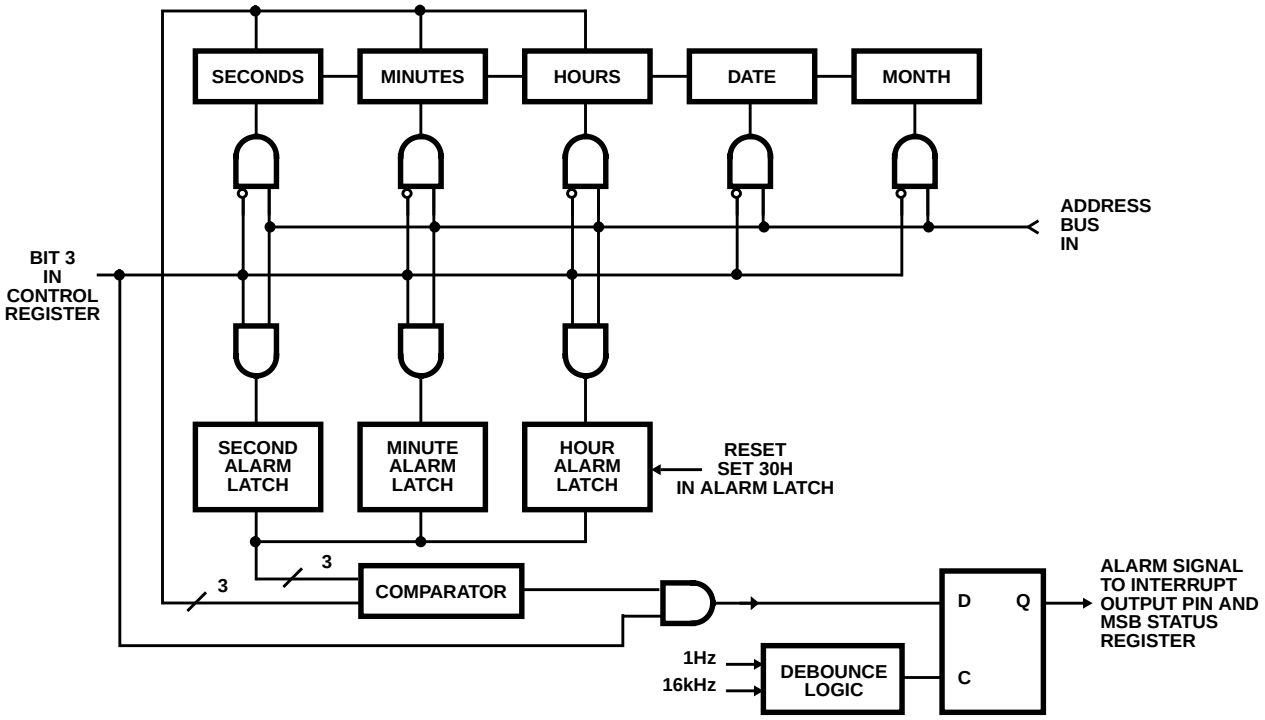


FIGURE 19. SIMPLIFIED DIAGRAM OF COUNTER/ALARM LATCH ACCESS

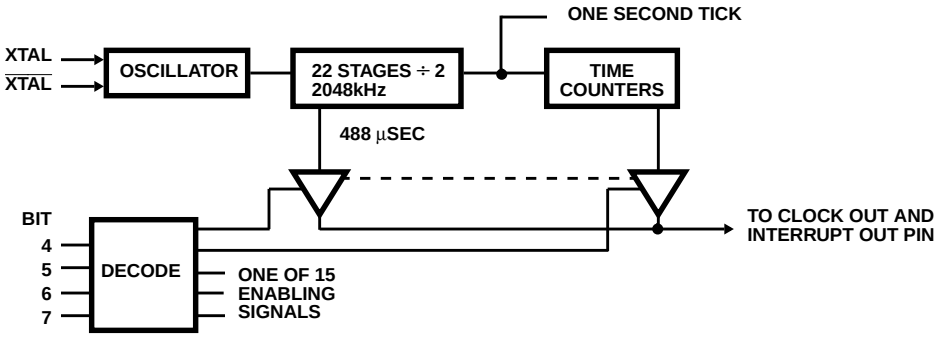
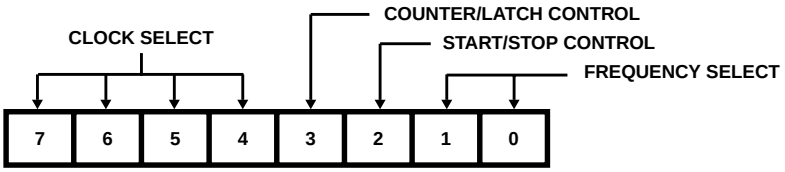


FIGURE 20. BLOCK DIAGRAM, CLOCK-OUT SELECT



BIT 7	6	5	4	FREQUENCY	CLOCK-OUT WAVEFORM (1 OF 15)
0	0	0	0	Deselect	
0	0	0	1	488.2µs	
0	0	1	0	976.5µs	
0	0	1	1	1953.1µs	
0	1	0	0	3906.2µs	
0	1	0	1	7812.5µs	
0	1	1	0	15.625ms	
0	1	1	1	31.25ms	
1	0	0	0	62.5ms	
1	0	0	1	125.0ms	
1	0	1	0	250.0ms	
1	0	1	1	500.0ms	
1	1	0	0	Second	
1	1	0	1	Minute	
1	1	1	0	Hour	
1	1	1	1	Day	

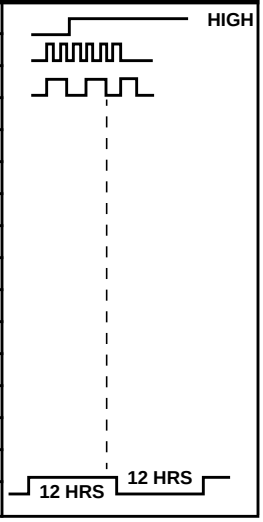


FIGURE 21. CLOCK-OUT SELECTIONS

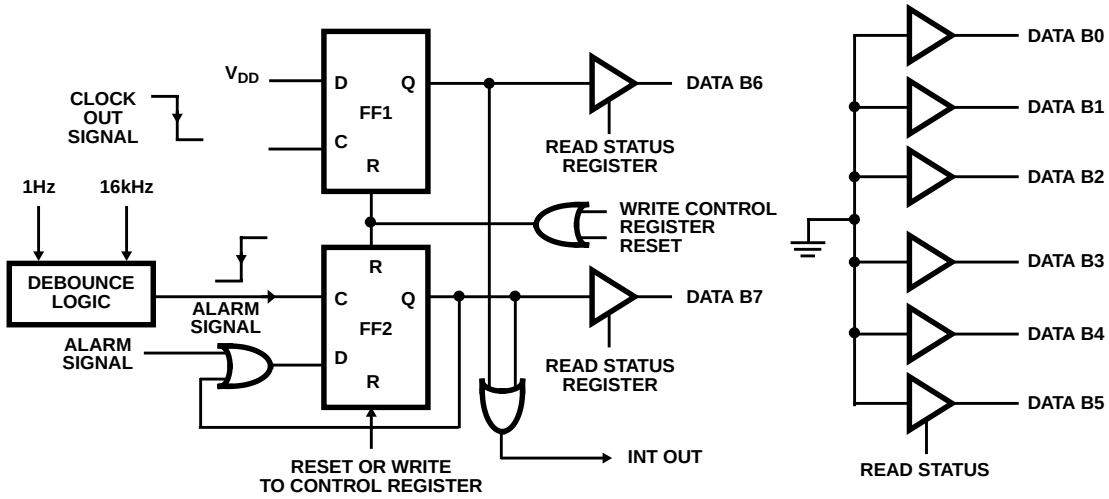


FIGURE 22. STATUS REGISTER

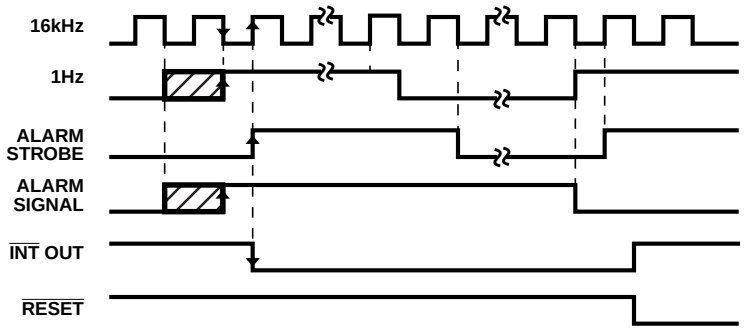


FIGURE 23. DEBOUNCE WAVEFORMS

Operating Sequence

Although accessing of the clock is similar to accessing of memory, certain procedures should be followed when writing the data to assure correct operation.

The control register is accessed first to set the operating characteristics and to direct subsequent accesses to the counters or alarm latches. The upper nibble of the control-register byte selects one of 15 square-wave output signals that appear at the clock-out pin. If a clock-out is selected before the time counters are accessed and loaded, an inadvertent interrupt may be generated. To preclude this occurrence when the interrupt signal is utilized, the upper nibble of the control register byte is set to zero during the initial control-register write cycle. The time counters and/or alarm latches are then loaded. The control register is then written to again, and the value in the upper nibble selects the required clock.

Data Format Required (BCD)

1. Seconds and Minutes counters and alarm latches 00 to 59
2. Hours counter: 01 to 12 for AM/PM
   00 to 23 for 24-hour time

   Bit 7: 0 = AM, 1 = PM

   Bit 6: 0 = 24 hour, 1 = 12 hour

   Hour alarm latch: 01 to 12 for AM/PM, 00 to 23 for 24 hour.

   12 hour (AM/PM): Bit 7: 0 = AM, 1 = PM

   If the time counter is set for 24-hour time, bit 7 is don't care.
3. Day-of-month counter: 01 to 28, 29, 30 or 31.
4. Month counter: Jan. = 1, Dec. = 12

   Bit 7: 0 = No leap year, 1 = leap year

Setting the Time

The time counters, from seconds to months, are accessed and written into using the procedure described below. Data entered is in BCD format. For example, 12 seconds in the seconds counter would be represented as 00010010. The hours counter, however, utilizes its upper bits for AM/PM designation and 12/24-hour selection. Moreover, bit 7 in the months counter is set by the user to indicate leap year. All of these bits must be set as required in addition to the BCD hour and month information. For example, if 4 PM is written to the hours counter, a BCD code of 00000100 for the hours plus a 1 in bits 6 and 7 to enable PM and 12-hour operation would require a data byte of 11000100 (Hex C4).

Procedure to Set the Time

1. Chip selected and address 7 present on the address lines to access the control register.
2. Write to control register with the required data byte. Bit 3 must be set to zero.
3. Use addresses 2 to 6 to access seconds-to-months counters, in any order, and load appropriate data byte. (BCD data plus bits 6 and 7 in hours counter and bit 7 in month counter.)
4. Writing to the seconds counter resets the last 7 stages of the prescaler, thereby setting an accuracy of 10ms.

Setting the Alarm

Figure 24 shows the alarm logic. As previously described, bit 3 in the control register must be a 1 to direct subsequent data to the alarm latches. A comparator circuit compares the time and alarm latch seconds, minutes, and hour outputs. When this comparison is true and bit 3 in the control register is set to 1, an alarm is generated that activates the interrupt-out pin and sets bit 7 in the status register to a high logic level. The two most significant bits in the hours time counter are used for an AM/PM indication (User set for AM or PM with subsequent toggling every 12 hours) and to set 12/24-hour operation.

If bit 6, the 12/24-hour control bit, is set to zero (24-hours), a match of bit 7 (AM/PM) between the hours time counter and alarm latch is not required to generate a true comparison.

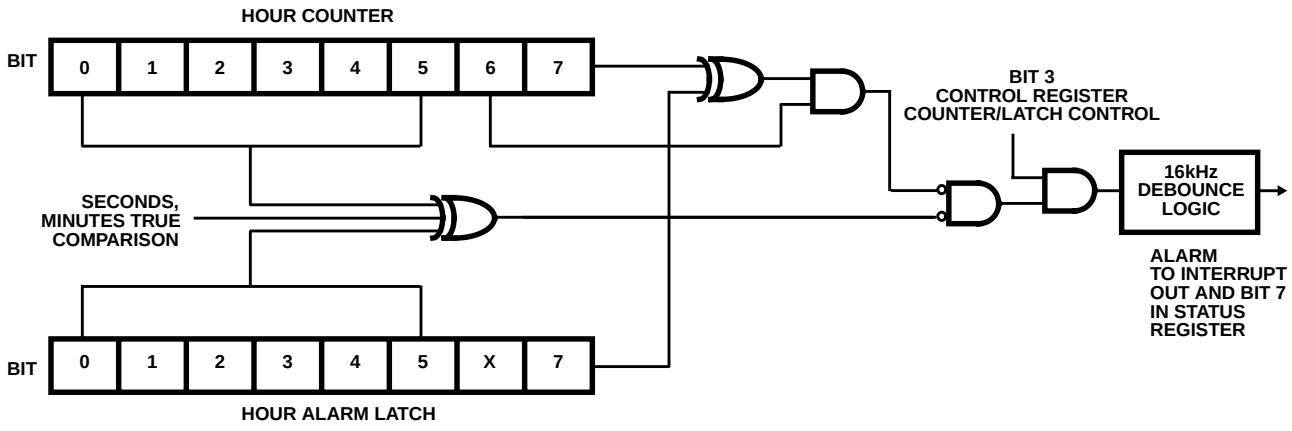


FIGURE 24. ALARM LOGIC

When an alarm occurs, there is a delay of 30µs before the alarm bit is set in the status register. The interrupt-out pin signal is also delayed for this period. Additionally, if a clock out was selected that also activates the interrupt-out in coincidence with the alarm-out signal (for example, clock-out set for one second and any alarm-time set), the status register will indicate a clock-out transition (bit 6 = 1) 30µs before bit 7 is set to 1 in the status register.

Resetting the Interrupt-Out Signal and Status Register

There are two methods of resetting the interrupt-out signal and status register once an alarm or clock-out transition has occurred.

Reset Pin (Schmitt Input)

A low on the reset pin will accomplish the following:

1. Set the interrupt-out pin high.
2. Clear the status register.
3. Place 30 Hex in the hour alarm latch. This entry will prevent an inadvertent interrupt when programming the time.

Control Register Write

Writing to the control register sets the interrupt-out high and clears the status register.

Power-Down Operation

Figure 25 shows power-down input-control logic. A low on the power-down pin (Schmitt input) activates the real-time-clock's power-down function. This function is enabled at the trailing edge of a read or write signal and, therefore, power down will not occur until the read or write cycle is concluded.

When power down is activated, the following events occur:

1. Read and write control signals are disabled.
2. The data bus is placed in an input condition and logic transitions are ignored. (Therefore, the bus must be terminated.)
3. The clock-out signal is set low.
4. The interrupt-out pin is three-stated.

The clock continues to keep time and there is no appreciable change in operating power. The interrupt output will go low if an alarm or clock transition (internal clock transition) occurs after power down has been initiated. An application using the power-down feature to control a microprocessor's clock signal is illustrated in Figure 26. This application is especially appealing in a CMOS circuit design where only quiescent current will be drawn when the processor's clock input is disabled.

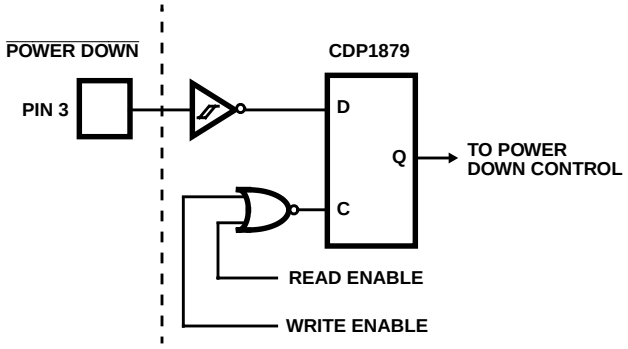


FIGURE 25. POWER-DOWN INPUT-CONTROL LOGIC

In an operational sequence utilizing the circuitry of Figure 26, the serial Q output of the CPU is activated after the clock is configured with an alarm time. The oscillator then stops and the device enters the power-down mode. When the alarm activates and the $\overline{INT}$ output is set low, the CPU resets and polls the $\overline{EF1}$ flag to determine whether a cold or warm start routine is in order. The control register is then written to, an event that resets the interrupt requests.

Any general-purpose microprocessor can utilize the low operating power of the real-time clock. Typical operating current with a crystal-controlled oscillator at 32kHz and 5V is 100µA, and at 4MHz, 600µA. The trade-off between high frequency and accuracy and low-frequency operation with lower power consumption must be resolved by the user. The ease of programming and the features offered by the real-time clock aid the designer and lower the level of programmed support required.

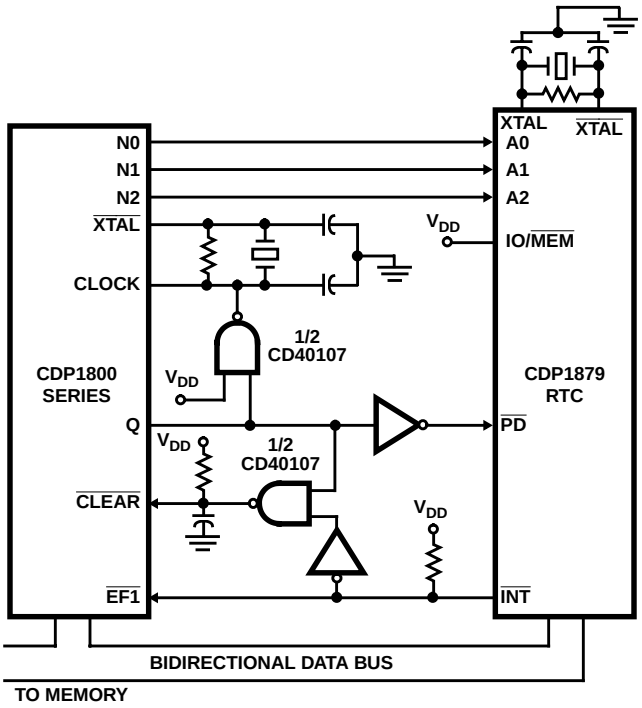


FIGURE 26. APPLICATION OF REAL-TIME CLOCK THAT USES POWER-DOWN FEATURE TO CONTROL A MICROPROCESSOR'S CLOCK SIGNAL

Power Considerations

The CDP1879 power requirements are shown in Table 5. The values listed are maximum limits with a V_{DD} of ±5% and a temperature range of -40°C to 85°C.

Table 6 shows output drive capabilities under the same conditions. All inputs must meet CMOS requirements with a minimum high of 3.5V and a maximum low of 1.5V at a V_{DD} of 5V.

Standby Operation (Low Voltage)

When utilizing an external crystal with its on-board oscillator as the frequency source, the CDP1879 and CDP1879C1 can operate at a supply voltage no lower than 4 volts. However, if a 32kHz external frequency source is provided at the XTAL input pin, the clock can operate in a standby mode down to 2.5V at 0 to 70°C, and 3V at -40°C to +85°C. Figure 27 shows the typical minimum standby voltage. Figure 28 shows that the real-time clock must be disabled by CS (chip-select signal) a minimum of 2µs before reaching the standby voltage level, and enabled again after the same period of time when the voltage is raised again.

When the clock is in the standby mode, it functions only as a timekeeping device; all read/write data accesses are disallowed.

TABLE 5. POWER REQUIREMENTS OF THE REAL-TIME CLOCK

MODE	INPUT FREQUENCY	POWER-SUPPLY VOLTAGE		UNITS
		5V	10V	
Operating Current with Crystal Oscillator	(NOTE 1) 32kHz	0.25	-	mA
	1MHz	0.5	3.0	mA
	2MHz	0.6	3.5	mA
	4MHz	0.8	5.0	mA
Operating Current with External Clock Source	32kHz	0.15	0.25	mA
	1MHz	1.0	2.0	mA
	2MHz	1.5	3.0	mA
	4MHz	2.0	4.5	mA

NOTE:

1. CDP1879C1 Only

TABLE 6. OUTPUT DRIVE CAPABILITIES

POWER-SUPPLY VOLTAGE	5V	10V	UNITS
Data-Bus and Interrupt-Out Drive (Sink)	1.8	3.6	mA
Data-Bus and Interrupt-Out Drive (Source)	-1.10	-2.6	mA
Clock Out (Sink)	0.6	1.2	mA
Clock Out (Source)	-1.1	-2.6	mA

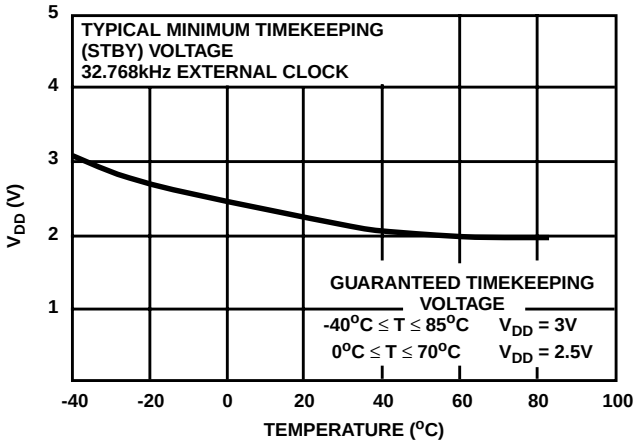


FIGURE 27. TYPICAL MINIMUM STANDBY VOLTAGE

Oscillator Operation

The CDP1879 operates with a crystal connected to its XTAL and $\overline{XTAL}$ inputs, or accepts an external clock source at its XTAL input that has a rise and fall time of less that 10µs. Typical oscillator parameters are listed in Table 8; suggested circuits are described in Figures 29 through 32.

TABLE 7. STANDBY-VOLTAGE CHARACTERISTICS

PARAMETER	V_{DD}	V (STBY)	CDP1879		CDP1879C1		UNITS
			MIN	MAX	MIN	MAX	
Chip Deselect to Stby Voltage Time, $t_{C(STBY)}$	5	2.5, 3	2	-	2	-	µs
	10	2.5, 3	1	-	-	-	µs
Recovery to Normal Operation Time, t_{RC}	5	2.5, 3	2	-	2	-	µs
	10	2.5, 3	1	-	-	-	µs

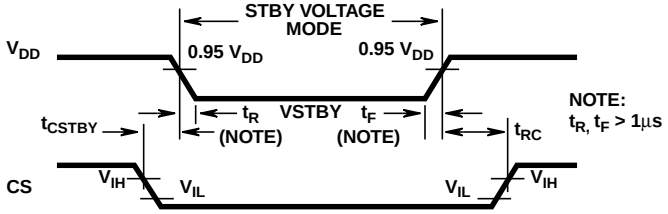


FIGURE 28. WAVEFORMS AND TIMING DIAGRAM

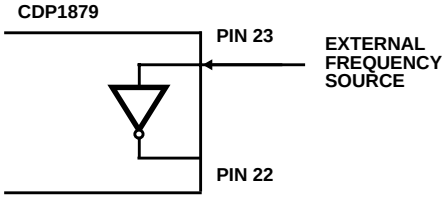


FIGURE 29. CONNECTIONS FOR CDP1879 WHEN AN EXTERNAL FREQUENCY SIGNAL IS SUPPLIED

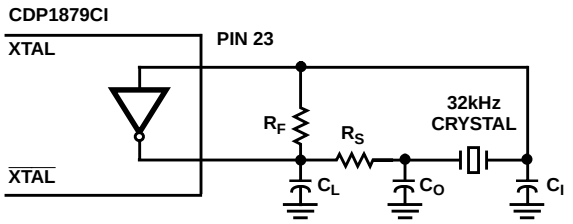


FIGURE 30. SUGGESTED OSCILLATOR CIRCUIT FOR 32kHz CRYSTAL OPERATION

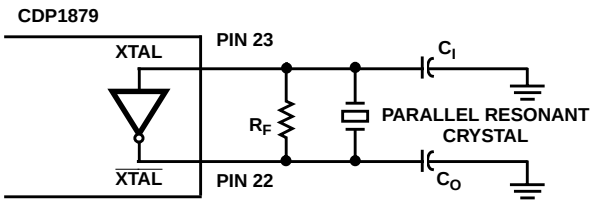


FIGURE 31. SUGGESTED OSCILLATOR CIRCUIT FOR 1, 2, OR 4MHz OPERATION

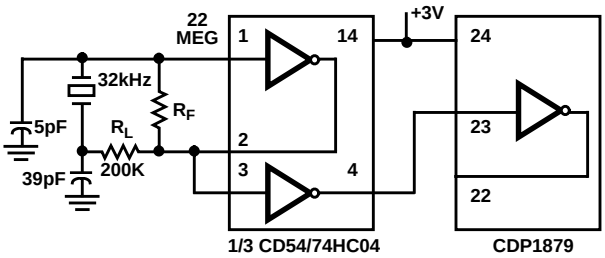


FIGURE 32. TYPICAL EXTERNAL-CLOCK-SOURCE DIAGRAM

Design Considerations for a Stable Crystal Oscillator

1. Stray capacitance should be minimized for best oscillator performance. Circuit-board traces connected to the oscillator pins should be kept to a maximum of 1 inch, and there should be no parallel traces.
2. A signal or power-source line must not cross or approach the oscillator-circuit line.
3. It is advisable to put a nonelectrolytic 0.1µF capacitor between V_{DD} and V_{SS} of the CDP1879.

Real-Time-Clock System

Figure 33 illustrates a working system in which the CDP1879 is configured for I/O operation to display time in minutes and hours. Figure 34 shows the real-time-clock flowchart. A CDP1802 processor outputs instructions and data in a two-level device-selection scheme. An output instruction of OUT 1 (Hex 61) activates the processors N lines, and is decoded by the CDP1873C to provide a chip-select signal to the CDP1875C output port. The data present on the data bus during the output instruction is latched in the CDP1875C and provides the chip-select signal for the clock or the CD22105A LCD driver.

If no other OUT 1 instruction with different bus data is issued by the processor, the device will remain selected. Subsequent output and input instructions will then address the clock, if it is selected, to read or write to its registers. When the LCD driver is selected, the processor's OUT 2 instructions load the driver with the display information.

The backplane signal from the LCD driver is input to one of the processor's flag lines, and is sampled to flash the colon by placing the colon input, via the processor's Q line, in or out of phase with the backplane signal. The CDP1879's clock-out signal is set for one second, and drives the processor's interrupt to turn the display colon off. A routine in the main program turns the colon on when the interrupt is not present.

A sample program that illustrates the CDP1879's clock-out signal and alarm capability is listed in Figure 35. The alarm routine is written to flash eights when the alarm activates. The clock will continue to keep time and will display it along with the alarm display.

Reference

For Intersil documents available on the web, see
http://www.intersil.com/
Intersil AnswerFAX (407) 724-7800

[1] *CDP1879, CDP1879C-1 Data sheet,* Intersil Corporation, AnswerFAX Doc No. 1360

TABLE 8. TYPICAL OSCILLATOR-CIRCUIT PARAMETERS FOR SUGGESTED OSCILLATOR CIRCUITS

PARAMETER	OSCILLATOR FREQUENCY				UNITS
	4.197MHz	2.097MHz	1.049MHz	(NOTE 1) 32768Hz	
R_F	22	22	22	22	MΩ
C_O	39	39	39	39	pF
C_I	5	5	5	5	pF
R_S	-	-	-	200	kΩ
C_L	-	-	-	91	pF
Crystal Impedance	73	200	200	50K (max)	Ω

NOTE:

1. CDP1879C1 Only

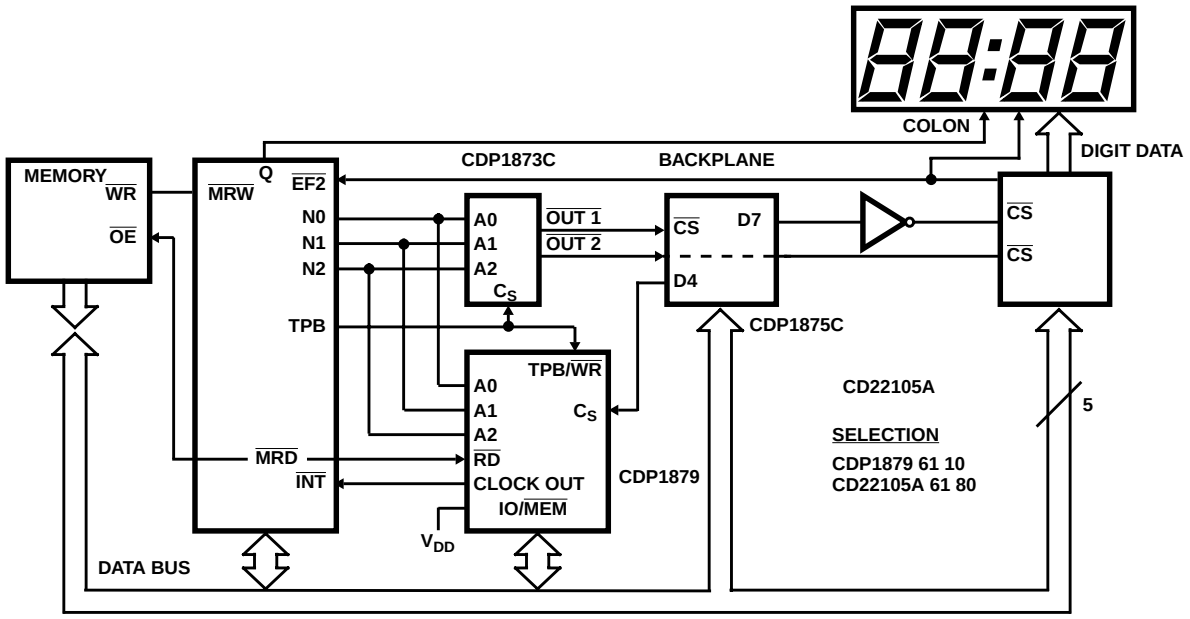


FIGURE 33. REAL-TIME CLOCK SYSTEM

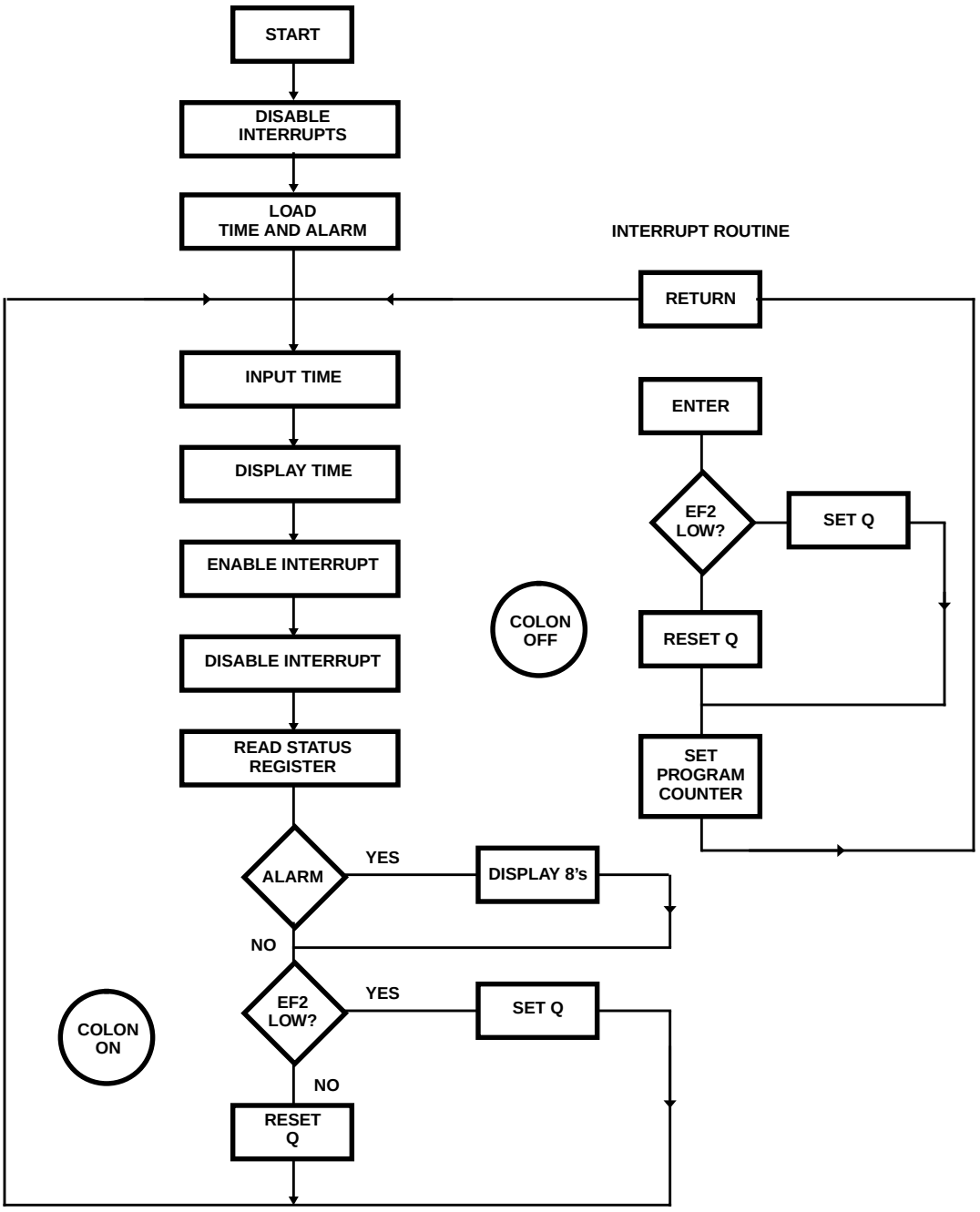


FIGURE 34. REAL-TIME-CLOCK FLOWCHART

```
        ... PROGRAM DISPLAYS 8:30 A.M. AND FLASHES
        ... 8'S AND TIME WHEN ALARM ACTIVATES
        ... AT 8:31:10.
        ... INTERRUPT ON PROCESSOR CONNECTS TO 1 SEC.
        ... CLOCK OUT ON CDP1879. EF2 CONNECTS TO
        ... BACKPLANE SIGNAL ON LCD DRIVER.
        ... INTERRUPT ROUTINE IS USED TO TURN COLON OFF
        ... BY SAMPLING EF2 AND TOGGLING Q.
        ... TWO LEVEL I/O IS USED FOR SELECTION
        ... CLOCK IS SELECTED WITH 61 10.
        ... LCD DRIVER IS SELECTED WITH 61 80.
        ... AND 62 INSTRUCTIONS LOAD DRIVER AFTER SELECTION.
        DIS; DC00H
        LDI A.1 (ENTER); PHI R1          ... SET INTERRUPT POINTER
        LDI A.0 (ENTER); PLO R1
        OUT 1; DC 010H                   ... SELECT CLOCK
        OUT 7; DC 003H                   ... LOAD C.R.
        OUT 2; DC 000H                   ... ZERO SECONDS
        OUT 3; DC 030H                   ... 30 MINUTES
        OUT 4; DC 048H                   ... 8 A.M.
        OUT 7; DC 00BH                   ... SELECT ALARM LATCH
        OUT 2; DC 010H                   ... 10 SEC. ALARM
        OUT 3; DC 031H                   ... 31 MIN. ALARM
        OUT 4; DC 048H                   ... 8 A.M. ALARM
        OUT 7; DC 0CFH                   ... ONE SEC. CLOCK
                                         ... ALARM ACTIVATES 1 MIN.
                                         ... 10 SEC. AFTER START
INPUT   SEX 0; OUT1; DC 010H             ... SELECT CLOCK
        LDI A.1 (MIN); PHI R8
        LDI A.0 (MIN); PLO R8
        SEX 8
        INP 3; PLO R7                    ... INP MINUTES
        ANI 0FH                          ... MASK UPPER
        STXD; GLO R7                     ... STR LOW MIN.
        ANI 0F0H                         ... MASK LOWER
        SHR; SHR; SHR; SHR
        ADI 010H; STXD                   ... ADD CHAR. POS.
        INP 4; PLO R7                    ... INPUT HOURS
        ANI 0FH                          ... MASK UPPER
        ADI 020H; STXD                   ... ADD CHAR. POS
        GLO R7; ANI 030H                 ... MASK 6 BITS
        BNZ HR                           ... CHECK FOR 0 HRS
        LDI 03FH; STR R8                 ... STR BLANK HRS
        BR OUT

HR      SHR; SHR; SHR; SHR
        ADI 030H                         ... ADD CHAR. POS.
        STR R8
OUT     SEX 0
        OUT 1; DC 080H                   ... SELECT LCD DRIVER
        SEX 8
        OUT 2; OUT 2; OUT 2; OUT 2       ... LOAD DRIVER
        SEX 0
        RET; DC 00H                      ... ENABLE INT TO SAMPLE CLOCK OUT
        DIS; DC 00H                      ... DISABLE INT
        OUT 1; DC 010H
        SEX 8
        INP 7; XRI 0C0H                  ... READ STATUS REG
        BX ALARM                         ... FOR ALARM
CHK     B2 ON                            ... COLON ON
        REQ; BR INPUT
ON      SEQ
        BR INPUT                         ... REPEAT
ALARM   LDI A.1 (MIN); PHI R8
        LDI A.0 (MIN); PLO R8
        LDI 008H; STXD                   ... LEAD 8'S INTO
        LDI 018H; STXD                   ... LCD DRIVER
        LDI 028H; STXD
        LDI 038H; STR R8
        SEX 0; OUT 1; DE 080H; SEX 8
        OUT 2; OUT 2; OUT 2; OUT 2
        BR CHK
BACK    SEP R0                           ... RETURN MAIN
ENTER   B2 OFF                           ... ENTER POINT FOR
        SEQ                              ... INTERRUPT ROUTINE
        BR SET                           ... COLON OFF
OFF     REQ
SET     LDI A.1 (INPUT); PHI R0          ... RESET P.C.
        LDI A.0 (INPUT); PLO R0
        BR BACK
HOURS   DS 3
MIN     DS 1
```

FIGURE 35. REAL-TIME-CLOCK PROGRAM