The CDP1871A Keyboard Encoder

Application Note | March 1997 | AN7374.2

Introduction

The CDP1871A Keyboard Encoder [1] interfaces directly between a CDP1800-series (or other) processor and a mechanical keyboard array. It services up to 53 ASCII-coded keys and up to 32 Hex-coded keys. This note describes the encoder's operation, explains its dynamic electrical characteristics, and features those factors that will affect device operation when the encoder is used with a non-1800-series processor.

Operation

The CDP1871A is made up of two major sections: the counter/scan-selection logic and the control logic. Figure 1 shows a block diagram of the device, Figure 2 the terminal diagram, and Figure 3 the control schematic; the Appendix contains operational information as well as recommended operating conditions and electrical characteristics.

The counter and scan-selection logic scans the keyboard array using the drive lines (D1 - D11) and the sense lines (S1 - S8). The outputs of the internal five stage scan counter are conditionally encoded by the ALPHA, SHIFT, and CONTROL inputs, Appendix Table A-1, and are used to drive the D1 - D11 output lines high, one at a time. Each D1 - D11 output may drive up to eight keys, which are sampled by the sense-line inputs (S1 - S8). The S1 - S8 inputs are enabled by the internal three stage scan counter.

The control logic interfaces with the CDP1800-series I/O and timing signals to establish timing and status conditions for the CDP1871A.

The TPB input clocks the scan counters, and is also used to reset the data available output ($\overline{DA}$). When a valid keydown condition is detected on a sense line, the control logic inhibits the clock to the scan counters on the next low-to-high transition of TPB, and the $\overline{DA}$ output is set low. The scan-counter outputs (C1 - C8) represent the ASCII and HEX key codes (Appendix Table A-2), and are used to drive the BUS 0 - BUS 7 outputs, which interface directly to the CDP1800-series data bus.

The BUS 0 - BUS 7 outputs, which are normally three-stated, are enabled by decoding the CS inputs during a CPU input instruction. The low-to-high transition of TPB during the input instruction resets the $\overline{DA}$ output high. Once the $\overline{DA}$ output has been reset, it cannot go low again until the present key is released and a new keydown condition is detected. (This arrangement prevents unwanted repeated keycode outputs, which may be caused by fast software routines.)

After the depressed key is released and the debounce delay (determined by R_X, C_X) has occurred, the scan clock inhibit is removed, allowing the scan counters to advance on the following high-to-low transitions of TPB. This condition provides an N-key lockout feature, which prevents the entry of erroneous codes when two or more keys are pressed simultaneously. The first key pressed in the scanning order is recognized, while all other keys pressed are ignored until the first key is released and read by the CPU, at which time the next key pressed in the scanning order is detected.

If the first key remains closed after the CPU reads the data and resets the $\overline{DA}$ output (on the low-to-high transition of the TPB), an auxiliary signal ($\overline{RPT}$) is generated. This signal is available to the CPU, and indicates an auto-repeat condition. The $\overline{RPT}$ output is reset high at the end of the debounce delay after the depressed key is released.

The debounce input (pin 36) provides a terminal connection for an external user-selected RC circuit designed to eliminate detection of a keydown condition caused by keyboard noise. The operation of the debounce circuit is explained below with the aid of Figures 1 and 3.

When a valid keydown is detected, the on chip active-resistor device (R_N) is enabled, and the external capacitor (C_X) is discharged, providing a key closure debounce time of approximately R_NC_X. The discharge of C_X is sensed by the Schmitt trigger inverter, which clocks the $\overline{DA}$ flip-flop (latching the $\overline{DA}$ output low and inhibiting the scan clock). (The $\overline{DA}$ flip-flop is reset by the low-to-high transition of TPB when the CS inputs are enabled.)

When a valid key release is detected, R_N is disabled and C_X begins charging through the external resistor (R_X), providing a key release debounce time of approximately R_XC_X. The change in charge is, again, sensed by the Schmitt trigger inverter, enabling the scan clock to continue on the next high-to-low transitions of TPB, after the current keycode data is read by the CPU.

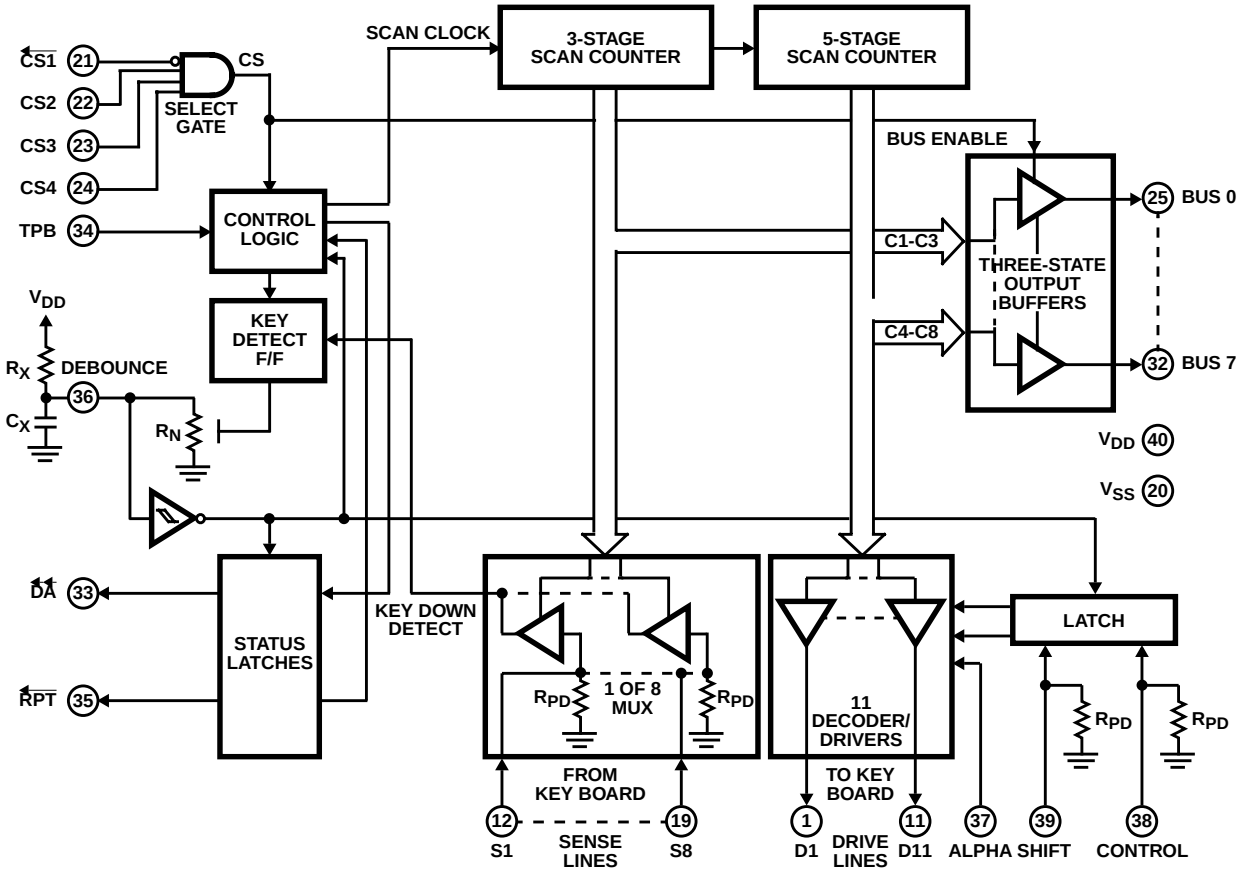

FIGURE 1. BLOCK DIAGRAM OF THE CDP1871A KEYBOARD ENCODER

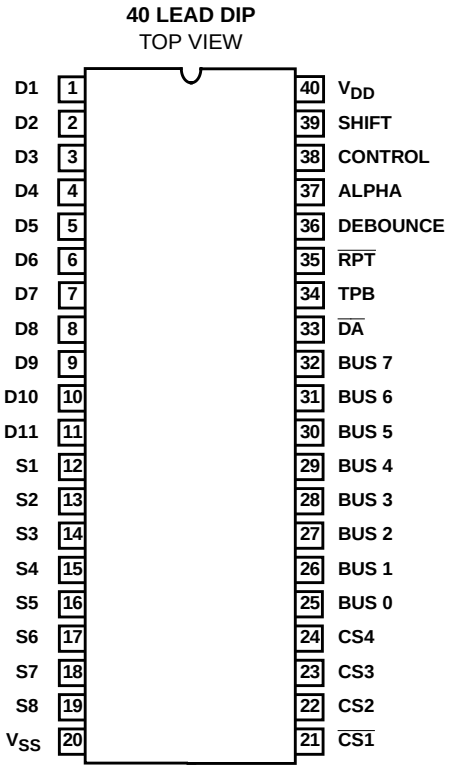

FIGURE 2. TERMINAL DIAGRAM

Functions of Terminals

D1 - D11 (Outputs)

Drive lines for the 11 x 8 keyboard switch matrix. These outputs are connected through the external switch matrix to the sense lines (S1 - S8).

S1 - S8 (Inputs)

Sense lines for the 11 x 8 keyboard matrix. These inputs have internal pull-down resistors, and are driven high by the drive line when a keyboard switch is closed.

$\overline{CS1}$, CS2, CS3, CS4 (Inputs)

Chip-select inputs, which are used to enable the tristate data bus outputs (BUS 0 - BUS 7), and to enable the resetting of the status flag ($\overline{DA}$) on the low-to-high transition of TPB. These four inputs are normally connected to the N-lines (N0 - N2) and $\overline{MRD}$ output of the CDP1800-series microprocessor.

BUS 0 - BUS 7 (Outputs)

Tristate data bus outputs that provide the ASCII and HEX codes of the detected keys. The outputs are normally connected to the BUS 0 - BUS 7 terminals of the CDP1800-series microprocessor.

$\overline{DA}$ (Output)

The data available output flag, which is set low when a valid key closure is detected. It is reset high by the low-to-high transition of TPB when data is read from the CDP1871A. This output is normally connected to a flag input ($\overline{EF1}$ - $\overline{EF4}$) of the CDP1800-series microprocessor.

TPB (Input)

The input clock used to drive the scan generator and reset the status flag ($\overline{DA}$). This input is normally connected to the TPB output of the CDP1800-series microprocessor.

RPT (Output)

The repeat-output flag used to indicate that a key is still closed after data has been read from the CDP1871A ($\overline{DA}$ high). It remains low as long as the key is closed, and is used for an autorepeat function, under CPU control. This output is normally connected to a flag input (EF1 - EF4) of the CDP1800-series microprocessor.

Debounce (Input)

This input is connected to the junction of an external resistor to V_{DD} and an external capacitor to V_{SS}. It provides a debounce time delay (t = RC) after the release of a key. The external pull-up resistor is required under all circumstances.

Alpha, Shift, Control (Inputs)

A high on the shift or control input will be internally latched (after the debounce time), and the drive and sense line decoding will be modified as shown in Appendix Table A-1. These inputs are normally connected to the keyboard, but produce no code by themselves. The shift and control inputs have internal pull-down resistors to simplify use with momentary-contact switches. The alpha input is not latched and is designed to provide an alpha-lock function when used with a standard SPDT switch. When alpha = 1, the drive and sense line decoding will be modified as shown in Appendix Table A-1.

V_{DD}, V_{SS}

V_{DD} is the positive supply voltage input. V_{SS} is the most negative supply voltage terminal, and is normally connected to ground. All outputs swing from V_{SS} to V_{DD}. The recommended input-voltage swing is also from V_{SS} to V_{DD}.

Figure 4 shows a CDP1800-series processor operating in its I/O mapped mode with the keyboard encoder. CDP1800-series processors have fourteen I/O instructions and three dedicated output lines (N0 - N2) that are used for I/O functions. The N lines are toggled when the I/O instructions are used; otherwise, they remain at a low level.

Unlike memory-mapping, when the processor outputs and inputs data, the memory is the source of the system data when the input or output instructions are executed.

For example, an input instruction writes data to the memory and the processor; therefore, the read line remains high while the write line goes low. An output instruction outputs data from the memory. In this case, the read line goes low and the write line remains high.

An important input to the encoder is the TPB signal. This timing signal occurs at the end of the machine cycle of a CDP1800-series processor and is used to clock the encoder's scan counter. It also resets the data available signal when the encoder is selected. It is synchronous in that it must not toggle when the chip is selected and data is being read from the encoder.

The TPB signal is used to strobe data into a peripheral. Note in Figure 4 that the read line is used in addition to the N lines to select the encode; therefore, the only time the encoder will drive the data bus is when the proper input instruction is executed. The encoder is not selected until the N lines are at the required levels and the read line is high. When a key closure is detected by the CDP1871A, the data available signal is activated; the processor is alerted by sensing its EF flag input. The processor then performs an input instruction to capture the key data.

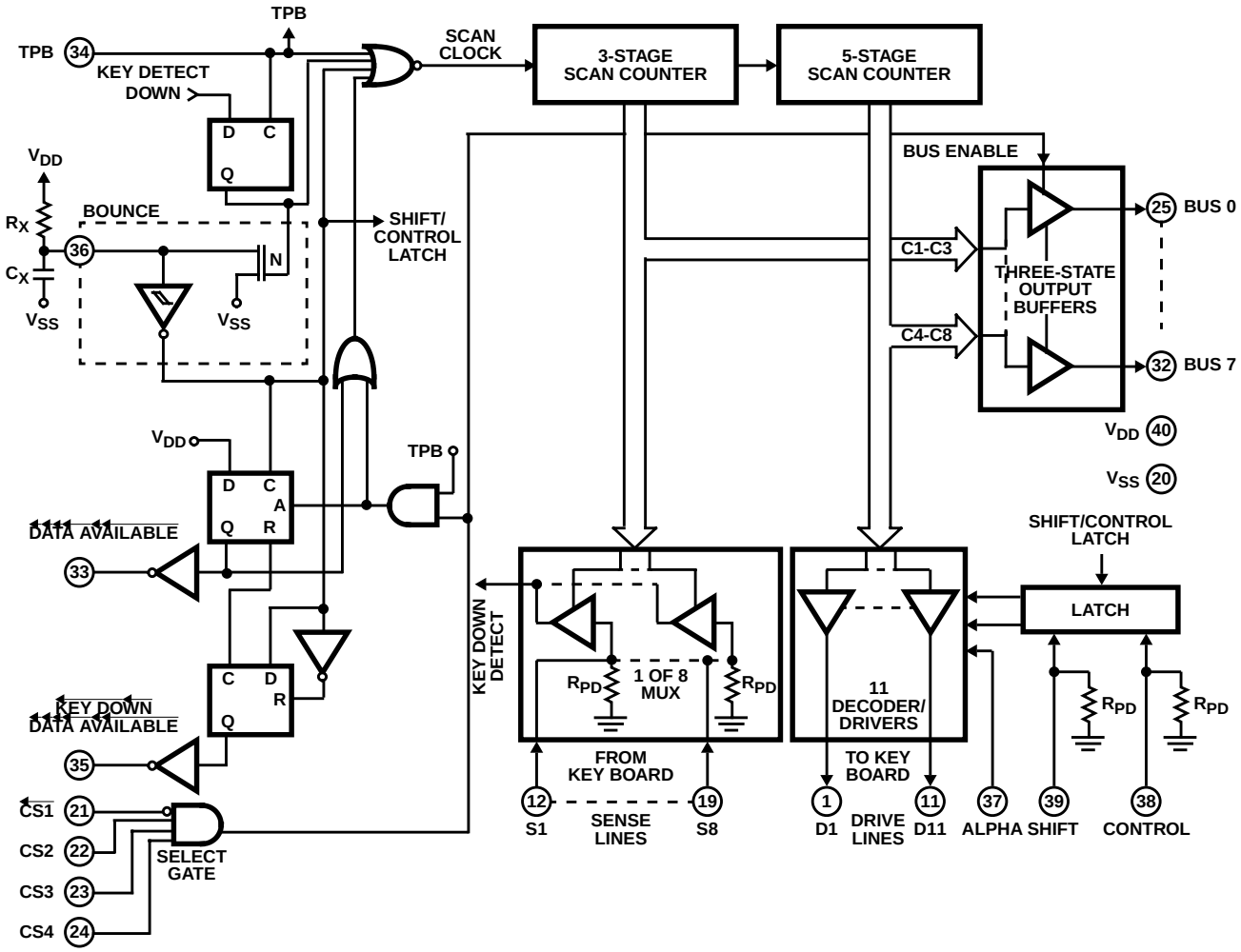

FIGURE 3. CDP1871A CONTROL SCHEMATIC

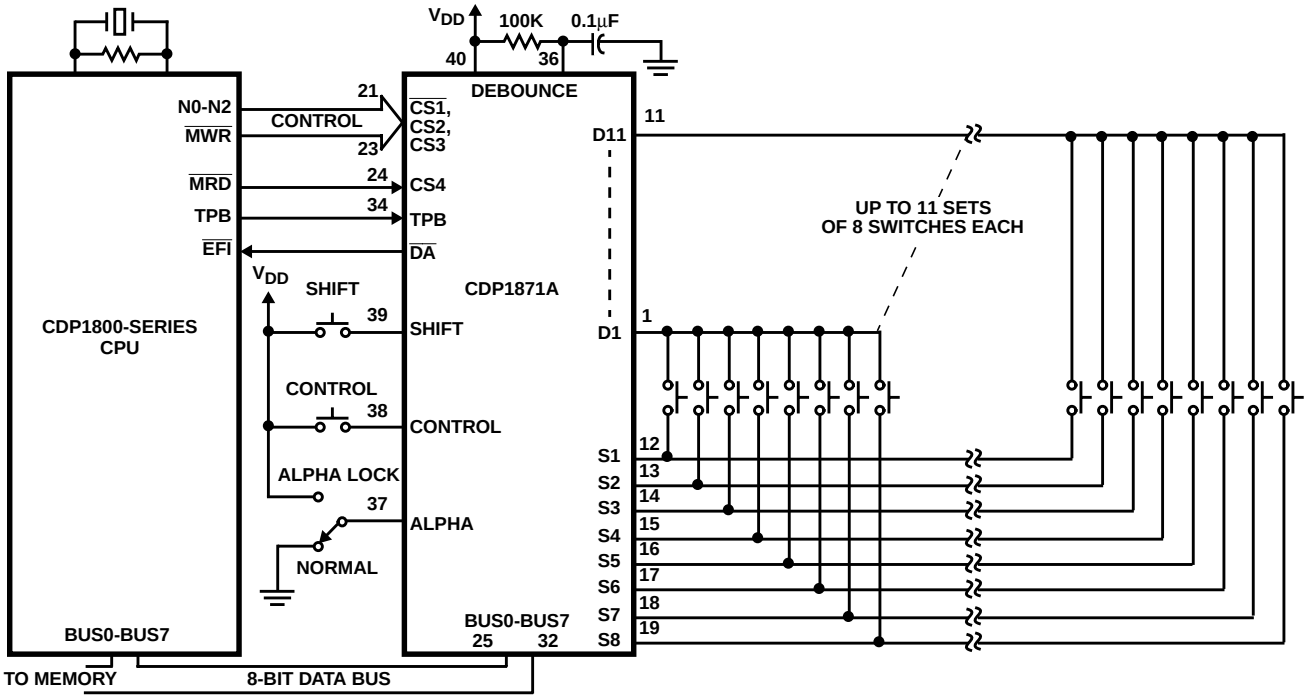

FIGURE 4. TYPICAL CDP1800-SERIES MICROPROCESSOR SYSTEM USING THE CDP1871A

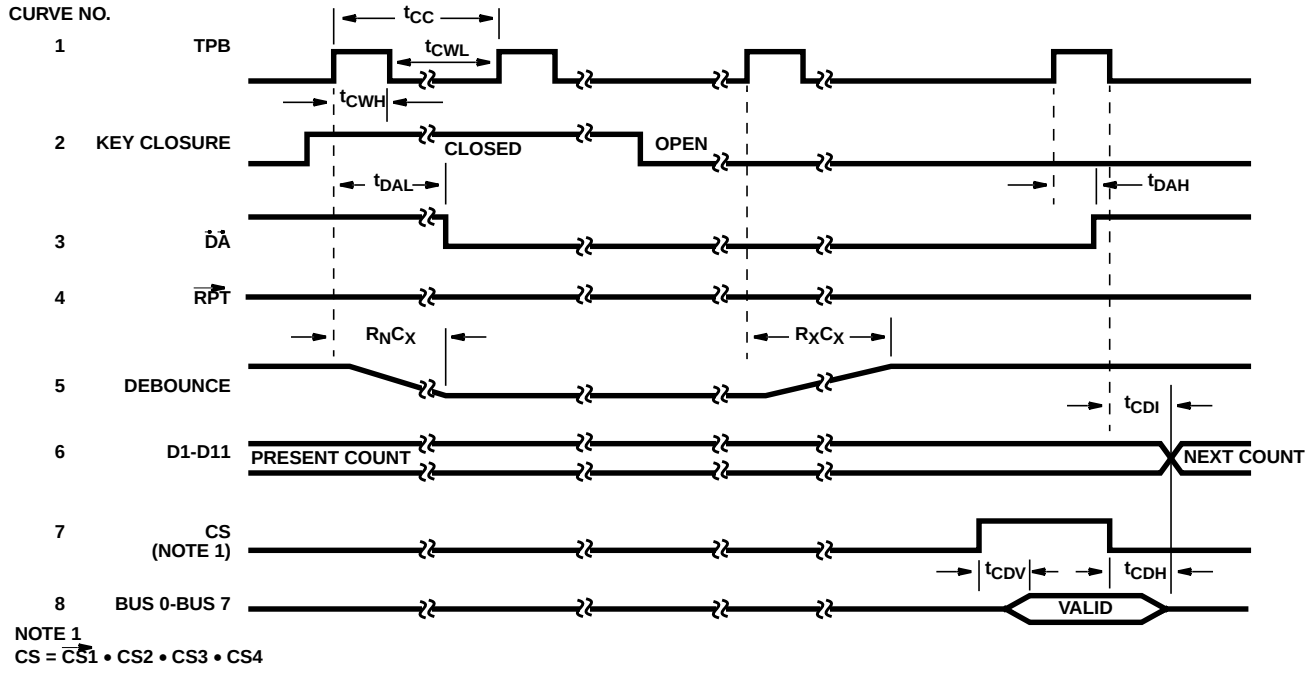

FIGURE 5. CDP1871A DYNAMIC TIMING DIAGRAM (NON-REPEAT)

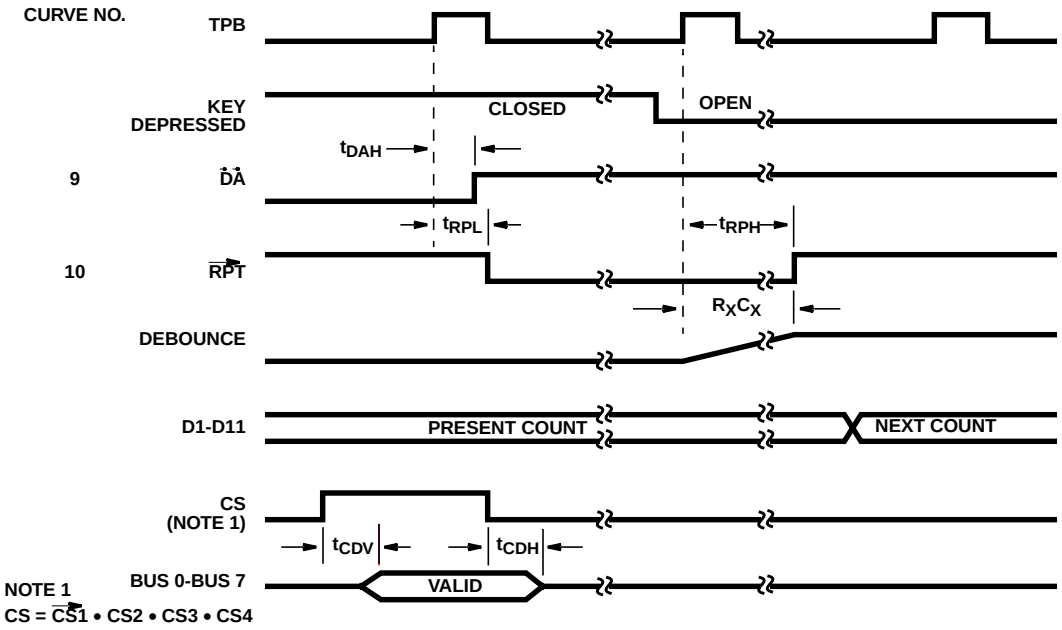

FIGURE 6. CDP1871A DYNAMIC TIMING DIAGRAM (REPEAT)

Dynamic Electrical Characteristics

The dynamic electrical characteristics of the CDP1871A are shown in Table 1, and the timing diagrams in Figure 5. The clock cycle time, the first entry, A, Table 1, and curve 1 in the timing diagram of Figure 5, TPB, define the high and low limits of the clock cycle as $t_{CC} + t_{CWH} + t_{CWL}$. TPB must remain high for at least 100ns (B). The low portion of the clock cycle (t_{CWL}) consists of t_{CD} [1] (E) and the keyboard capacitance. This parameter is selected to allow the TPB clock pulse time to ripple through the scan counters. The maximum frequency of TPB is 400kHz at 5V V_{DD} and 800kHz at 10V V_{DD}.

Table parameters C and D and curve 3 define the data available valid and invalid (reset) delays. The delays are measured from the leading edge of the TPB signal. The valid delay signal is activated on the first TPB signal after the leading edge debounce time when a key closure is detected, and returns high when the encoder is selected on the low-to-high transition of TPB. The valid data out delay and hold times from chip select are shown in table entries F, G and curve 8. The final parameters, H and J, refer to the repeat signal set and reset level delays measured from the leading edge of the TPB; curve 10, Figure 6.

Note in Figure 5 that the action starts when a key closure is sensed by the encoder; curve 2. On the next low-to-high transition of TPB, the debounce time of R_NC_X occurs as C_X discharges through the transistor and the Schmitt trigger clocks the data available flip-flop; curve 3. The R_N value of the transistor is about 200Ω, so that, with an external capacitor of 0.1µF, a 20µs delay can be expected. The key release trailing edge debounce time is calculated from the values of the external capacitor and resistor (R_X, C_X). With a 0.1µF capacitor and a 100kΩ resistor, the debounce time will be 10ms.

Once the data available signal has been reset (chip selected and TPB high), the scan counter operates again on the next trailing edge of TPB, curve 6, and table parameter E. Note in Figure 6 that the repeat signal is activated when the data available signal is reset high while the key is still closed; curves 9 and 10. The repeat signal is reset after the debounce time on the next leading edge of the TPB signal when the key is no longer closed.

TABLE 1. DYNAMIC ELECTRICAL CHARACTERISTICS OF THE CD1871A

PARAMETER			V_{DD} (V)	LIMITS						UNITS
				CDP1871AD CDP1871AE			CDP1871ACD CDP1871ACE			
				MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Clock Cycle Time	A	t_{CC}	5	-	-	-	-	-	-	Note 2
			10	-	-	-	-	-	-	
Clock Pulse Width High	B	t_{CWH}	5	100	40	-	100	40	-	ns
			10	50	20	-	-	-	-	
Data Available Valid Delay	C	t_{DAL}	5	-	260	500	-	260	500	ns
			10	-	130	250	-	-	-	
Data Available Invalid Delay	D	t_{DAH}	5	-	70	150	-	70	150	ns
			10	-	35	75	-	-	-	
Scan Count Delay (Non-Repeat)	E	t_{CD1}	5	-	850	1900	-	850	1900	ns
			10	-	425	950	-	-	-	
Data Out Valid Delay	F	t_{CDV}	5	-	120	250	-	120	250	ns
			10	-	60	125	-	-	-	
Data Out Hold Time	G	t_{CDH}	5	-	100	200	-	100	200	ns
			10	-	50	100	-	-	-	
Repeat Valid Delay	H	t_{RPL}	5	-	150	400	-	150	400	ns
			10	-	75	200	-	-	-	
Repeat Invalid Delay	J	t_{RPM}	5	-	350	700	-	350	700	ns
			10	-	170	350	-	-	-	

NOTES:

1. Typical Values are for $T_A = +25^oC$ and Nominal V_{DD}.
2. $t_{CC} = t_{CWH} + t_{CWL}$, $t_{CWL} = t_{CD1} + K$, k = 0.9 per pF of keyboard capacitance.

Use with Other Processors

Although the keyboard encoder has been designed to operate with CDP1800-series processors, it can be used with other processors if certain precautions are followed.

The encoder is designed as an I/O port; it is not intended to operate with its chip selects active at all times. If this feature is desired, connect an external Schmitt trigger to the debounce pin and place a tristate latch on the data bus.

The most likely use of the CDP1871A will be as an I/O port, and the concern here is the synchronization of the TPB input. The TPB must be held high when the chip selects are active to reset the data available signal. If the TPB is allowed to toggle with the chip selected before it is read, it can hold the data available flip-flop in reset continuously, and can clock the scan counter.

Figure 7 shows the encoder connected to a CDP6805 processor. It can interface directly in this arrangement since the DS output from the CDP6805 is similar to the timing of the TPB timing signal of the CDP1800. However, in a 5MHz system, DS occurs every microsecond, too fast for the encoder's requirement of a TPB input less than 400kHz at 5V. If a divider is used to lower the TPB input, synchronization will be lost. A way around this problem is to use a NAND gate in front of the TPB input and to have one of its inputs tied to the active-low chip select; Figure 8. Then, when the CDP1871A is selected, the TPB input will be forced high and TPB will only toggle again after the encoder is read and the chip select signal is again false.

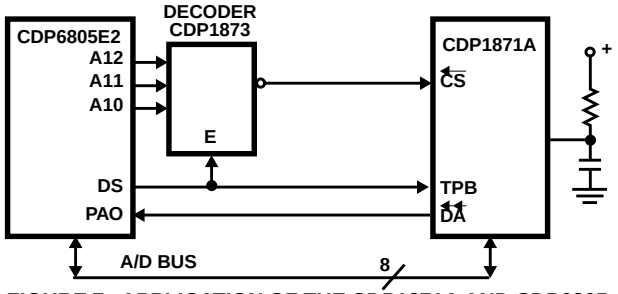

FIGURE 7. APPLICATION OF THE CDP1871A AND CDP6805 PROCESSOR

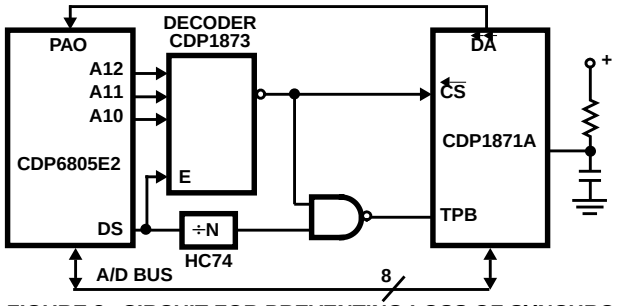

FIGURE 8. CIRCUIT FOR PREVENTING LOSS OF SYNCHRONIZATION IN CDP1871A/CDP6805 INTERFACE

Note that DS enables the decoder, so that during the time that the processor is placing its low address on the data bus, the CDP1871A is disabled. If an asynchronous clock is used for the TPB input, as shown in Figure 9, the NAND gate can be used to assure that TPB remains high during the CDP1871A select times.

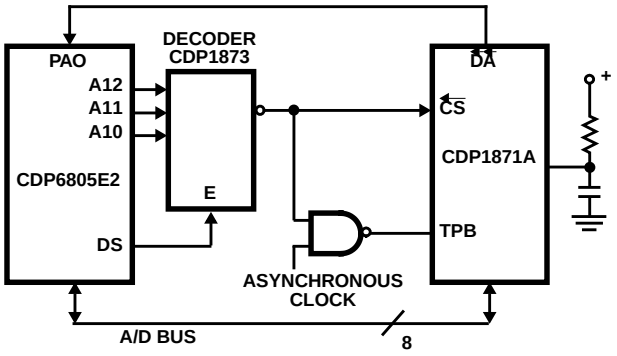

FIGURE 9. METHOD OF ASSURING THAT TPB REMAINS HIGH DURING CDP1871A SELECT TIMES

The keyboard encoder can be used to advantage with another popular processor, the 8085. Figure 10 shows a circuit that interfaces the two devices with an OR gate and a NAND gate. In this circuit, the only time the encoder can drive the data bus is when it is selected and the read signal is active. Since there is no DS equivalent in the 8085 processor, the additional device shown in the figure is needed.

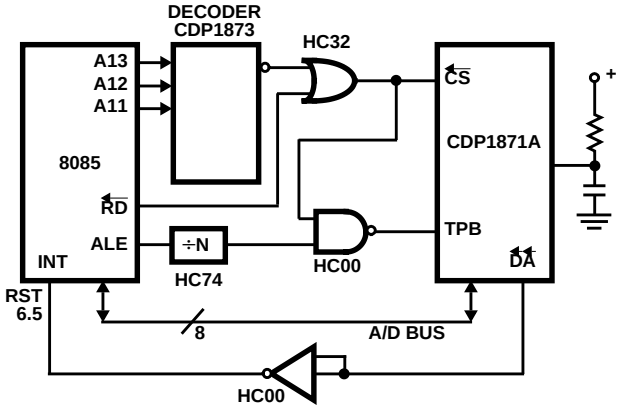

FIGURE 10. A CDP1871A/8085 INTERFACE EMPLOYING AN OR AND A NAND GATE

Figure 11 shows the encoder connected to the 6502 processor. The timing for this part is similar to that for the CDP6805, and the same concerns apply.

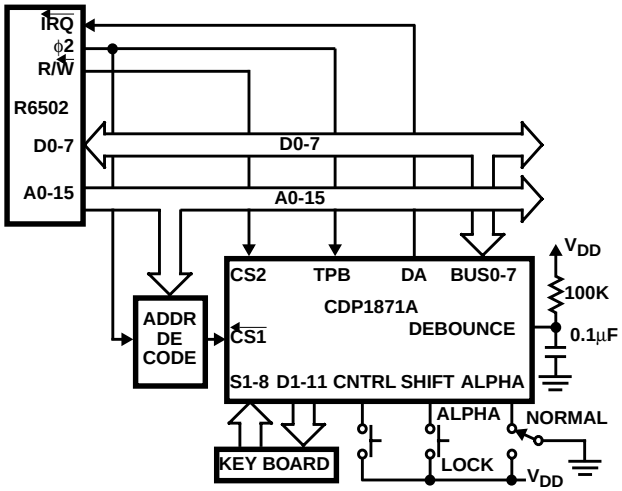

FIGURE 11. A CDP1871A/R6502 INTERFACE

Reference

[1] CMOS Keyboard Encoder, CD1871A," Intersil Corporation File No. 1374. (The CDP1871A comes in two versions: CDP1871A and CDP1871AC. The two are identical except for recommended operating voltage range: 4V to 10.5V for the A version, and 4V to 6.5V for the AC version.)

Appendix

TABLE A-1. DRIVE AND SENSE LINE KEYBOARD CONNECTIONS (NOTE 1)

SENSE LINES	DRIVE LINES															
	D1		D2		D3		D4		D5		D6		D7	(NOTE 2) D8	(NOTE 2) D9	(NOTE 2) D10	(NOTE 2) D11
S1	SP	0	(	8	‘	@	H	H	P	P	X	X	Space	80_{16}	88_{16}	90_{16}	98_{16}
	0		8		@	NUL	h	BS	p	DLE	x	CAN					
S2	!	1	)	9	A	A	I	I	Q	Q	Y	Y		81_{16}	89_{16}	91_{16}	99_{16}
	1		9		a	SOH	i	HT	q	DC1	y	EM					
S3	“	2	*	:	B	B	J	J	R	R	Z	Z	Line Feed	82_{16}	$8A_{16}$	92_{16}	$9A_{16}$
	2		:		b	STX	j	LF	r	DC2	z	SUB					
S4	#	3	+	;	C	C	K	K	S	S	{	[	Escape	83_{16}	$8B_{16}$	93_{16}	$9B_{16}$
	3		;		c	ETX	k	VT	s	DC3	[	ESC					
S5	$	4	<	,	D	D	L	L	T	T	¦	\		84_{16}	$8C_{16}$	94_{16}	$9C_{16}$
	4		,		d	EOT	l	FF	t	DC4	\	FS					
S6	%	5	=	-	E	E	M	M	U	U	}	]	Carriage Return	85_{16}	$8D_{16}$	95_{16}	$9D_{16}$
	5		-		e	ENQ	m	CR	u	NAK	]	GS					
S7	&	6	>	.	F	F	N	N	V	V	~	↑		86_{16}	$8E_{16}$	96_{16}	$9E_{16}$
	6		.		f	ACK	n	SO	v	SYN	↑	RS					
S8	‘	7	?	/	G	G	O	O	W	W	DEL	–	Delete	87_{16}	$8F_{16}$	97_{16}	$9F_{16}$
	7		/		g	BEL	o	SI	w	ETB	–	US					

KEY:

SHIFT*	ALPHA*
NORMAL	CONTROL*

* CONTROL Overrides SHIFT and ALPHA

= No Response

NOTES:

1. Showing ASCII outputs for all combinations with and without SHIFT, ALPHA LOCK and CONTROL.
2. Drive lines 8, 9, 10 and 11 generate non-ASCII hex values which can be used for special codes.

TABLE A-2. HEXADECIMAL VALUES OF ASCII CHARACTERS

	BITS				b7 → b6 → b5 →	MSD							
						0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	b4	b3	b2	b1	HEX ↓	0	1	2	3	4	5	6	7
LSD	0	0	0	0	0	NUL	DLE	SP	0	@	P	\	p
	0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
	0	0	1	0	2	STX	DC2	“	2	B	R	b	r
	0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
	0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
	0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
	0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
	0	1	1	1	7	BEL	ETB	/	7	G	W	g	w
	1	0	0	0	8	BS	CAN	(	8	H	X	h	x
	1	0	0	1	9	HT	EM	)	9	I	Y	i	y
	1	0	1	0	A	LF	SUB	*	:	J	Z	j	z
	1	0	1	1	B	VT	ESC	+	;	K	[	k	{
	1	1	0	0	C	FF	FS	,	<	L	\	l	¦
	1	1	0	1	D	CR	GS	-	=	M	]	m	}
	1	1	1	0	E	SO	RS	.	>	N	↑	n	~
	1	1	1	1	F	SI	US	/	?	O	–	o	DEL

TABLE A-3. RECOMMENDED OPERATING CONDITIONS AT T_A = -40°C TO +85°C

For Maximum Reliability, Operating Conditions should be selected so that operation is always within the following ranges:

PARAMETER		V_{DD} (V)	LIMITS				UNITS
			CDP1871AD CDP1871AE		(NOTE 1) CDP1871ACD CDP1871ACE		
			MIN	MAX	MIN	MAX	
Supply Voltage Range		-	4	10.5	4	6.5	V
Recommended Input Voltage Range		-	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Clock Input Frequency, TPB (Keyboard Capacitance = 200pF)	f_{CL}	5	DC	0.4	DC	0.4	MHz
		10	DC	0.8	-	-	

NOTE:

1. D in suffix indicates ceramic package; E indicates plastic package.

TABLE A-4. STATIC ELECTRICAL CHARACTERISTICS at T_A = -40°C to +85°C, Except as Noted

PARAMETER	SYMBOL	CONDITIONS			LIMITS						UNITS
					CDP1871AD CDP1871AE			CDP1871ACD CDP1871ACE			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0, 5	5	-	0.1	50	-	1	200	µA
		-	0, 10	10	-	1	200	-	-	-	
Output Low Drive (Sink) Current (except debounce and D1 - D11)	I_{OL}	0.4	0, 5	5	0.5	1	-	0.5	1	-	mA
		0.5	0, 10	10	1	2	-	-	-	-	
Debounce	I_{OL}	0.4	0, 5	5	0.75	1.5	-	0.75	1.5	-	
		0.5	0, 10	10	1	2	-	-	-	-	
D1 - D11	I_{OL}	0.4	0, 5	5	.05	0.1	-	.05	0.1	-	
		0.5	0, 10	10	0.1	0.2	-	-	-	-	
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-0.3	-0.6	-	-0.3	-0.6	-	
		9.5	0, 10	10	-0.75	-1.5	-	-	-	-	
Input Low Voltage (Except Debounce)	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		1, 9	-	10	-	-	3	-	-	-	
Input High Voltage (Except Debounce)	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	
		1, 9	-	10	7	-	-	-	-	-	
Debounce Schmitt Trigger Input Voltage											
Positive Trigger Voltage	V_D	0.4	-	5	2.0	3.3	4.0	2.0	3.3	4.0	
		0.5	-	10	4.0	6.3	8.0	-	-	-	
Negative Trigger Voltage	V_N	0.4	-	5	0.8	1.8	3.0	0.8	1.8	3.0	
		0.5	-	10	1.9	4.0	6.0	-	-	-	
Hysteresis	V_H	0.4	0, 5	5	0.3	1.6	2.6	0.3	1.6	2.6	
		0.5	0, 10	10	0.7	2.3	4.7	-	-	-	
Output Voltage Low Level	V_{OL}	-	0, 5	5	-	0	0.05	-	0	0.05	
		-	0, 10	10	-	0	0.05	-	-	-	
Output Voltage High Level	V_{OH}	-	0, 5	5	4.95	5	-	4.95	5	-	
		-	0, 10	10	9.95	10	-	-	-	-	
Input Leakage Current (Except S1 - S8, Shift, Control)	I_{IN}	-	0, 5	5	-	0.01	1	-	0.01	1	µA
		-	0, 10	10	-	0.01	1	-	-	-	
Three-State Output Leakage Current	I_{OUT}	0.5	0, 5	5	-	0.01	1	-	0.02	2	
		0, 10	0, 10	10	-	0.02	2	-	-	-	
Pull-Down Resistor Value (S1 - S8, Shift, Control)	R_{PD}	-	-	-	7	14	24	7	14	24	kΩ
Operating Current (All outputs unloaded)	I_{OPER}	0.5, 4.5	0, 5	5	-	0.6	-	-	0.6	-	mA
f_{CL} = 0.4MHz											
f_{CL} = 0.8MHz		1, 9	0, 10	10	-	2.7	-	-	-	-	

NOTE:

1. Typical values are for T_A = +25°C and nominal V_{DD}.