# ACTS74MS

## Radiation Hardened Dual D Flip Flop with Set and Reset

January 1996

### Features

- Devices QML Qualified in Accordance with MIL-PRFF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96713 and Intersil's QM Plan
- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose . . . . . >300K RAD (Si)
- Single Event Upset (SEU) Immunity: <1 x $10^{-10}$ Errors/Bit/Day (Typ)
- SEU LET Threshold . . . . . >100 MEV-$cm^2$/mg
- Dose Rate Upset . . . . . >$10^{11}$ RAD (Si)/s, 20ns Pulse
- Dose Rate Survivability . . . . . >$10^{12}$ RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range . . . . . -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range . . . . . 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current ≤ 1μA at VOL, VOH
- Fast Propagation Delay . . . . . 20ns (Max), 13ns (Typ)

### Description

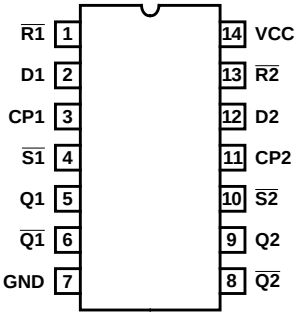
The Intersil ACTS74MS is a Radiation Hardened Dual D Flip Flop with Set(s) and Reset (R). The logic level at data input is transferred to the output during the positive transition of the clock. The Set and Reset are independent from the clock and accomplished by a low level on the appropriate input.

The ACTS74MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of a radiation hardened, high-speed, CMOS/SOS Logic Family.

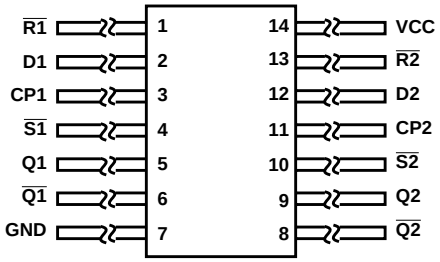
The ACTS74MS is supplied in a 14 lead Ceramic Flatpack (K suffix) or a 14 Lead Ceramic Dual-In-Line Package (D suffix).

### Pinouts

**14 PIN CERAMIC DUAL-IN-LINE**
**MIL-STD-1835 DESIGNATOR CDIP2-T14,**
**LEAD FINISH C**
TOP VIEW




**14 PIN CERAMIC FLATPACK**
**MIL-STD-1835 DESIGNATOR CDFP3-F14,**
**LEAD FINISH C**
TOP VIEW




### Ordering Information

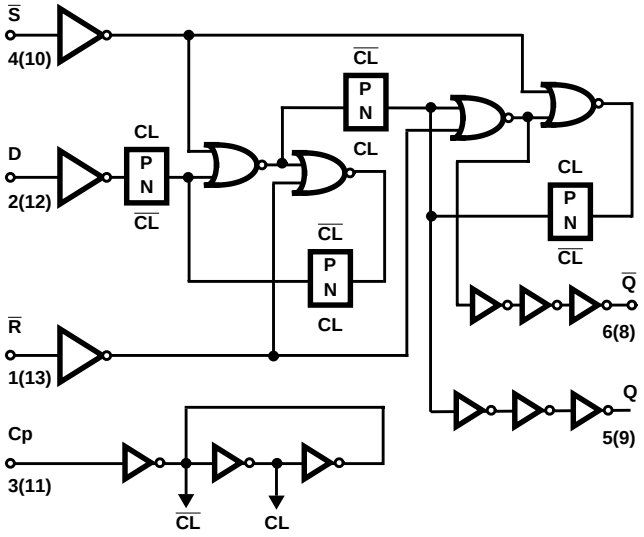
| PART NUMBER | TEMPERATURE RANGE | SCREENING LEVEL | PACKAGE |
|---|---|---|---|
| 5962F9671301VCC | -55°C to +125°C | MIL-PRF-38535 Class V | 14 Lead SBDIP |
| 5962F9671301VXC | -55°C to +125°C | MIL-PRF-38535 Class V | 14 Lead Ceramic Flatpack |
| ACTS74D/Sample | 25°C | Sample | 14 Lead SBDIP |
| ACTS74K/Sample | 25°C | Sample | 14 Lead Ceramic Flatpack |
| ACTS74HMSR | 25°C | Die | Die |





Spec Number **518787**
File Number **3382.1**

## Functional Diagram




**TRUTH TABLE**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{SET}$ | $\overline{RESET}$ | CP | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H (Note 2) | H (Note 2) |
| H | H | ⌐/ | H | H | L |
| H | H | ⌐/ | L | L | H |
| H | H | L | X | Q0 | $\overline{Q0}$ |

H = High Level (Steady State)
L = Low Level (Steady State)
X = Don't Care
⌐/ = Transition from Low to High Level

NOTES:

1. Q0 = the level of Q before the indicated input conditions were established.
2. This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

## Die Characteristics

**DIE DIMENSIONS:**

88 mils x 88 mils
2240mm x 2240mm

**METALLIZATION:**

Type: AlSi
Metal 1 Thickness: 7.125kÅ ±1.125kÅ
Metal 2 Thickness: 9kÅ ±1kÅ

**GLASSIVATION:**

Type: $SiO_2$
Thickness: 8kÅ ±1kÅ

**WORST CASE CURRENT DENSITY:**

$<2.0 \times 10^5 A/cm^2$

**BOND PAD SIZE:**

110µm x 110µm
4.3 mils x 4.3 mils

## Metallization Mask Layout

**ACTS74MS**