ADVANCE INFORMATION | Data Sheet | June 2000 | File Number 4657.3

3V Dual 8-Bit, 20/40/60MSPS A/D Converter with Internal Voltage Reference

The ISL5640 is a monolithic, dual 8-bit analog-to-digital converter fabricated in an advanced CMOS process. It is designed for high speed applications where integration, bandwidth and accuracy are essential. The ISL5640 features a 9-stage pipeline architecture. The fully pipelined architecture and an innovative input stage enable the ISL5640 to accept a variety of input configurations, single-ended or fully differential. Only one external clock is necessary to drive both converters and an internal band-gap voltage reference is provided. This allows the system designer to realize an increased level of system integration resulting in decreased cost and power dissipation.

The ISL5640 has excellent dynamic performance while consuming less than 100mW power at 40MSPS. The A/D only requires a single +3.0V power supply. Data output latches are provided which present valid data to the output bus with a latency of 5 clock cycles.

The ISL5640 is offered in 20MSPS, 30MSPS, 40MSPS and 60MSPS sampling rates.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.	SAMPLING RATE (MSPS)
ISL5640/2IN	-40 to 85	48 Ld LQFP	Q48.7x7	20
ISL5640/3IN	-40 to 85	48 Ld LQFP	Q48.7x7	30
ISL5640/4IN	-40 to 85	48 Ld LQFP	Q48.7x7	40
ISL5640/6IN	-40 to 85	48 Ld LQFP	Q48.7x7	60
ISL5640 EVAL	25	Evaluation Platform		

Features

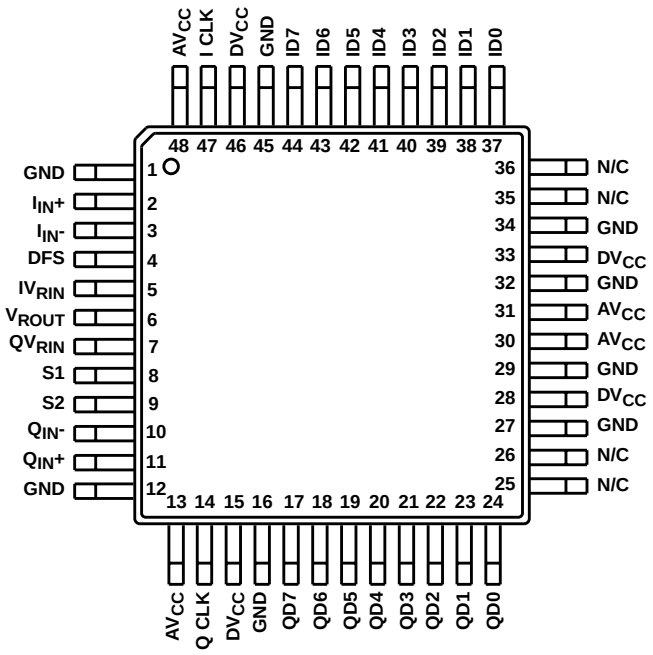
- Sampling Rate 40MSPS
- 7.4 Bits at f_{IN} = 1MHz
- Low Power at 40MSPS. 100mW
- Power Down Mode . . . . . <1mW
- Wide Full Power Input Bandwidth. 250MHz
- SFDR at f_{IN} = 1MHz. 55dB
- Excellent Channel-to-Channel Isolation . . . . . >75dB
- On-Chip Sample and Hold Amplifiers
- Internal Bandgap Voltage Reference 1.25V
- Single Supply Voltage Operation . . . . . +3.0V
- Offset Binary or Two's Complement Output Format
- Dual 8-Bit A/D Converters on a Monolithic Chip
- Pin Compatible Upgrade to AD9288

Applications

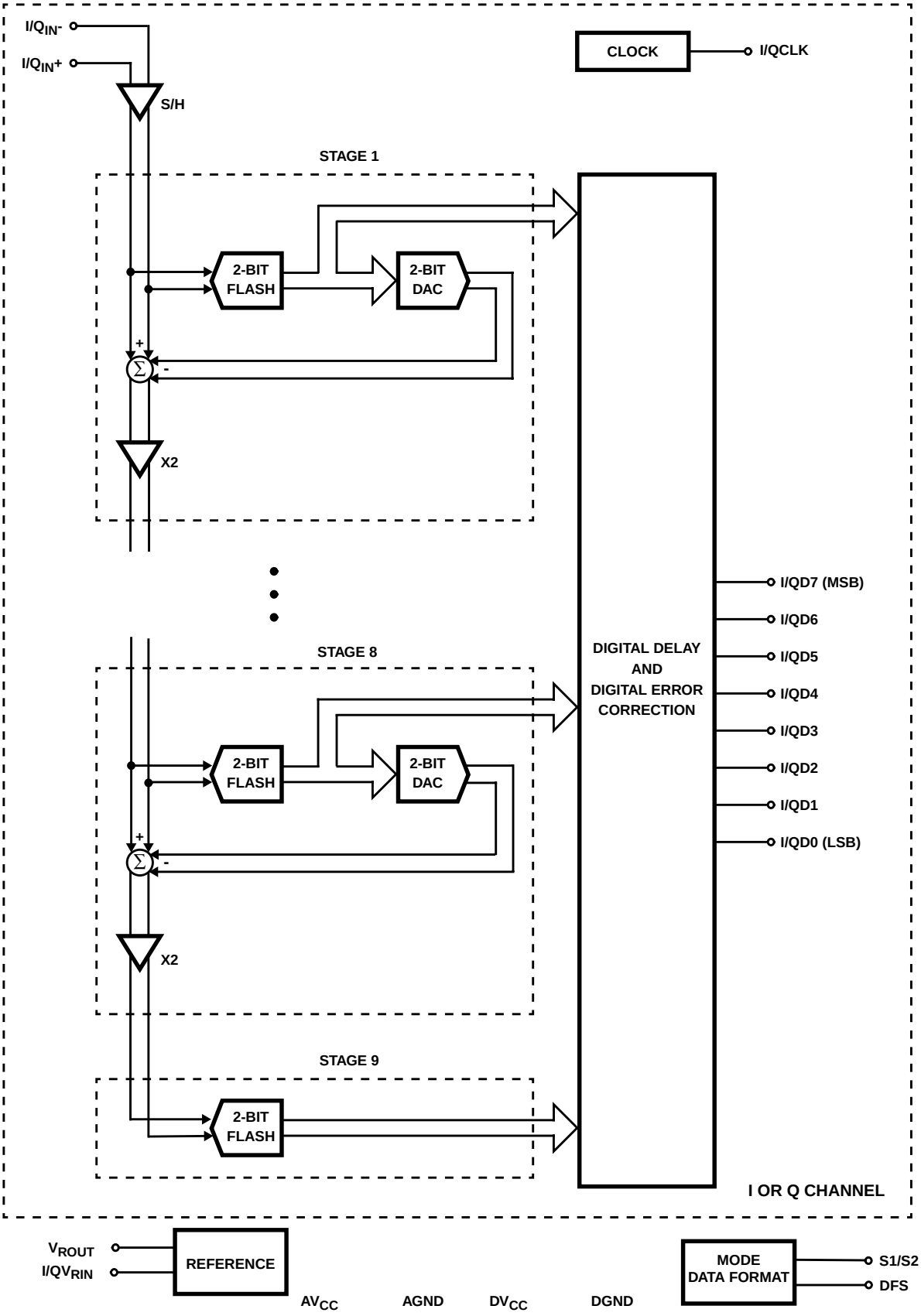
- Wireless Local Loop
- PSK and QAM I&Q Demodulators
- Medical Imaging
- High Speed Data Acquisition

Pinout

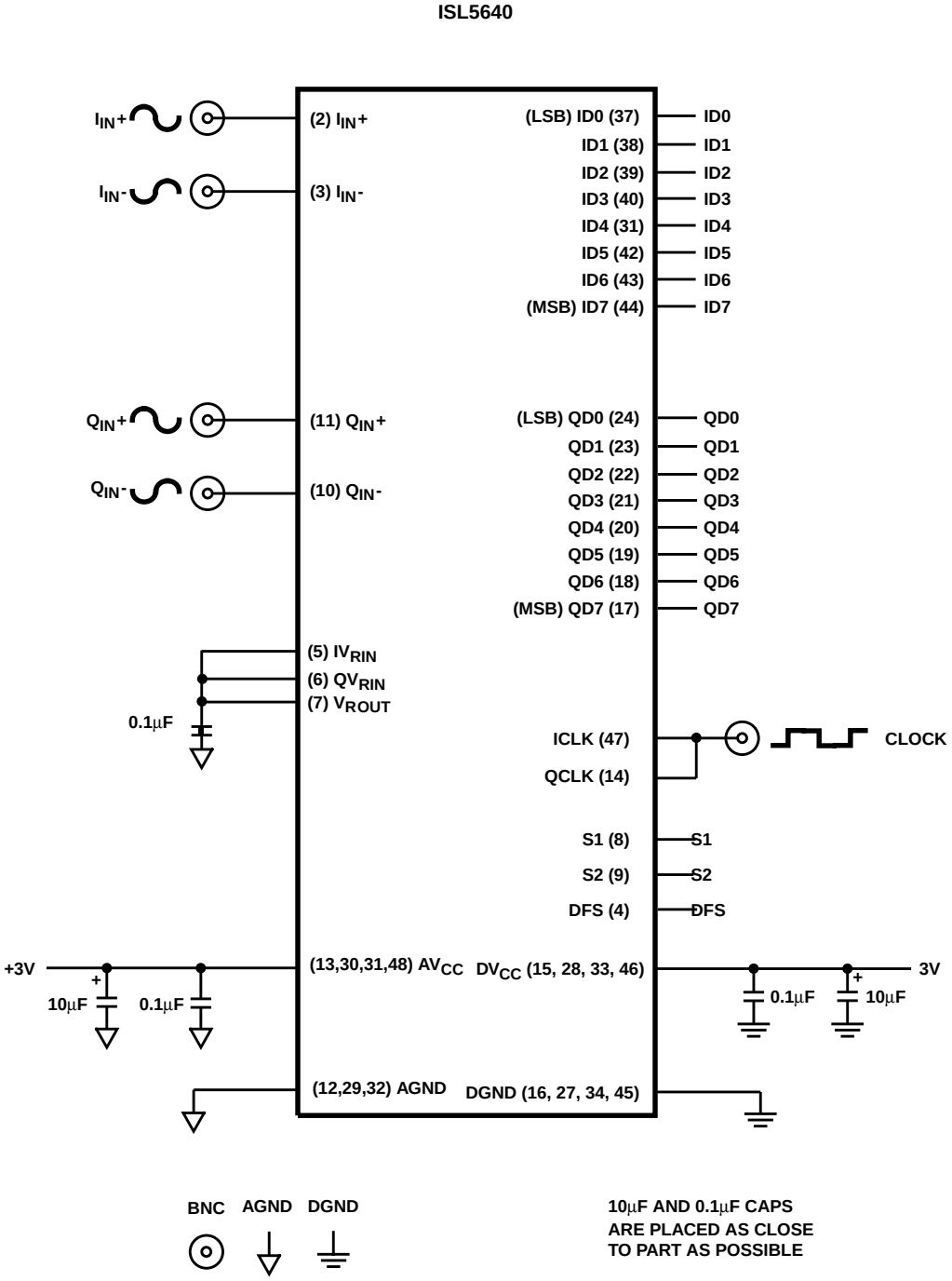
48 LEAD LQFP
TOP VIEW



Functional Block Diagram



Typical Application Schematic



Pin Descriptions

PIN NO.	NAME	DESCRIPTION
1	A_{GND}	Analog Ground
2	I_{IN+}	I-Channel Positive Analog Input
3	I_{IN-}	I-Channel Negative Analog Input
4	DFS	Data Format Select (Low for Offset Binary and High for Twos Complement Output Format)
5	IV_{RIN}	I-Channel Voltage Reference Input
6	V_{ROUT}	+1.25V Reference Voltage Output (Decouple with 0.1µF Capacitor)
7	QV_{RIN}	Q-Channel Voltage Reference Input
8	S1	Mode Select Pin 1 (See Table)
9	S2	Mode Select Pin 2 (See Table)
10	Q_{IN-}	Q-Channel Negative Analog Input
11	Q_{IN+}	Q-Channel Positive Analog Input
12	A_{GND}	Analog Ground
13	AV_{CC}	Analog Supply
14	QCLK	Q-Channel Clock Input
15	DV_{CC}	Digital Supply
16	D_{GND}	Digital Ground
17	QD7	Q-Channel, Data Bit 7 Output (MSB)
18	QD6	Q-Channel, Data Bit 6 Output
19	QD5	Q-Channel, Data Bit 5 Output
20	QD4	Q-Channel, Data Bit 4 Output
21	QD3	Q-Channel, Data Bit 3 Output
22	QD2	Q-Channel, Data Bit 2 Output
23	QD1	Q-Channel, Data Bit 1 Output

Pin Descriptions (Continued)

PIN NO.	NAME	DESCRIPTION
24	QD0	Q-Channel, Data Bit 0 Output (LSB)
25	N/C	No Connect
26	N/C	No Connect
27	D_{GND}	Digital Ground
28	DV_{CC}	Digital Supply
29	A_{GND}	Analog Ground
30	AV_{CC}	Analog Supply
31	AV_{CC}	Analog Supply
32	A_{GND}	Analog Ground
33	DV_{CC}	Digital Supply
34	D_{GND}	Digital Ground
35	N/C	No Connect
36	N/C	No Connect
37	ID0	I-Channel, Data Bit 0 Output
38	ID1	I-Channel, Data Bit 1 Output
39	ID2	I-Channel, Data Bit 2 Output
40	ID3	I-Channel, Data Bit 3 Output
41	ID4	I-Channel, Data Bit 4 Output
42	ID5	I-Channel, Data Bit 5 Output
43	ID6	I-Channel, Data Bit 6 Output
44	ID7	I-Channel, Data Bit 7 Output (MSB)
45	D_{GND}	Digital Ground
46	DV_{CC}	Digital Supply
47	ICLK	I-Channel Clock Input
48	AV_{CC}	Analog Supply

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, AV_{CC} or DV_{CC} to AGND or DGND 4V
DGND to AGND 0.3V
Digital I/O Pins . . . . . DGND to DV_{CC}
Analog I/O Pins . . . . . AGND to AV_{CC}

Operating Conditions

Temperature Range
ISL5640IN . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
ISL5640IN 70
Maximum Junction Temperature . . . . . .150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . .300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$A_{VDD} = D_{VDD} = +3.3V$; $V_{IN} = 1.50V$; $f_S = 40MSPS$ at 50% Duty Cycle; $C_L = 10pF$; $T_A = 25^oC$; Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		8	-	-	Bits
Integral Linearity Error, INL	f_{IN} = 1MHz	-	0.5	-	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = 1MHz	-	±0.2	±1.0	LSB
Offset Error, V_{OS}	f_{IN} = DC	-10	-	+10	LSB
Full Scale Error, FSE	f_{IN} = DC	-	1	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	-	-	MSPS
Maximum Conversion Rate	No Missing Codes	40	-	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 1MHz	-	7.5	-	Bits
Signal to Noise and Distortion Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 1MHz	-	46	-	dB
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 10MHz	-	47	-	dB
Total Harmonic Distortion, THD	f_{IN} = 10MHz	-	-53	-	dBc
2nd Harmonic Distortion	f_{IN} = 10MHz	-	-54	-	dBc
3rd Harmonic Distortion	f_{IN} = 10MHz	-	-70	-	dBc
Spurious Free Dynamic Range, SFDR	f_{IN} = 10MHz	-	54	-	dBc
Intermodulation Distortion, IMD	f1 = 1MHz, f2 = 1.02MHz	-	-	-	dBc
I/Q Channel Crosstalk		-	-	-	dBc
I/Q Channel Offset Match		-	-	-	LSB
I/Q Channel Full Scale Error Match		-	-	-	LSB
Transient Response	(Note 2)	-	-	-	Cycle
Over-Voltage Recovery	0.2V Overdrive (Note 2)	-	-	-	Cycle
ANALOG INPUT					
Maximum Peak-to-Peak Single-Ended Analog Input Range		-	1.0	-	V
Analog Input Resistance, R_{INA} or R_{INB}	V_{INA}, V_{INB} = V_{REF}, DC	-	-	-	MΩ
Analog Input Capacitance, C_{INA} or C_{INB}	V_{INA}, V_{INB} = 1.5V, DC	-	-	-	pF

Electrical Specifications

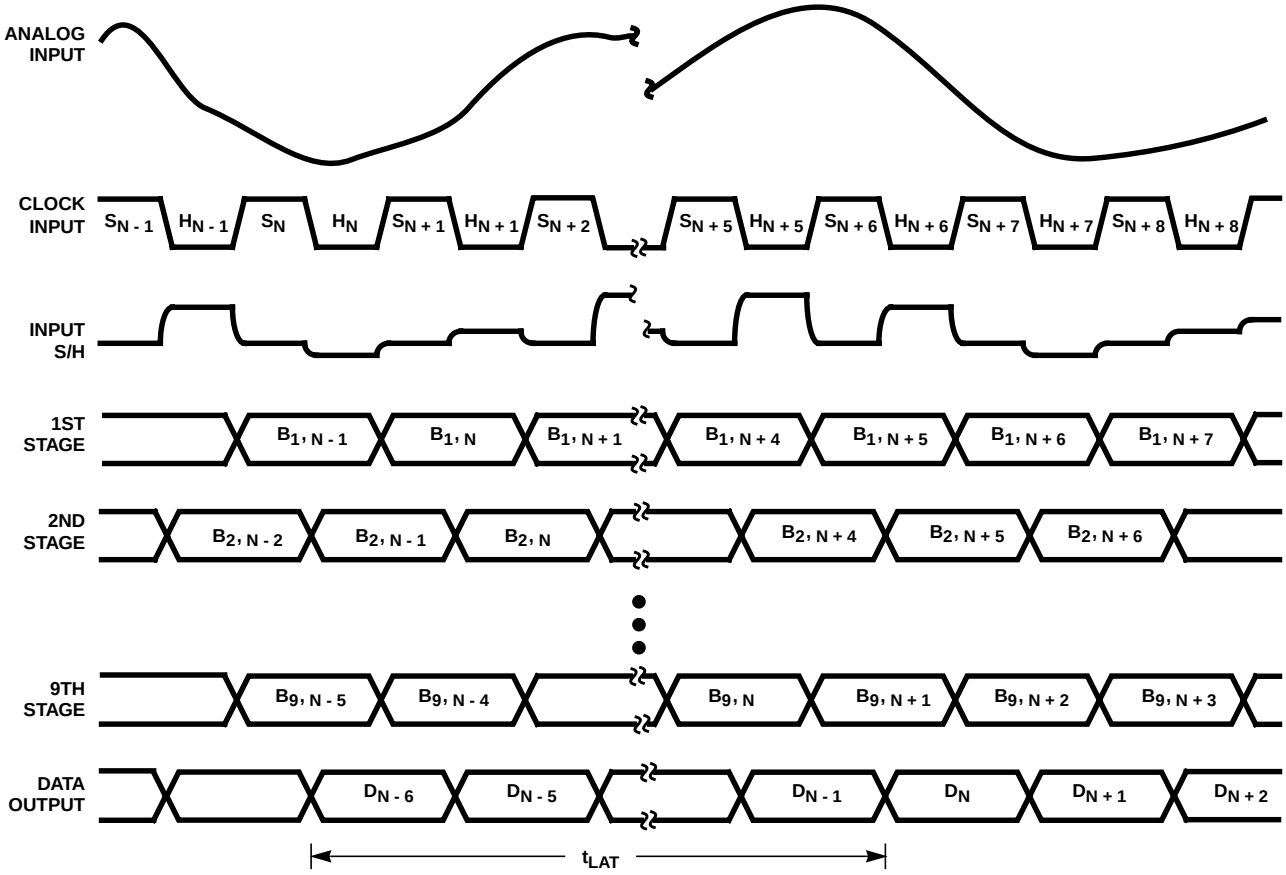
A_{VDD} = D_{VDD} = +3.3V; V_{IN} = 1.50V; f_S = 40MSPS at 50% Duty Cycle; C_L = 10pF; T_A = 25°C; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Analog Input Bias Current, I_BA or I_BB	V_{INA}/V_{INB} = ART/BRT, ARB/BRB, DC (Notes 2, 3)	-	-	-	µA
Full Power Input Bandwidth, FPBW	f_S = 40MHz, (Note 2)	-	250	-	MHz
REFERENCE VOLTAGE INPUT					
Reference Voltage Input Range		-	-	-	V
Total Reference Resistance, R_{RIN}		-	300	-	Ω
Reference Current, I_{RIN}		-	-	-	mA
SAMPLING CLOCK INPUT					
Input Logic High Voltage, V_{IH}	CLK	2.0	-	-	V
Input Logic Low Voltage, V_{IL}	CLK	-	-	0.8	V
Input Logic High Current, I_{IH}	CLK, V_{IH} = 3.3V	-	-	-	µA
Input Logic Low Current, I_{IL}	CLK, V_{IL} = 0V	-	-	-	µA
Input Capacitance, C_{IN}	CLK	-	-	-	pF
DIGITAL OUTPUTS					
Output Logic High Voltage, V_{OH}	I_{OH} = 100µA; D_{VDD} = 3.3V	-	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OL} = 1.5mA; D_{VDD} = 3.3V	-	-	-	V
Output Logic High Voltage, V_{OH}	I_{OH} = 100µA; D_{VDD} = 3.0V	-	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OL} = 100µA; D_{VDD} = 3.0V	-	-	-	V
Output Capacitance, C_{OUT}		-	-	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	4	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps_{RMS}
Data Output Hold, t_H		-	10.7	-	ns
Data Output Delay, t_{OD}		-	11.7	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	-	5	-	Cycles
Power-Up Initialization	Data Invalid Time (Note 2)	-	-	-	Cycles
Sample Clock Pulse Width (Low)	(Note 2)	11.25	12.5	-	ns
Sample Clock Pulse Width (High)	(Note 2)	11.25	12.5	-	ns
Sample Clock Duty Cycle Variation		-	±5	-	%
POWER SUPPLY CHARACTERISTICS					
Analog Supply Voltage, A_{VDD}	(Note 2)	3.0	3.3	3.6	V
Digital Supply Voltage, D_{VDD}	(Note 2)	3.0	3.3	3.6	V
Supply Current, I_{DD}	f_S = 40MSPS	-	30.3	-	mA
Power Dissipation		-	100	110	mW
Offset Error Sensitivity, ΔV_{OS}	A_{VDD} or D_{VDD} = 3.3V ±5%	-	±0.125	-	LSB
Gain Error Sensitivity, ΔFSE	A_{VDD} or D_{VDD} = 3.3V ±5%	-	±0.15	-	LSB

NOTES:

1. Parameter guaranteed by design or characterization and not production tested.
2. With the clock low and DC input.

Timing Waveforms



NOTES:

3. S_N: N-th sampling period.
4. H_N: N-th holding period.
5. $B_{M,N}$: M-th stage digital output corresponding to N-th sampled input.
6. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. ISL5640 INTERNAL CIRCUIT TIMING

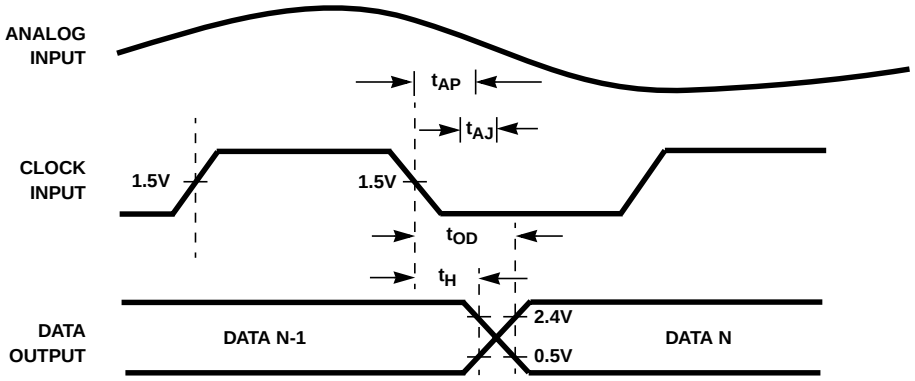


FIGURE 2. ISL5640 INPUT TO OUTPUT TIMING

TABLE 1. A/D CODE TABLE

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE ($I/Q_{IN}+ - I/Q_{IN}-$)	OFFSET BINARY OUTPUT CODE									
		MSB									LSB
		I/QD9	I/QD8	I/QD7	I/QD6	I/QD5	I/QD4	I/QD3	I/QD2	I/QD1	I/QD0
+Full Scale ($+f_S$) $-^1/_4$LSB	0.499756V	1	1	1	1	1	1	1	1	1	1
$+f_S - 1^1/_4$LSB	0.498779V	1	1	1	1	1	1	1	1	1	0
$+^3/_4$LSB	732.422µV	1	0	0	0	0	0	0	0	0	0
$-^1/_4$LSB	-244.141µV	0	1	1	1	1	1	1	1	1	1
$-f_S + 1^3/_4$LSB	-0.498291V	0	0	0	0	0	0	0	0	0	1
-Full Scale ($-f_S$) + $^3/_4$LSB	-0.499268V	0	0	0	0	0	0	0	0	0	0

NOTE:

7. The voltages listed above represent the ideal center of each output code shown with V_{REFIN} = +1.25V.

Detailed Description

Theory of Operation

The ISL5640 is a dual 8-bit fully differential sampling pipeline A/D converter with digital error correction logic. Figure 3 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H) amplifiers. The switches are controlled by an internal sampling clock which is a non-overlapping two phase signal, Φ_1 and Φ_2, derived from the master sampling clock. During the sampling phase, Φ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of Φ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, Φ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The front end sample-and-hold output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the I/Q_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 400MHz for the converter.

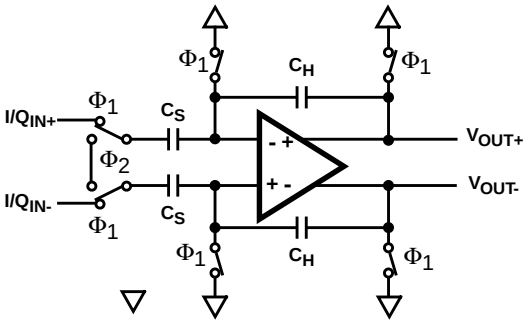


FIGURE 3. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the Functional Block Diagram and the timing diagram in Figure 1, eight identical pipeline subconverter stages, each containing a two-bit flash converter and a two-bit multiplying digital-to-analog converter, follow the S/H circuit with the ninth stage being a two bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual subconverter clock signal is offset by 180 degrees from the previous stage clock signal resulting in alternate stages in the pipeline performing the same operation.

The output of each of the eight identical two-bit subconverter stages is a two-bit digital word containing a supplementary bit to be used by the digital error correction logic. The output of each subconverter stage is input to a digital delay line which is controlled by the internal sampling clock. The function of the digital delay line is to time align the digital outputs of the eight identical two-bit subconverter stages with the corresponding output of the ninth stage flash converter before applying the eighteen bit result to the digital error correction logic. The digital error correction logic uses the supplementary bits to correct any error that may exist before generating the final ten bit digital data output of the converter.

Because of the pipeline nature of this converter, the digital data representing an analog input sample is output to the digital data bus following the 6th cycle of the clock after the

analog sample is taken (see the timing diagram in Figure 1). This time delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital output data is provided in offset binary format (see Table 1, A/D Code Table).

Internal Reference Voltage Output, V_{ROUT}

The ISL5640 is equipped with an internal 1.25V bandgap reference voltage generator, therefore, no external reference voltage is required. V_{ROUT} should be connected to V_{RIN} when using the internal reference voltage. An external, user-supplied, 0.1µF capacitor may be connected from the V_{ROUT} output pin to filter any stray board noise.

Reference Voltage Inputs, I/Q V_{REFIN}

The ISL5640 is designed to accept a 1.25V reference voltage source at the V_{RIN} input pins for the I and Q channels. Typical operation of the converter requires V_{RIN} to be set at 1.25V. The ISL5640 is tested with V_{RIN} connected to V_{ROUT} yielding a fully differential analog input voltage range of ±0.5V.

The user does have the option of supplying an external 1.25V reference voltage. As a result of the high input impedance presented at the V_{RIN} input pin, MΩ typically, the external reference voltage being used is only required to source small amount of reference input current.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the reference voltage input pin, V_{RIN}.

Analog Input, Differential Connection

The analog input of the ISL5640 is a differential input that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 4 and Figure 5) will deliver the best performance from the converter.

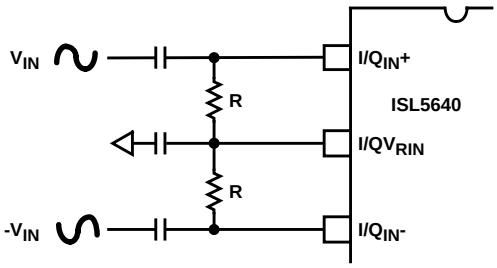


FIGURE 4. AC COUPLED DIFFERENTIAL INPUT

Since the ISL5640 is powered by a single +3V analog supply, the analog input is limited to be between ground and +3V. For the differential input connection this implies the analog input common mode voltage can range from 0.25V to 2.75V. The performance of the ADC does not change significantly with the value of the analog input common mode voltage.

For the AC coupled differential input (Figure 4) and with V_{RIN} connected to V_{ROUT}, full scale is achieved when the V_{IN} and $-V_{IN}$ input signals are $0.5V_{P-P}$, with $-V_{IN}$ being 180 degrees out of phase with V_{IN}. The converter will be at positive full scale when the $I/Q_{IN}+$ input is at I/Q_{VRIN} + 0.25V and the $I/Q_{IN}-$ input is at I/Q_{VRIN} - 0.25V ($I/Q_{IN}+ - I/Q_{IN}- = +0.5V$). Conversely, the converter will be at negative full scale when the $I/Q_{IN}+$ input is equal to I/Q_{VRIN} - 0.25V and $I/Q_{IN}-$ is at I/Q_{VRIN} + 0.25V ($I/Q_{IN}+ - I/Q_{IN}- = -0.5V$).

The analog input can be DC coupled (Figure 5) as long as the inputs are within the analog input common mode voltage range ($0.25V \leq VDC \leq 2.75V$).

The resistors, R, in Figure 5 are not absolutely necessary but may be used as load setting resistors. A capacitor, C, connected from $I/Q_{IN}+$ to $I/Q_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

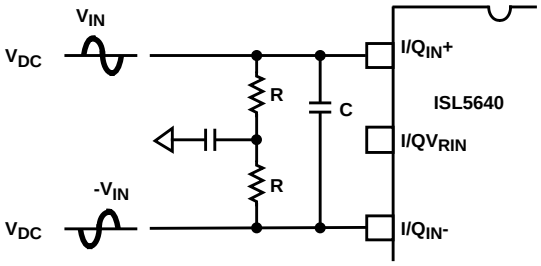


FIGURE 5. DC COUPLED DIFFERENTIAL INPUT

Analog Input, Single-Ended Connection

The configuration shown in Figure 6 may be used with a single ended AC coupled input.

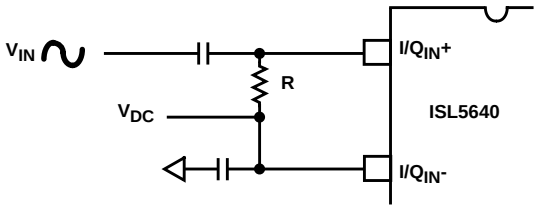


FIGURE 6. AC COUPLED SINGLE ENDED INPUT

Again, with V_{RIN} connected to V_{ROUT}, if V_{IN} is a $1V_{P-P}$ sinewave, then $I/Q_{IN}+$ is a $1.0V_{P-P}$ sinewave riding on a positive voltage equal to V_{DC}. The converter will be at positive full scale when $I/Q_{IN}+$ is at V_{DC} + 0.5V ($I/Q_{IN}+ - I/Q_{IN}- = +0.5V$) and will be at negative full scale when $I/Q_{IN}+$ is equal to V_{DC} - 0.5V ($I/Q_{IN}+ - I/Q_{IN}- = -0.5V$). Sufficient

headroom must be provided such that the input voltage never goes above +3V or below AGND. In this case, V_{DC} could range between 0.5V and 2.5V without a significant change in ADC performance. The simplest way to produce VDC is to use the I/Q_{VRIN} bias source, I/QV_{DC}, output of the ISL5640.

The single ended analog input can be DC coupled (Figure 7) as long as the input is within the analog input common mode voltage range.

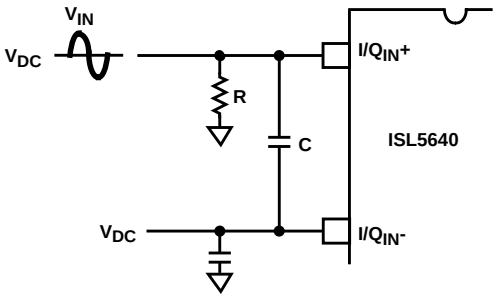


FIGURE 7. DC COUPLED SINGLE ENDED INPUT

The resistor, R, in Figure 7 is not absolutely necessary but may be used as a load setting resistor. A capacitor, C, connected from $I/Q_{IN}+$ to $I/Q_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

A single ended source may give better overall system performance if it is first converted to differential before driving the ISL5640.

Operational Mode

The ISL5640 contains several operational modes including a normal two channel operation, placing one or both channels in standby and delaying the Q channel data 1/2 clock cycle. The operational mode is selected via the S1 and S2 pins and is asynchronous to either clock. When either channel is placed in standby, the output data is stalled and not high impedance. When recovering from standby, valid data is available after 20 clock cycles.

The delay mode can be used to set the Q channel 180 degrees out phase of the I channel if the same clock is driving both channels. If separate, inverted clocks are used for the I and Q channels, this feature can be used to align the data.

OPERATIONAL MODES

S1	S2	MODE
0	0	Standby I and Q Channels.
0	1	I channel operates normally with Q Channel in standby mode.
1	0	I and Q Channels operating with I/Q output data in phase.
1	1	I and Q Channels operating with Q data 180 degrees out of phase.

Sampling Clock Requirements

The ISL5640 sampling clock input provides a standard high-speed interface to external TTL/CMOS logic families.

In order to ensure rated performance of the ISL5640, the duty cycle of the clock should be held at 50% ±5%. It must also have low jitter and operate at standard TTL/CMOS levels.

Performance of the ISL5640 will only be guaranteed at conversion rates above 1MSPS (Typ). This ensures proper performance of the internal dynamic circuits. Similarly, when power is first applied to the converter, a maximum of 20 cycles at a sample rate above 1MSPS must be performed before valid data is available.

Supply and Ground Considerations

The ISL5640 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the ISL5640 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply can be isolated by a ferrite bead from the digital supply.

Refer to the application note “Using Intersil High Speed A/D Converters” (AN9214) for additional considerations when using high speed converters.