MCRF450/451/452/455

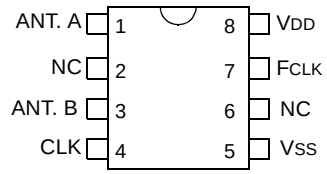
13.56 MHz Read/Write Passive RFID Device

FEATURES

- Contactless read and write
- 1024 bits (32 blocks) of total memory
- 864 bits of user programmable memory
- User controlled write protection of each block
- Manchester coding protocol with CRC for reading
- 70 kHz data rate
- RF field gaps and 1-of-16 PPM with CRC for writing
- High speed deterministic anti-collision algorithm for reading and writing virtually any number of tags in the same RF field
- Three pads for external antenna circuit (MCRF450, 451, 455)
- Two pads for external antenna (MCRF452)
- Internal resonance capacitors (MCRF451, 452, 455)
- Factory programmed unique 32-bit tag ID
- Interrogator talks first (ITF) or tag talks first (TTF) operation
- Fast and normal modes for data transmission
- Anti-tearing feature for secure write transactions
- Full 32-bit EAS support
- Very low power CMOS design
- Die, wafer, bumped wafer, PDIP, or SOIC package options
- Asynchronous operation for low power/extended read range

PACKAGE TYPES

PDIP/SOIC

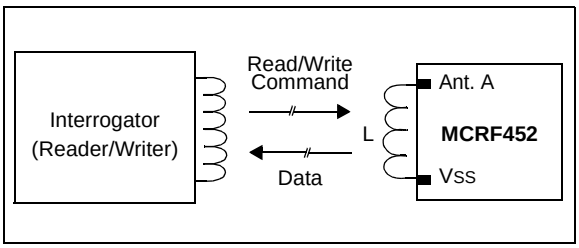


DESCRIPTION

The MCRF45X is a contactless read/write passive RFID device that is optimized for 13.56 MHz RF carrier signal. The device needs an external LC resonant circuit to communicate with interrogator wirelessly. The device is powered remotely by rectifying an RF signal that is transmitted from the interrogator, and transmits or updates its contents of memory based on commands from the interrogator.

The device is engineered to be used effectively for item level tagging applications such as retail and inventory management, where a large volume of tags are read and written in the same interrogator field.

APPLICATION



The device contains 32 blocks of EEPROM memory. Each block consists of 32 bits. The first three blocks (B0 - B2: 96 bits) are allocated for device operation, the next 27 blocks (B3 - B29: 864 bits) are for user data, and the remaining 2 blocks (B30 - B31: 64 bits) are reserved for future use. The 864 (B3 - B29) user bits are contactlessly read or written block-wise by interrogator commands. All blocks except bits 30 and 31 in block 0 are write protectable.

The device has two operational modes depending on the conditions of talk first (TF) and fast read (FR) bits. These modes are: “tag talks first” (TTF) and “interrogator talks first” (ITF) modes. The device operates in TTF mode if both TF and FR bits are set. In this mode, the device transmits its fast read response data (96 bits in default) as soon as it is energized, and waits for the next commands. The device operates in the “interrogator talks first” mode, if the TF bit is cleared. In this mode, the device requires an interrogator command before it sends any data.

The device uses an internal oscillator for data timing of the read operation. The data rate for reading is 70 kHz and uses Manchester format. The communication between the interrogator and the device takes place asynchronously.

The interrogator sends commands to the device by amplitude modulating its RF carrier signal. 1-of-16 Pulse Position Modulation (PPM) and specially timed gap pulses are used for the modulation of the carrier signal. The device includes a detection circuit to detect these interrogator commands.

To enhance the detection accuracy in the device, the interrogator sends a time reference signal (time calibration pulse) to the device followed by the command and programming data. The time reference signal is used to calibrate timing of the internal decoder of the device.

Depending on the metal mask options, the device includes internal resonant capacitor between antenna A and VSS pads: (a) no internal resonant capacitor for the MCRF450, (b) 100 pF for the MCRF451, (c) two 50 pF in series (25 pF in total) for the MCRF452, and (d) 50 pF for the MCRF455. The internal resonant capacitor for each metal mask option is shown in Figures 1-2 through 1-5.

The MCRF450 needs an external LC resonant circuit that is connected between antenna A, antenna B, and VSS pads. See Figure 1-2 for the external circuit configuration. The MCRF452 needs a single external antenna coil only between antenna A and VSS pads as shown in Figure 1-4.

This external circuit along with the internal resonant capacitor must be tuned to the carrier frequency of the interrogator for maximum performance.

When a tag (device with the external LC resonant circuit) is brought to the interrogator’s RF field, it develops an RF voltage across the external circuit. The device rectifies the RF voltage and develops a DC voltage (VDD). The device becomes functional as soon as VDD reaches the operating voltage level.

The device sends data to the interrogator by turning on/off the internal modulation transistor. This internal modulation transistor is located between antenna B and VSS. The modulation transistor has very small turn-on resistance between Drain (antenna B) and Source (VSS) terminals during its turn-on time.

When the modulation transistor turns-on, the resonant circuit component between antenna B and VSS, that is in parallel with the modulation transistor, is shorted due to the low turn-on resistance. This results in a change of the LC value of the circuit. As a result, the circuit no longer resonates at the carrier frequency of the interrogator. Therefore, the voltage across the circuit is minimized. This condition is called cloaking.

When the modulation transistor turns-off, the circuit resonates at the carrier frequency of the interrogator, and develops maximum voltage. This condition is called uncloaking. Therefore, the data is sent to the interrogator by turning-on (cloaking) and off (uncloaking) the modulation transistor.

Therefore, the voltage amplitude of the carrier signal across the LC resonant circuit changes depending on the amplitude of modulation data (cloaking for logic “Hi” level and uncloaking for logic “Lo” level). This is called amplitude modulation signal. The receiver channel in the Interrogator detects this amplitude modulation signal and reconstructs the modulation data for decoding.

The device includes a unique anti-collision algorithm to be read or written effectively in multiple tag environments. To minimize data collision, the algorithm utilizes time division multiplexing of the device response. Therefore, each device can communicate with the interrogator in a different time slot. The devices in the interrogator’s RF field remain in a non-modulating condition if they are not in the given time slot. This enables the interrogator to communicate with the multiple devices one at a time without data collision. The details of the algorithm are described in Section 4.0.

To enhance data integrity for writing, the device includes an anti-tearing feature. This anti-tearing feature provides verification of data integrity for incomplete write cycles due to failed communication from the interrogator to the device during the write sequences.

1.0 ELECTRICAL CHARACTERISTICS

TABLE 1-1: ABSOLUTE RATINGS

Parameters	Symbol	Min.	Max.	Units	Conditions
Coil current into coil pad	I_{PP_AC}	—	40	mA	Peak-to-Peak coil current
Maximum power dissipation	P_{MPD}	—	1	W	
Ambient temperature with power applied	T_{AMB}	-40	125	°C	
Assembly temperature	T_{ASM}	—	300	°C	< 10 Sec
Storage temperature	T_{STORE}	-65	150	°C	

Note: Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-2: DC CHARACTERISTICS

All parameters apply across the specified operating ranges, unless otherwise noted.	Commercial (C): Tamb = -20°C to 70°C					
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Reading voltage	V_{DDR}	2.4	—	—	V	V_{DD} voltage for reading at 25°C
Operating current in normal mode	I_{OPER_N}	—	7	10	µA	V_{DD} = 2.4V during reading at 25°C
Operating current in fast mode	I_{OPER_F}	—	TBD	—	µA	V_{DD} = 2.4V during reading at 25°C
Writing current	I_{WRITE}	—	—	50	µA	At 25°C
Writing voltage	V_{WRITE}	2.4	—	—	V_{DC}	At 25 °C
Modulation resistance	R_M	—	3	4	Ω	DC turn-on resistance between Drain and Source terminals of the modulation transistor

TABLE 1-3: AC CHARACTERISTICS

All parameters apply across the specified operating ranges, unless otherwise noted.	Commercial (C): Tamb = -20°C to 70°C					
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Carrier frequency	FC	—	13.56	—	MHz	
Coil voltage during reading	VPP_AC	4	—	—	VPP	Peak-to-Peak AC voltage across the coil during reading
Internal Resonant Capacitor	CRES_100	85	100	115	pF	Between Ant. A and VSS pads at 13.56 MHz and at 25°C, MCRF451
Internal Resonant Capacitor	CRES_2_50A	42.5	50	57.5	pF	Between Ant. A and B pads at 13.56 MHz and at 25°C, MCRF452
Internal Resonant Capacitor	CRES_2_50B	42.5	50	57.5	pF	Between Ant. B and VSS pads at 13.56 MHz and at 25°C, MCRF452
Internal Resonant Capacitor	CRES_50	42.5	50	57.5	pF	Between Ant. A and VSS pads at 13.56 MHz and at 25°C, MCRF455
Coil detuning voltage	VDETUNE	—	TBD	—	VPP	Coil voltage at which the limiting circuit becomes active
Interrogator data (ITD) rate_normal	FITD_NORM	—	1.4286	—	kHz	
Interrogator data (ITD) rate_fast	FITD_FAST	—	25	—	kHz	
Device data rate	FDVD	58	70	82	kHz	Both normal and fast modes
Modulation depth of 1-of-16 PPM	MDEPTH_PPM	—	100	—	%	
Pulse width of 1-of-16 PPM for normal mode	PWPPM_N	—	175	—	µs	See Figure 4-2 and Table 4-7 for details.
Pulse width of 1-of-16 PPM for fast mode	PWPPM_F	—	10	—	µs	See Figure 4-2 and Table 4-7 for details.
Symbol width of 1-of-16 PPM for normal mode	SWPPM_N	—	2.8	—	ms	
Symbol width of 1-of-16 PPM for fast mode	SWPPM_F	—	160	—	µs	
Gap pulse width of Fast Read command	GPW_FR	—	175	—	µs	See Figure 4-3 and Table 4-7 for details.
EEPROM (Memory) Writing Time	TWRITE	—	5	—	ms	At 20°C, write time for a 32-bit block.
Command Decode Time	TDECODE	—	TBD	—	µs	Time delay between end of command symbol and start of the device response.
Time slot	TSLOT		2.5	2.925	ms	
Listening Window	TLW	TBD	1	TBD	ms	
Modulation depth of Fast Read command	MDEPTH_FRR	—	100	—	%	
Command Duration of Fast Read command (FRR and FRB)	T_CMD_FRR	—	1.575	—	ms	175 ms/pulse position x 9 pulse positions = 1.575 ms

TABLE 1-3: AC CHARACTERISTICS

All parameters apply across the specified operating ranges, unless otherwise noted.	Commercial (C): Tamb = -20°C to 70°C					
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input impedance A	Zin_A	—	TBD	—	Ω	Input impedance between antenna pad A and VSS, at 13.56 MHz with modulation transistor off (no external coils)
Input impedance B	Zin_B	—	TBD	—	Ω	Input impedance between antenna pad B and VSS, at 13.56 MHz with modulation transistor off (no external coils)
Data retention	—	200	—	—	Years	For T < 120°C
Endurance	—	1	—	—	Million Cycles	At 25°C

Note: Writing time starts at the end of the last command symbol.

TABLE 1-4: PAD COORDINATES (MICRONS)

Pad Name	**Lower Left X**	**Lower Left Y**	**Upper Right X**	**Upper Right Y**	**Passivation Openings**		**Pad Center X**	**Pad Center Y**
					Pad Width	**Pad Height**		
Ant. Pad A	-853.50	-953.90	-764.50	-864.90	89.00	89.00	-809.00	-909.40
Ant. Pad B	759.50	-955.50	848.50	-866.50	89.00	89.00	804.00	-911.00
VSS	769.10	939.70	858.10	1028.70	89.00	89.00	813.60	984.20
VDD	-839.50	83.70	-750.50	172.70	89.00	89.00	-795.00	128.20
CLK	721.10	116.00	810.10	205.00	89.00	89.00	765.60	160.50
FCLK	-821.50	872.50	-732.50	961.50	89.00	89.00	-777.00	917.00

Note 1: All coordinates are referenced from the center of the die. The minimum distance between pads (edge to edge) is 10 mil.

2: Unsawed die size = 74.96 mil x 89.15 mil.

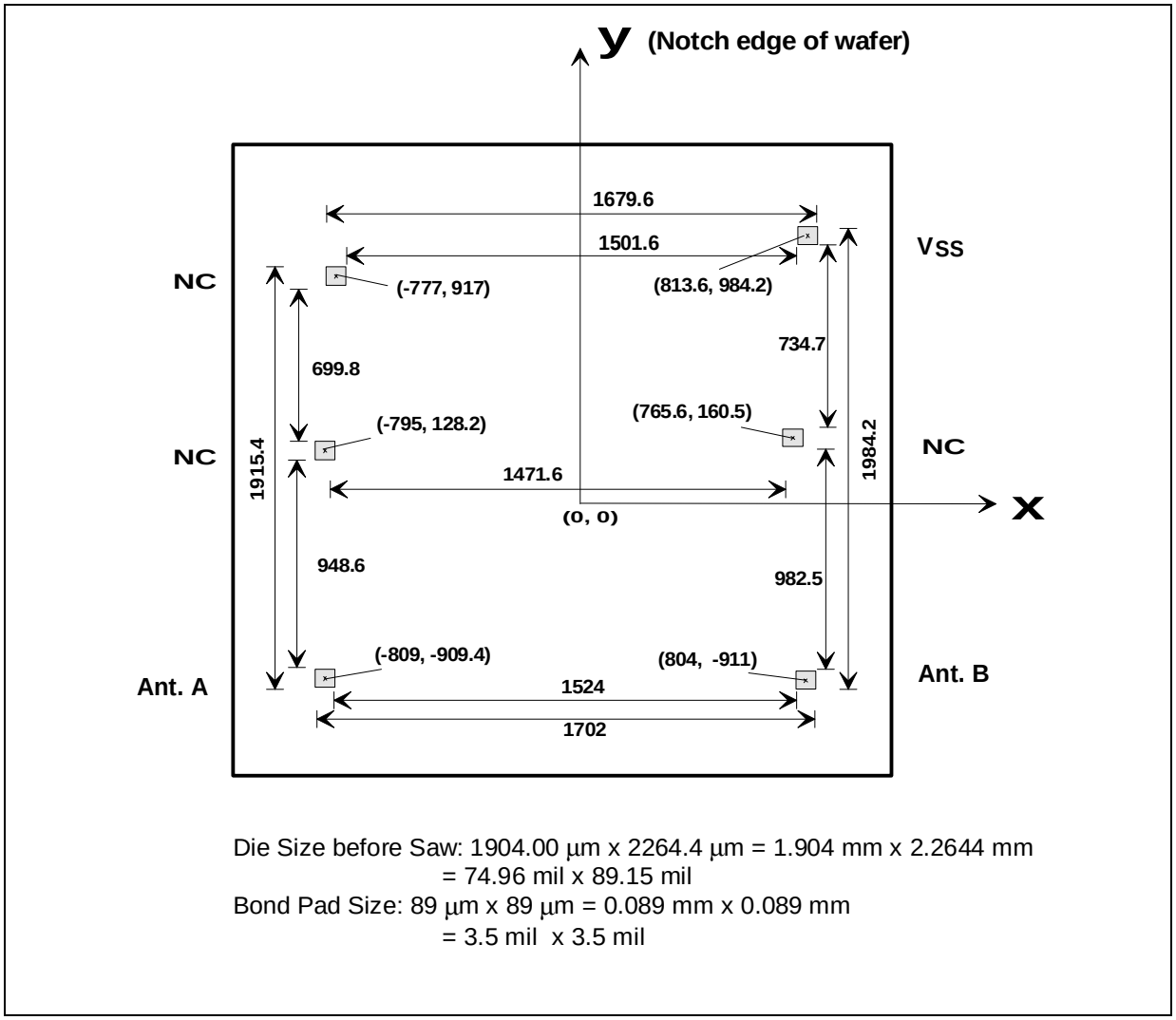
TABLE 1-5: DIE MECHANICAL DIMENSIONS

Specifications	Min.	Typ.	Max.	Unit	Comments
Bond pad opening	— —	3.5 x 3.5 89 x 89	— —	mil µm	**Note 1, Note 2**
Die backgrind thickness	— —	7 177.8	— —	mil µm	Sawed 8” wafer on frame (option = WF) **(Note 3)**
	— —	11 279.4	— —	mil µm	• Bumped, sawed 8” wafer on frame (option = WFB) • Unsawed wafer (option = W) • Unsawed 8” bumped wafer (option = WB), **(Note 3)**
Die backgrind thickness tolerance	— —	— —	±1 ±25.4	mil µm	**Note 4**
Die passivation thickness (multilayer)	—	0.9050	—	µm	**Note 5**
Die Size: Die size X*Y before saw (step size) Die size X*Y after saw	 — —	 74.96 x 89.15 73.39 x 87.58	 — —	 mil mil	

Note 1: The bond pad size is that of the passivation opening. The metal overlaps the bond pad passivation by at least 0.1 mil.
2: Metal Pad Composition is 98.5% Aluminum with 1% Si and 0.5% Cu.
3: As the die thickness decreases, susceptibility to cracking increases. It is recommended that the die be as thick as the application will allow.
4: This specification is not tested. For design guidance only.
5: The Die Passivation thickness can vary by device depending on the mask set used.
6: The conversion rate is 25.4 µm/mil.

Notice: Extreme care is urged in the handling and assembly of die products since they are susceptible to mechanical and electrostatic damage.

FIGURE 1-1: MCRF450/451/452/455 DIE LAYOUT



Die Size before Saw: 1904.00 µm x 2264.4 µm = 1.904 mm x 2.2644 mm
= 74.96 mil x 89.15 mil
Bond Pad Size: 89 µm x 89 µm = 0.089 mm x 0.089 mm
= 3.5 mil x 3.5 mil

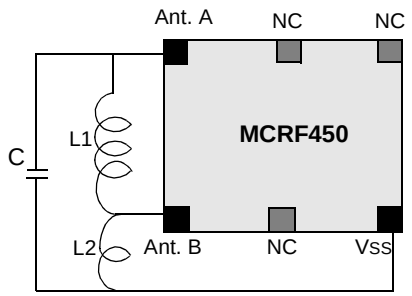
TABLE 1-6: PAD FUNCTION TABLE

Name	Function
Ant. Pad A	Connected to antenna coil L1
Ant. Pad B	Connected to antenna coils L1 and L2 (450/451/455), NC for 452
VSS	Connected to antenna coil L2 Device ground during test mode, **(Note 1)**
NC	Not connected, **(Note 2)**

Note 1: Substrate = VSS

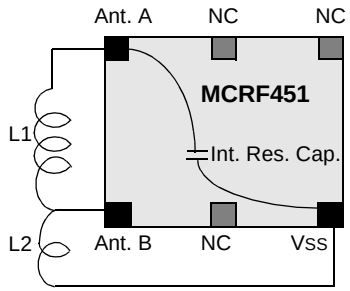
2: Leave floating or connect to VSS

FIGURE 1-2: MCRF450



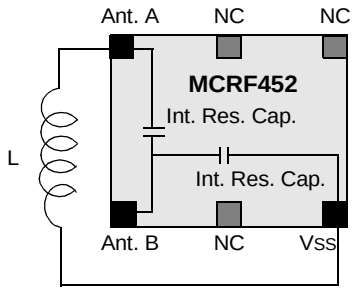
L1: External Antenna Coil A
L2: External Antenna Coil B
C: External Capacitor
NC: Not connected
Note: Substrate = VSS

FIGURE 1-3: MCRF451



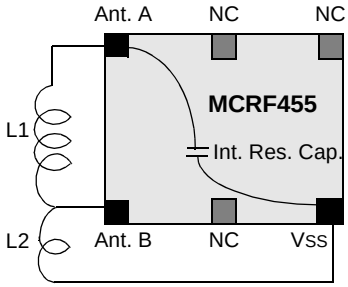
Internal Resonant Capacitor (CRES_100) = 100 pF
L1: External Antenna Coil A
L2: External Antenna Coil B
NC: Not connected
Note: Substrate = VSS

FIGURE 1-4: MCRF452



Internal Resonant Capacitor between Ant. A and Ant. B pads (CRES_2_50A) = 50 pF
Internal Resonant Capacitor between Ant. B and Vss pads (CRES_2_50B) = 50 pF
NC: Not connected
L: External Antenna Coil
Note: Substrate = VSS
Total Internal Resonant Capacitance = 25pF

FIGURE 1-5: MCRF455



Internal Resonant Capacitor (CRES_50) = 50 pF
L1: External Antenna Coil A
L2: External Antenna Coil B
NC: Not connected
Note: Substrate = VSS

2.0 BLOCK DIAGRAM

The device contains four major sections. They are: Analog Front-End, Detection/Encoding, Read/Write Anti-collision, and Memory sections. Figure 2-1 shows the block diagram of the device.

2.1 ANALOG FRONT-END SECTION

This section includes high and low voltage regulators, power-on-reset, 70 kHz clock generator, and modulation circuits.

2.1.1 HIGH AND LOW VOLTAGE REGULATOR

The high voltage circuit generates the programming voltage for the memory section. The low voltage circuit generates DC voltage (V_{DD}) to operate the device.

2.1.2 POWER ON RESET (POR)

This circuit generates a power-on-reset voltage. The reset releases when sufficient power has been developed by the voltage regulator to allow for correct operation.

2.1.3 CLOCK GENERATOR

This circuit generates a clock (CLK). The main clock is generated by an on-board 70 kHz time base oscillator. This clock is used for all timing in the device except for the fast mode PPM decoding.

2.1.4 DATA MODULATION

The data modulation circuit consists of a modulation transistor and an resonant LC resonant circuit. The resonant circuit must be tuned to the carrier frequency of the interrogator (i.e., 13.56 MHz) for maximum performance.

The modulation transistor is placed between antenna B and Vss pads, and is designed to result in the turn-on resistance of less than four ohms (R_M). This small turn-on resistance shorts the resonant circuit component between the antenna B and V_{SS} pads as it turns on. This results in a change of the resonant frequency of the resonant circuit. As a result, the resonant circuit becomes detuned to the carrier frequency of the interrogator. The voltage across the resonant circuit is minimized during this time. This condition is called “cloaking”.

The transistor, however releases the resonant circuit as it turns off. Therefore, the resonant circuit tunes to the carrier frequency of the interrogator again, and develops maximum voltage. This condition is called “uncloaking”.

The device transmits data by cloaking and uncloaking based on the on/off condition of the modulation transistor. Therefore, with the 70 kHz - Manchester format, the data bit “0” will be sent by cloaking and uncloaking the device for 7 µs each. Similarly, the data bit “1” will be sent by uncloaking and cloaking the device for 7 µs each. See Figure 4-1 for the Manchester waveform.

2.1.5 DETUNING CIRCUIT

The purpose of this circuit is to prevent excessive RF voltage across the resonant circuit.

This circuit monitors V_{DD} and detunes the resonant circuit if the RF coil voltage exceeds the threshold limit (V_{DETUNE}) which is above the operating voltage of the device.

FIGURE 2-1: BLOCK DIAGRAM

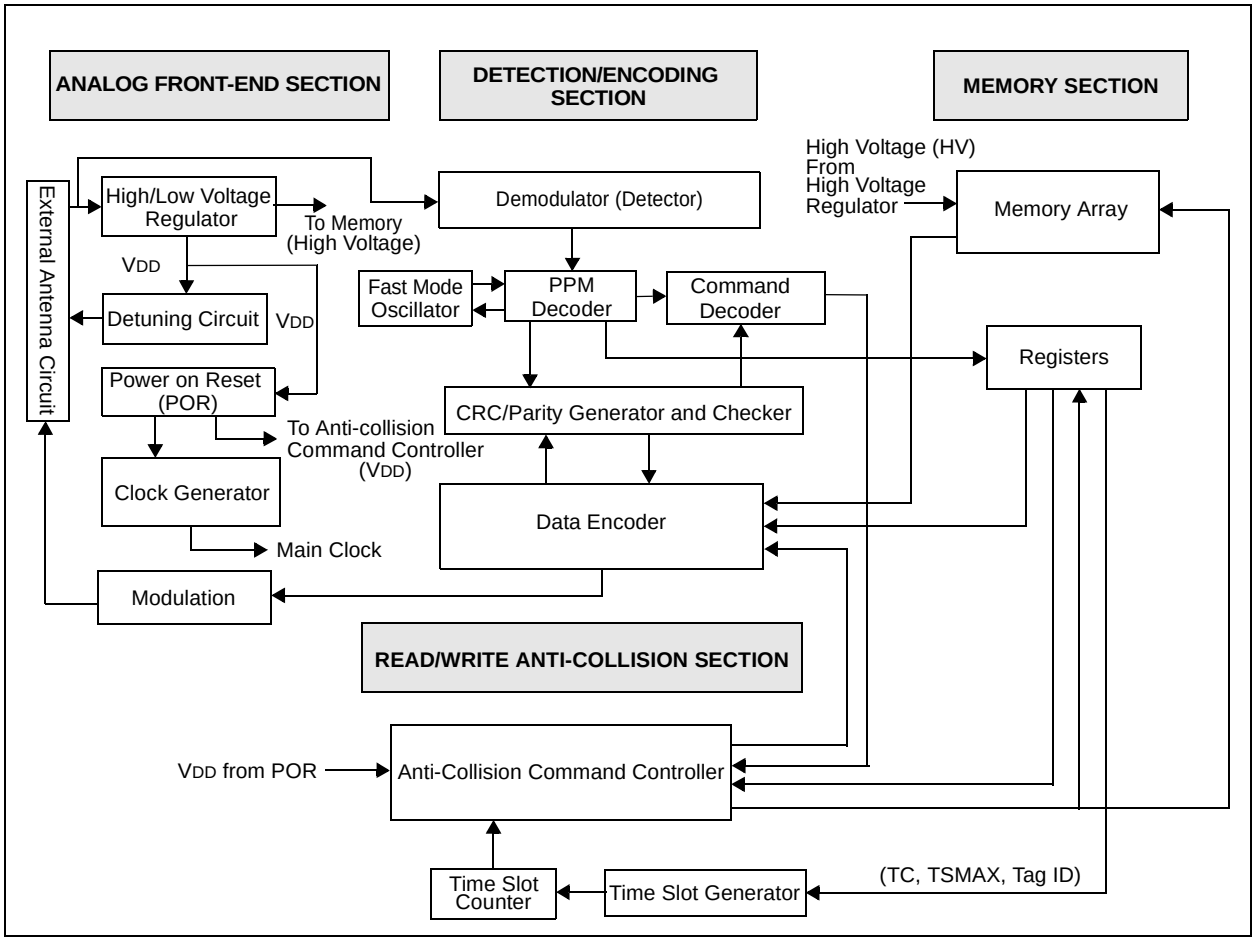
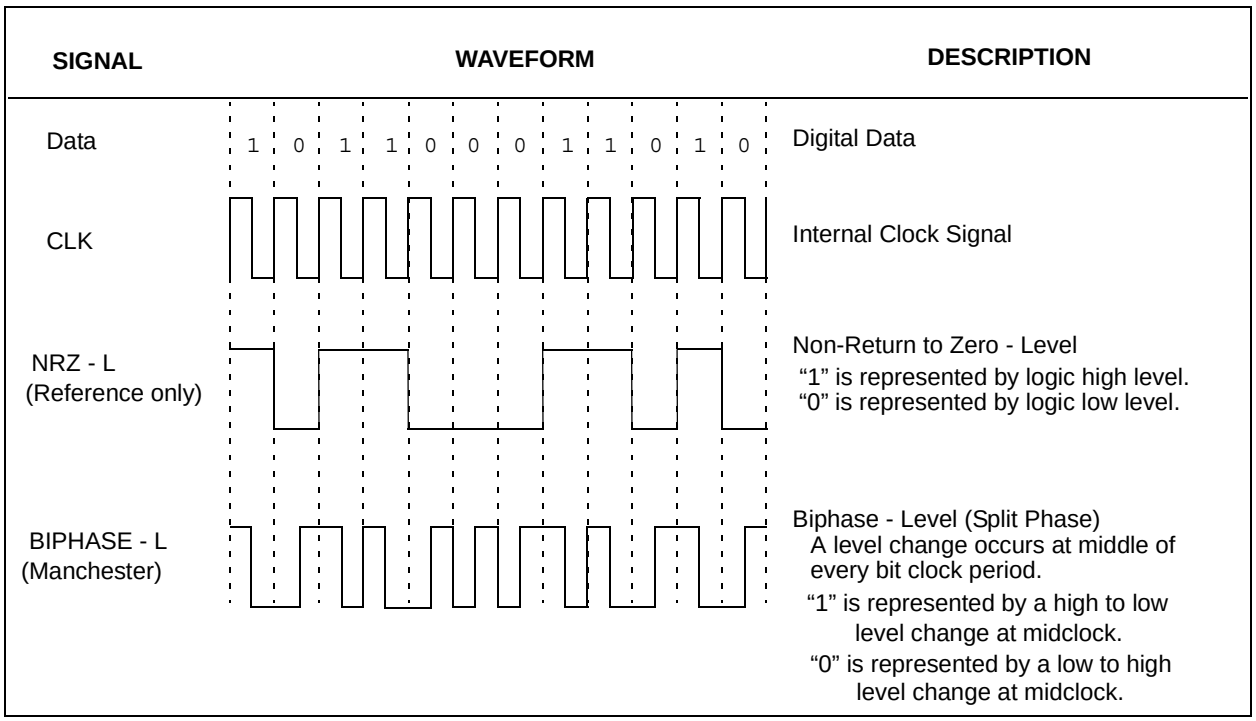


FIGURE 2-2: DATA WAVEFORM OF DEVICE



3.0 DETECTION AND ENCODING SECTION

This section encodes data with the Manchester format and also detects commands from the interrogator.

3.1 Demodulator (Detector)

This circuit demodulates the interrogator commands, and sends them to the Pulse Position Modulation (PPM) decoder.

3.2 Fast Mode Oscillator

This oscillator generates a clock that is used for decoding fast mode commands.

3.3 PPM Signal Decoder

This section decodes the PPM signals, and sends the results to both the command decoder and CRC/parity checker.

3.4 Command Decoder

This section decodes the interrogator commands and sends the results to the anti-collision/command controller.

3.5 CRC/Parity Generator and Checker

This section generates CRC and parity bits for transmitting and receiving data. The device utilizes a 16 bit cyclic redundancy code (CRC) for error detection. Its polynomial and initial values are:

CRC Polynomial: $X^{16}+X^{12}+X^5+X^0$

Initial Value: $FFFF

This polynomial is also known as CRC CCITT (Consultative Committee for International Telegraph and Telephone). The interrogator also uses the same CRC for data processing. The device uses the CRC in the following ways:

1. **Normal case:** The interrogator will send a write command with CRC. When the device receives the command, it checks the CRC prior to any processing. If it is a correct CRC, the device programs the block data and also stores the CRC in the EEPROM. As soon as the data is written in the memory, both the programmed data and stored CRC (SCRC) are sent back to the interrogator as a verification. The device also sends both the programmed data and stored CRC (SCRC) when as a response to the read command.

   If the CRC is incorrect, the device ignores the incoming message (does not respond to the interrogator) and waits for the next command with a correct CRC.

2. **Special Case 1:** When reading block 0 or 2, a calculated CRC (CCRC) is sent. This is because both the TF and FR bits in the block 0 are non-write protectable while the rest of the bits in the block are write protectable. This means the stored CRC (SCRC) in the block no longer represents the CRC of the block data if only the TF or the FR bit is reprogrammed. This is also true for block 2 which is a write protection block: The write protected bit can not be reprogrammed once it has been written. Therefore, the stored CRC in these blocks (0 and 2) are not used. Instead, the device calculates the current CRC of the block and sends it to the interrogator.
3. **Special Case 2:** For the Fast Read (FR) response (this is the device response to an FRR command), bits 0-15 (FRR_CRC) in block 0 are sent as the CRC of the fast read field (FRF: blocks 3-5). See Table 4-3 for device responses.

3.6 Data Encoder

This section multiplexes serial data, encodes it into Manchester format, and sends it to the modulation circuit. See Figure 2-2 for the Manchester waveform.

4.0 READ/WRITE ANTI-COLLISION LOGIC

This section includes the anti-collision algorithm of the device, and consists of the anti-collision/command controller, the time slot counter, and the time slot generator.

4.1 Description of Algorithm

The read and write anti-collision algorithm is based on time division multiplexing of tag responses. Each device is allowed to communicate with the interrogator in its time slot only. When not in its assigned time slot, the device remains in a non-modulating condition. This enables the interrogator to communicate with other devices in the same interrogator field with fewer chances of data collision.

Figure 4-1 shows the anti-collision algorithm flowchart, which consists of four control loops. They are: Detection, Processing, Sleeping, and Reactivation loops. All devices in the interrogator's RF field are controlled by five different commands and internal control flags.

The interrogator commands are:

1. **Fast Read Request (FRR):** If the TF bit of the device is cleared, then it will respond to only this command from the interrogator. This command consists of five specially timed gap pulses. See Figs. 4-3 to 4-8. The position of the five gap pulses in the given time span (1.575 ms) determines the parameters of the command. The command has three parameters: TCMAX, TSMAX, and Data transmission speed. The details of these parameters will be discussed in the following sections. If the device receives the FRR command, it sends the fast read (FR) response (96 bits in default) and then listens for 1 ms (T_{LW}) for a matching code from the interrogator.
2. **Fast Read Bypass (FRB):** This command is used in the Reactivation loop. This command is only applicable to a device with the fast read bit (FR bit: bit 31 in block 0) cleared. The device responds with 64 bits of data which includes block 1 data (32-bit Tag ID), and then listens for 1 ms (T_{LW}) for a matching code from the interrogator. The command structure is the same as the FRR command: Five specially timed gap pulses (1.575 ms). The command parameter (see Figure 4-8) determines the data rate (normal speed or fast speed) of subsequent interrogator commands.
3. **Matching Code 1 (MC1):** This command consists of time calibration pulses (TCP) followed by 1-of-16 PPM signals. It is used when the device does not need any further processing. This MC1 command causes a device which is in the Detection loop to enter the Sleeping loop.
4. **Matching Code 2 (MC2):** The command structure is the same as MC1: TCP followed by 1-of-16 PPM signals. The command is used when the device needs further processing (read/write). The device enters the Processing loop if it receives this command in the Detection loop.

   The matching code (MC1 and MC2) command consists of 12 bits (or 3 symbols). The first 8 bits (or the first two symbols) are selected from the 32-bit Tag ID. The next 4 bits (or the 3rd symbol) determine the matching code type (3 bits) and a parity bit (see Section 4.2.3.6). The command lasts for about 11.2 ms including the time calibration pulses.
5. **End Process (EP):** This command consists of the time reference pulses followed by 1-of-16 PPM signals. The EP command causes a device to exit the Processing loop and enter the Sleeping loop.

4.1.1 DETECTION LOOP

The device can enter this loop in two ways if the fast read (FR: bit 31 of block 0) bit is set. The two ways depend on the condition of the talk-first (TF: bit 30 of block 0) bit. They are: (1) If the TF bit is cleared, the device enters this loop and waits for a fast read request (FRR) command. This is called "interrogator talks first" (ITF) mode. (2) If the TF bit is set, the device enters this loop by transmitting the fast read (FR) response without waiting for an FRR command. This case (2) is called "tag talks first" (TTF) mode.

For case (1) above, the parameters of the FRR are:

(a). Maximum number of time slots (TSMAX=1, 16, or 64),

(b). Maximum transmission counter (TCMAX = 1, 2, or 4), and

(c). Data transmission speed (normal or fast mode).

The purpose of the TCMAX and TSMAX parameters is to acknowledge the device in the Detection loop as fast as possible. TSMAX represents the maximum number of time slots between the end of the FRR command and the beginning of the fast read (FR) response. One time slot (T_{SLOT}) represents 2.5 ms. For example, TSMAX=64 represents a maximum of 160 ms of time delay before sending the FR response. See Section 4.2.4 for the calculation of actual time delay. TCMAX represents the maximum number of fast read (FR) responses a device can send after an FRR command. For example, TCMAX=4 means the device can send its FR response four times (after the FRR command) for acknowledgment (matching code).

The TSMAX and TCMAX values are determined by the interrogator's decision on how many tags are in the field. The interrogator may assign TSMAX=1 and TCMAX = 1 assuming there is only one tag in the field. The efficiency of the detection will increase in multiple

tag environments by assigning a higher number to both the TSMAX and TCMAX. If the device receives the FRR, it clears the Position 1 flag, waits for its time slot and replies with the fast read (FR) response and then listens for 1 ms. The FR response consists of a maximum of 160 manchester data bits (default: 96 bits, see Table 4-3 and Example 7-1) which includes the 32-bit Tag ID and the fast read field data (blocks 3-5).

To acknowledge the FR response, the interrogator can start to send a matching code (MC) during the device's 1 ms listening window (T_{LW}). The MC is encoded with 1-of-16 PPM signal. See Figure 4-9 for the 1-of-16 PPM signal. The MC1 is given to the device if the device does not need any further processing. If the device receives the MC1, it enters the Sleeping loop and stays in the loop in a non-modulating condition. The MC2 command is given to the device if further processing (read/write) is required. If the device receives the MC2 command, it enters the Processing loop.

If the device misses the MC within the listening window, it sends the FR response again after its time slot if two conditions are met: (1) Position 1 flag is cleared and (2) TCMAX has not elapsed. The device checks the condition (elapsed or not elapsed) of TCMAX using an internal transmission counter (TC). The transmission counter (TC) consists of 3 bits. If the Position 1 flag is cleared, the device increments the TC by 1 each time it does not receive a MC during its listening window. See the flow chart in Figure 4-1 for the conditional increment of the transmission counter. Table 4-1 shows an example of detecting the elapsed TCMAX using a rolling modulo-8 transmission counter.

For the TTF case, the device repeats its FR response according to the TCMAX and TSMAX parameters as specified in Table 5-5. Even though the device is operating in TTF mode, it will respond to its correct MC during its listening window. If TCMAX = 1, 2, or 4, it will also respond to FRR commands just as in the ITF case (see Section 4.1.1.1).

4.1.1.1 Matching Code Queuing

Once the device receives the FRR command, it sends the FR response and waits for a matching code (MC) during its listening window. If the device does not receive its correct MC code before its TCMAX has elapsed (see Table 4-1), it goes back to the beginning of the Detection loop (position 1 in the loop), and waits for either a new FRR command or matching code (MC1 or MC2). This is called "matching code queuing". In this queuing, the device stays in the Detection loop waiting for an interrogator command (FRR or MC). This queuing takes place within the Detection loop and is controlled by the conditions of Set Position 1 Flag and TCMAX.

This queuing allows the interrogator to communicate with a device outside its listening window. The result is enhanced and accelerated processing of individual devices in a multiple tag environment.

TABLE 4-1: CONDITIONS FOR TCMAX = ELAPSED FOR ITF MODE

Rolling Modulo -8 TC			TCMAX = 1	TCMAX = 2	TCMAX = 4
0	0	1	elapsed	—	—
0	1	0	elapsed	elapsed	—
0	1	1	elapsed	—	—
1	0	0	elapsed	elapsed	elapsed
1	0	1	elapsed	—	—
1	1	0	elapsed	elapsed	—
1	1	1	elapsed	—	elapsed
0	0	0	elapsed	elapsed	—

4.1.2 PROCESSING LOOP

The reading and writing processes take place in this loop. Devices in this loop are waiting for commands for processing. In order to read from or write to the device, its "Processing Flag" (PF) must be set. Any device entering this loop with its PF cleared is called a follow-along tag. This follow-along tag in the loop is not processed for reading or writing.

If the device with PF set receives the End process (EP) command, it exits this loop and enters the Sleeping loop. However, the same EP command sends the follow-along tag back to the Detection loop.

If the device receives the FRR or FRB command in this loop, it sees the command as invalid, resets itself, and goes back to the initial power up state.

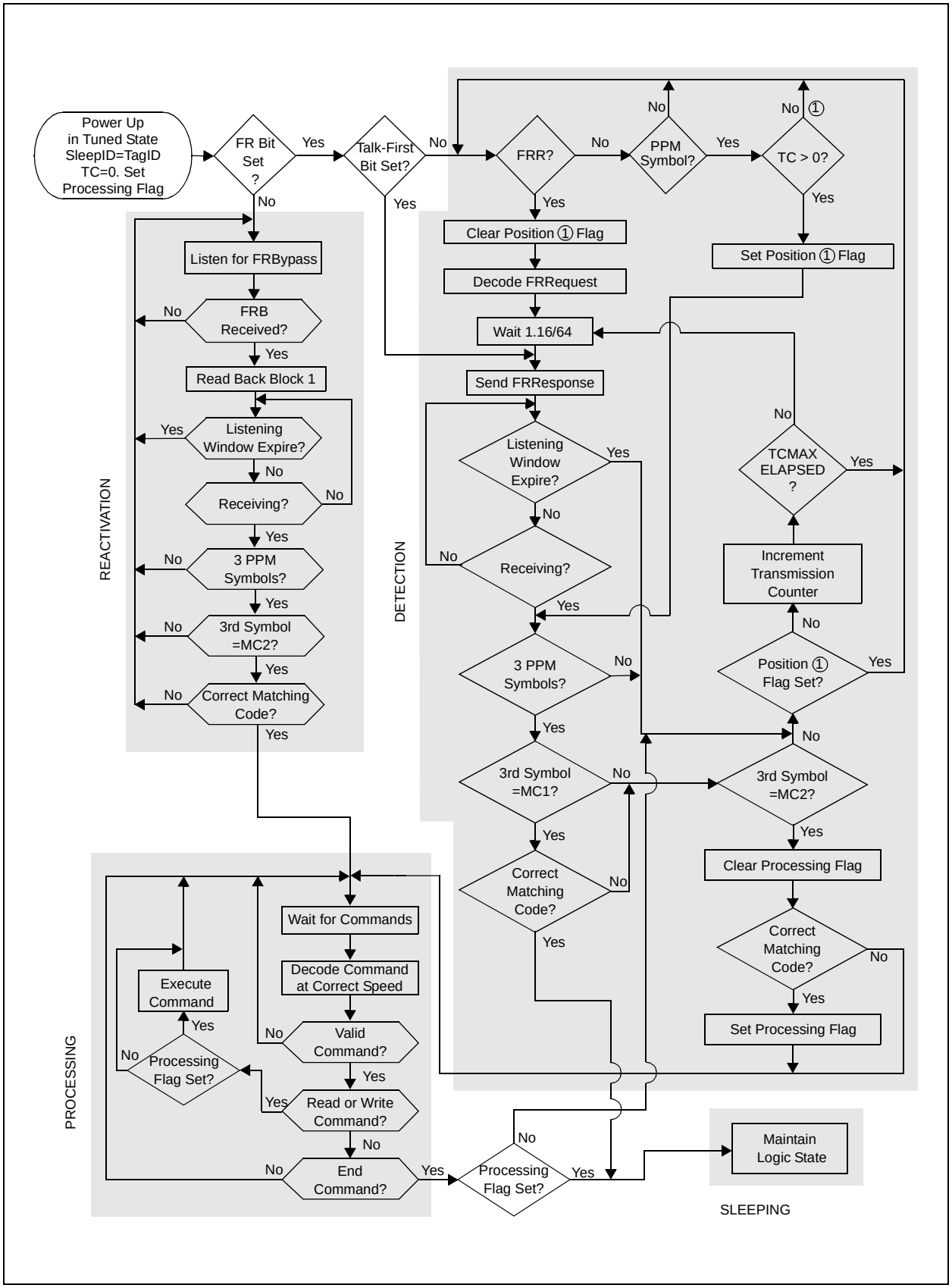
4.1.3 SLEEPING LOOP

This loop is used to keep all processed devices in a "silent" condition. The devices stay in this loop in a non-modulating condition as long as they remain in the field.

4.1.4 REACTIVATION LOOP

This loop is used to process a device with its fast read (FR) bit cleared. A device in this loop waits for the fast read bypass (FRB) command. If a device receives the FRB, it transmits the contents of block 1 (Tag ID) in its memory and waits for matching code 2 (MC2) in its listening window. If the device in this loop receives matching code 2 (MC2), it leaves this loop and enters the Processing loop. This reactivation loop has no anti-collision capability; it is designed for reactivation of single devices. This loop can be effectively used in retail store applications to process returning items from customers.

FIGURE 4-1: ANTI-COLLISION FLOW CHART



4.2 Anti-Collision Command Controller

This section manages the anti-collision algorithm and establishes the communications between the interrogator and device.

4.2.1 STRUCTURE OF READ/ WRITE COMMAND SIGNALS

The interrogator's read/write commands have the following structure:

Read/Write command = Command + Address + Data + Parity (or CRC)

The commands are summarized in the table below:

TABLE 4-2: READ/WRITE COMMANDS FROM INTERROGATOR TO DEVICE

Interrogator Command	Command Code	Address	Data	Parity or CRC	Symbol Length
Unused	00x	xxxxx	—	—	—
Read 32-bit block	110	aaaaa	—	Parity	3 symbols
Unused	111	00xxx	—	—	—
Unused	111	0100x	—	—	—
End Process	111	01010	—	Parity	3 symbols
Unused	111	01011	—	—	—
Unused	111	011xx	—	—	—
Unused	111	1000x	—	—	—
Set Talk First Bit	111	10010	—	Parity	3 symbols
Set FR Bit	111	10011	—	Parity	3 symbols
Clear Talk First Bit	111	10100	—	Parity	3 symbols
Clear FR Bit	111	10101	—	Parity	3 symbols
Unused	111	1011x	—	—	—
Unused	111	11xxx	—	—	—
Unused	100	xxxxx	—	—	—
Write 32-bit block	101	aaaaa	32 bits	CRC-16	14 symbols
Unused	01x	xxxxx	—	—	—

Legend: aaaaa = Block address
x = don't care
Command and address are sent MSN (most significant nibble) first
Data and parity/CRC are sent LSN (least significant nibble) first.

4.2.2 STRUCTURE OF DEVICE RESPONSE

When the device receives the interrogator command, it responds with 70 kHz - Manchester encoded data having the following structures:

For blocks 0 and 2:

Device Response = Preamble (8 bits) + Block Number (5 bits) + "000" + Block Data (32 bits) + Calculated CRC (CCRC: 16 bits)

For all other blocks:

Device Response = Preamble (8 bits) + Block Number (5 bits) + "000" + Block Data (32 bits) + Stored CRC (SCRC: 16 bits)

TABLE 4-3: INTERROGATOR COMMANDS AND DEVICE RESPONSES

Interrogator Command	Delay	Device Response
Read 32-bit block for block 0 and block 2	TDECODE	Preamble, block #, "000", block data, CCRC
Read 32-bit block except for block 0 and block 2	TDECODE	Preamble, block #,"000", block data, SCRC
Write 32-bit block	TWRITE	For blocks 0 and 2: Preamble, block #, "000",block data, CCRC For all others: Preamble, block #, "000", block data, SCRC
Set Fast Read (FR) bit	TWRITE	Preamble, 1 byte 0's, block 0 data, CCRC
Clear Fast Read (FR) bit	TWRITE	Preamble, 1 byte 0's, block 0 data, CCRC
Set Talk First (TF) bit	TWRITE	Preamble, 1 byte 0's, block 0 data, CCRC
Clear Talk First (TF) bit	TWRITE	Preamble, 1 byte 0's, block 0 data, CCRC
End Process (EP)	TDECODE	Preamble
FRR	f(TSMAX, TCMAX, 8-bit Tag ID)	Preamble,TC, TP, "0", Tag ID, FRF, FRR_CRC (bits 0-15 in block 0) (maximum of 160 data bits)
FRB	TDECODE	Preamble, address of block #1(00001),"000", Tag ID (32 bits), SCRC (64 data bits)

References used in this table. Examples are given in Section 7.0.

Preamble =	11111110 (8 bits)."0" is transmitted last.
Block # =	5 bit addressed block, transmits LSB (least significant bit) first.
Block data =	32-bit data of the addressed block, transmits LSB first.
CCRC =	Calculated CRC of the preceding block number and block data. Transmits LSB first.
SCRC =	Stored CRC. This SCRC is the CRC of the write command, address, and data from the interrogator, LSB first. The device stores the CRC of the command for each block. See Section 5.2 for details.
TP =	Tag parameters (4 bits: "0", DF0, DF1, parity). where DF0 and DF1 determine the FR field length (see Table 5-6).
TC =	Transmission counter (3 bits), transmits LSB first.
Parity =	Even parity bit of TC and TP.
Tag ID =	32 bits of unique identification code of the device, transmits LSB first. This Tag ID is pre-programmed in the factory prior to shipping.
8-bit Tag ID =	8 bits of Tag ID selected from the 32 bits of the unique tag identification code. Transmits LSB first (see Section 4.2.3.6 for selecting the 8 bits from the Tag ID).
FRF =	Fast Read Field (blocks 3-5), transmits LSB first (see Section 5.0).
f(TSMAX, TCMAX, 8-bit Tag ID =	Delay is a function of the TSMAX, TCMAX and 8-bit Tag ID.
TWRITE =	Writing time for EEPROM (see Table 1-3).
FRR_CRC =	CRC of 32-bit Tag ID first followed by fast read field (FRF) data.
TDECODE =	Time requirement for command decoding (see Table 1-3).

4.2.3 DETECTION OF INTERROGATOR COMMANDS

The interrogator sends commands to the device by amplituding modulating the carrier signal (gap pulse). The interrogator uses two classes of encoding signals for modulation. They are (a) 1-of-16 PPM for data transmission, and (b) specially timed gap pulse sequence for the fast read commands (FRR and FRB). The fast read commands consist of five gap pulses within nine possible gap pulse positions (1.575 ms). The combination of the possible gap positions determines the command type and parameters of the fast read command.

The interrogator also sends time calibration pulses (TCP) prior to the 1-of-16 PPM. The TCP is used to calibrate the time base of the decoder in the device. The specifics of the two encoding methods and the TCP are described in the following sections.

4.2.3.1 FAST READ COMMANDS

The fast read commands are composed of five 175 µs-wide gap pulses (see Figure 4-2) whose spacing within 1.575 ms determines the command type and its parameters. Table 4-4 shows the specification of the gap signal for the fast read commands. Two commands are used for the fast read. They are: (1) Fast Read Request (FRR) in the Detection loop, and (2) Fast Read Bypass (FRB) in the Reactivation loop. See Tables 4-5 and 4-6 for the FRR gap pulse positions and also Figures 4-3 to 4-8 for the gap modulation patterns.

The parameters of FRR are (1) number of time slots (TSMAX=1,16,or 64), (2) max transmission counter (TCMAX), and (3) data transmission speed. The FRB has only a data transmission speed parameter (normal or fast speed mode). The device extracts these parameters based on the positions of the five gap pulses within the 1.575 ms time span as shown in Figs. 4-3 to 4-8.

TSMAX=1 is given if there is only one device in the field. This is called “conveyor mode” or “single tag environment”. In this mode, the device responds with the FR response signal in every time slot until it receives a correct matching code, or until TCMAX is elapsed.

4.2.3.2 DATA TRANSMISSION SPEED

The interrogator can send data with two different data rates: (1) Normal and (2) Fast speed modes. The normal speed uses 2.8 ms/symbol, and the fast speed uses 160 µs/symbol. One symbol represents one 4-bit data packet (see Section 4.2.3.4 for 1-of-16 PPM). The data transmission speed is a parameter of the fast read commands (FRR and FRB). This parameter indicates the data speed of subsequent interrogator commands. The data rate of the device output (70 kHz) is not affected by this parameter.

TABLE 4-4: SPECIFICATION OF GAP SIGNAL FOR FAST READ COMMANDS (FRR AND FRB)

Number of gaps for one command	5
Total available number of gap positions within the command time span	9
Command time span	1.575 ms
Gap pulse width	175 µs

TABLE 4-5: SPECIFICATION OF MODULATION SEQUENCE FOR FAST READ REQUEST (FRR)

Maximum Time Slot (TSMAX)	TCMAX	Gap Pulse Position	Data Transmission Mode
1	1	(1,2,3,4,6)	Normal Speed
		(1,3,5,6,8)	Fast Speed
	2	(1,2,3,4,5)	Normal Speed
		(1,3,5,6,7)	Fast Speed
	4	(1,2,3,5,6)	Normal Speed
		(1,3,5,7,8)	Fast Speed
16	1	(1,2,4,6,8)	Normal Speed
		(1,3,4,6,8)	Fast Speed
	2	(1,2,4,6,7)	Normal Speed
		(1,3,4,6,7)	Fast Speed
	4	(1,2,4,5,6)	Normal Speed
		(1,3,4,5,6)	Fast Speed
64	1	(1,2,4,5,7)	Normal Speed
		(1,3,4,5,7)	Fast Speed

TABLE 4-6: SPECIFICATION OF MODULATION SEQUENCE FOR FRB COMMAND

Symbol	Gap Pulse Position	Data Transmission Mode
FRB_N	(1,2,3,5,7)	Normal Speed
FRB_F	(1,3,5,7,9)	Fast Speed

FIGURE 4-2: PULSE WAVEFORM OF GAP AND 1-OF-16 PPM SIGNALS

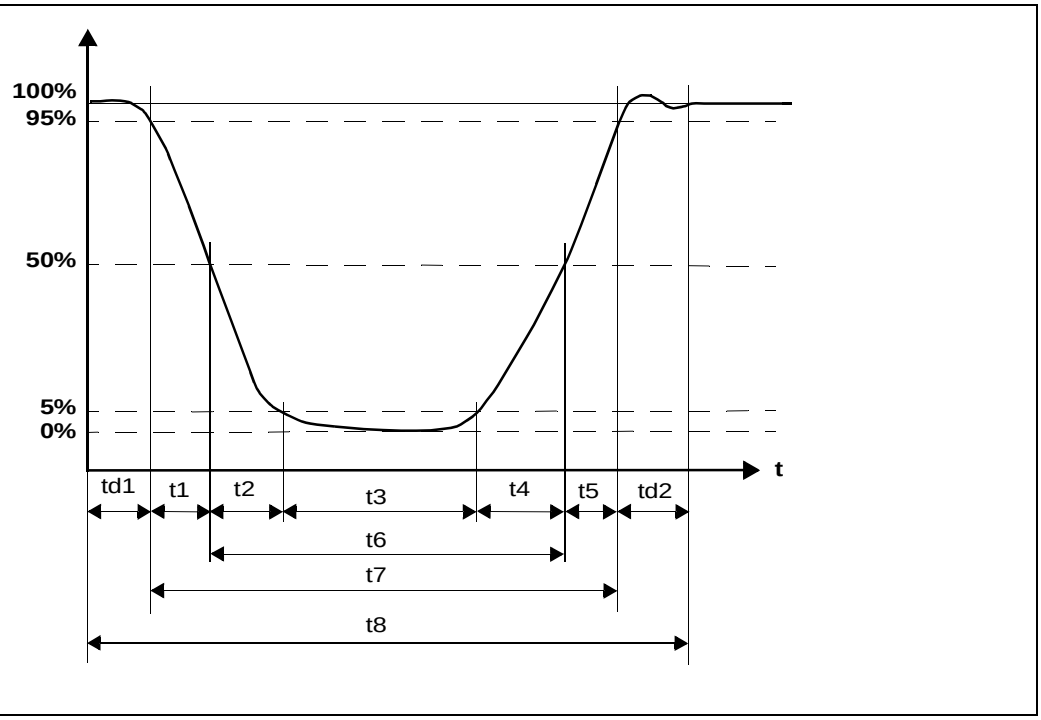


TABLE 4-7: WAVEFORM CHARACTERISTICS OF GAP AND 1-OF-16 PPM SIGNALS

Signal	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gap signal and 1-of-16 PPM for normal mode	td1	—	25	—	µs	—
	td2	—	25	—	µs	—
	t1	0	12.5	—	µs	—
	t2	0	12.5	—	µs	—
	t3	—	75	—	µs	—
	t4	0	12.5	—	µs	—
	t5	0	12.5	—	µs	—
	t6	—	100	—	µs	PW_{PPM_N}
	t7	—	125	—	µs	—
	t8	—	175	—	µs	—
1-of-16 PPM for fast mode	td1	—	1.25	—	µs	—
	td2	—	1.25	—	µs	—
	t1	0	0.75	—	µs	—
	t2	0	0.75	—	µs	—
	t3	—	4.5	—	µs	—
	t4	0	0.75	—	µs	—
	t5	0	0.75	—	µs	—
	t6	—	6	—	µs	PW_{PPM_F}
	t7	—	7.5	—	µs	—
	t8	—	10	—	µs	—

The following figures show the various modulation patterns of the fast read commands (FRR and FRB). Each command consists of a combination of five gap pulses within nine possible gap positions. The pulse width of each gap is 175 µs and the total time span of each command for the nine possible positions is 1.575 ms (175 µs x 9 = 1.575 ms).

In the figures, P*mn* represents *m*th gap pulse at *n*th gap position in the given data packet (symbol).

FIGURE 4-3: GAP MODULATION PATTERNS FOR FRR, NORMAL SPEED, TSMAX = 1

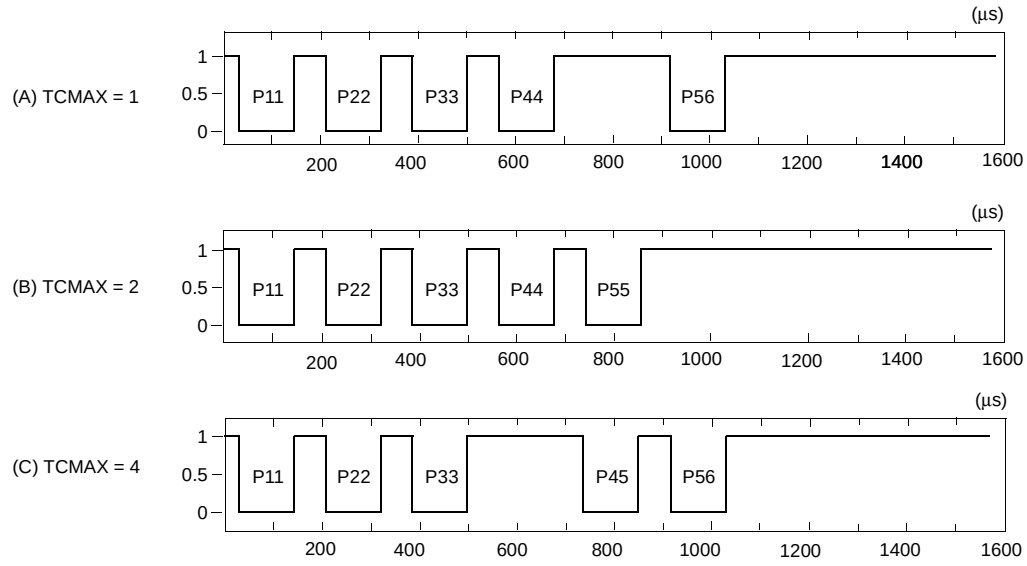


FIGURE 4-4: GAP MODULATION PATTERNS FOR FRR, FAST SPEED, TSMAX = 1

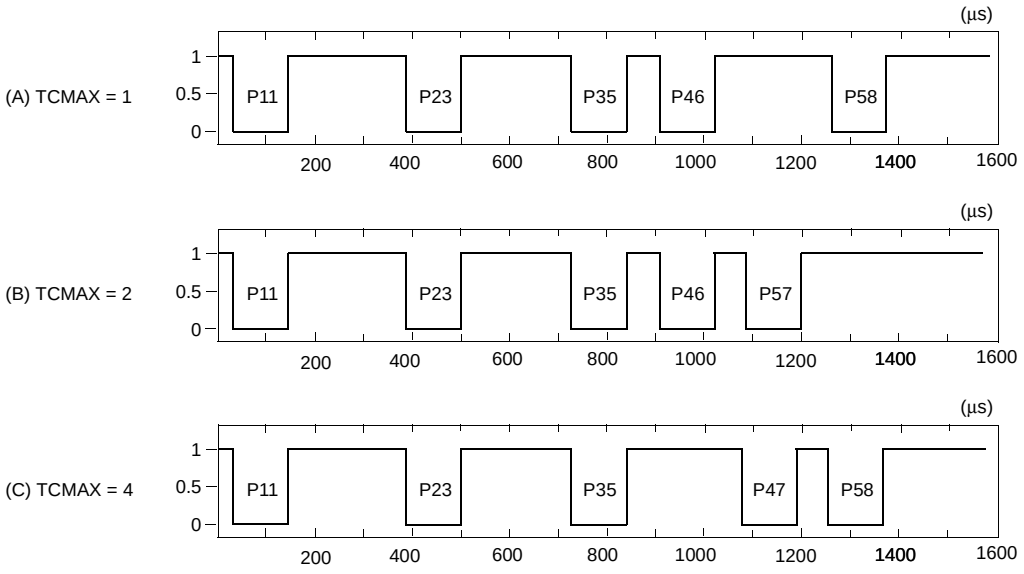


FIGURE 4-5: Gap Modulation Patterns for FRR, Normal speed, TSMAX = 16

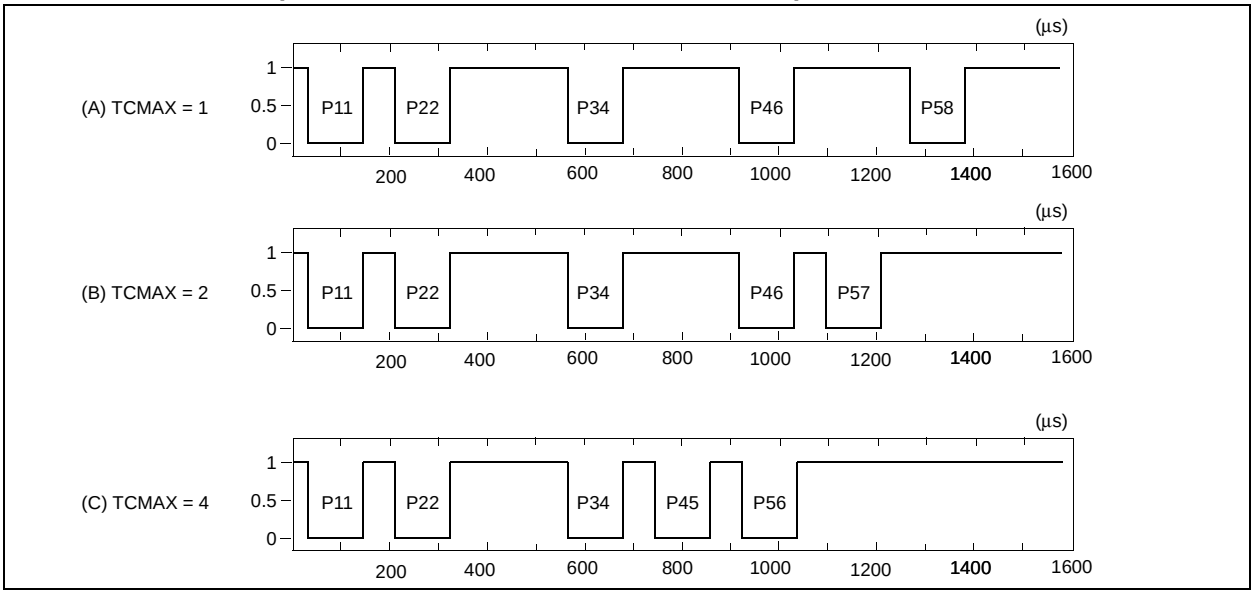


FIGURE 4-6: GAP MODULATION PATTERNS FOR FRR, FAST SPEED, TSMAX = 16

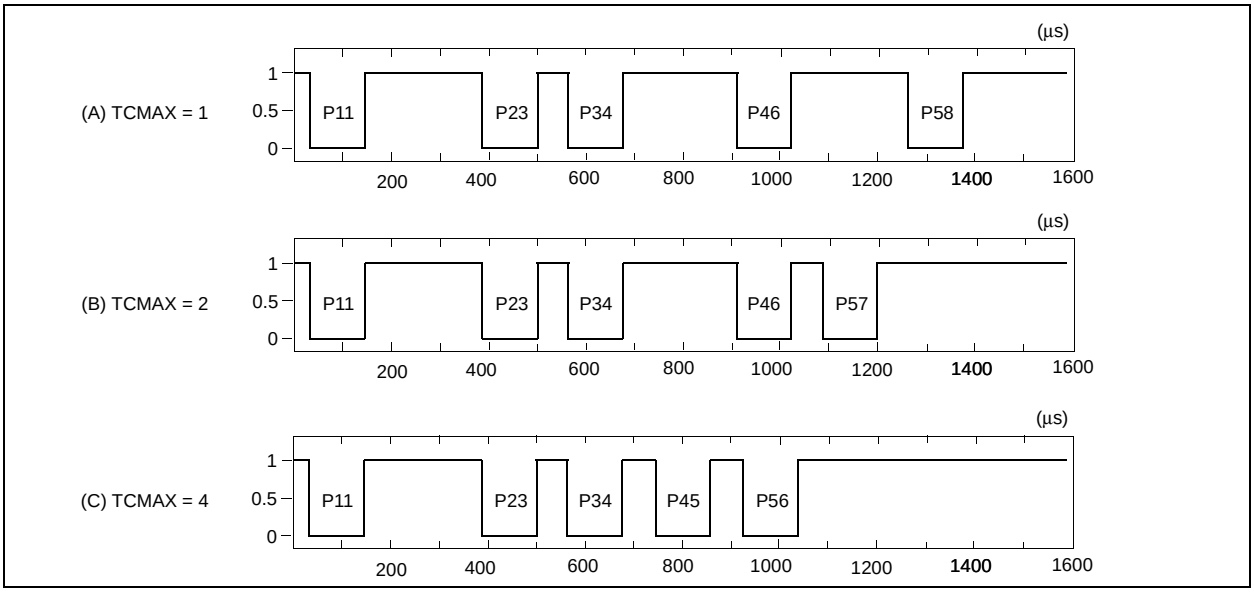


FIGURE 4-7: GAP MODULATION PATTERNS FOR FRR, TSMAX = 64, TCMAX = 1

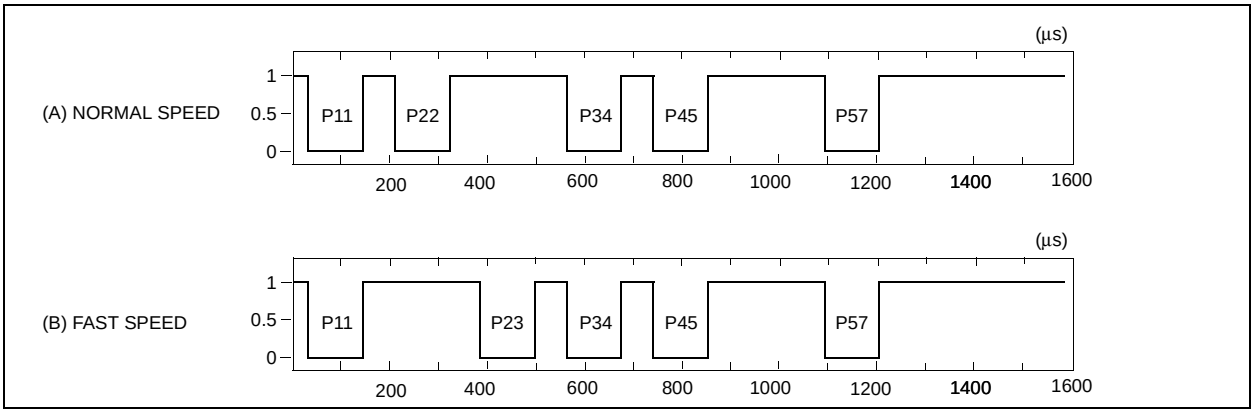
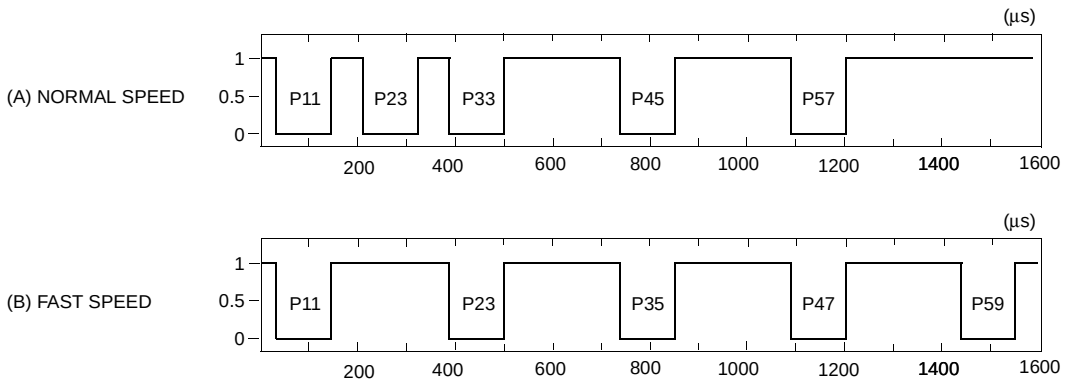


FIGURE 4-8: GAP MODULATION PATTERNS FOR FRB (FAST REQUEST BYPASS)



4.2.3.3 USAGE OF TSMAX AND TCMAX

The parameters of the TSMAX and TCMAX are determined by an expected number of tags in the detection loop. The following table shows the recommended FRR command repeat time for each of the 7 possible combinations of TSMAX and TCMAX. The command repeat time in Table 4-8 is calculated by:

Command Repeat Time = TSMAX x TCMAX x 2.5ms x 1.17

where:

1.17 is related to the tolerance of the baud rate.

TABLE 4-8: FRR COMMAND REPEAT TIME VS. (TSMAX, TCMAX)

(TSMAX,TCMAX)	(1,1)	(1,2)	(1,4)	(16,1)	(16,2)	(16,4)	(64,1)
Command Repeat Time	2.925 ms	5.85 ms	11.7 ms	46.8 ms	93.6 ms	187.2 ms	187.2 ms

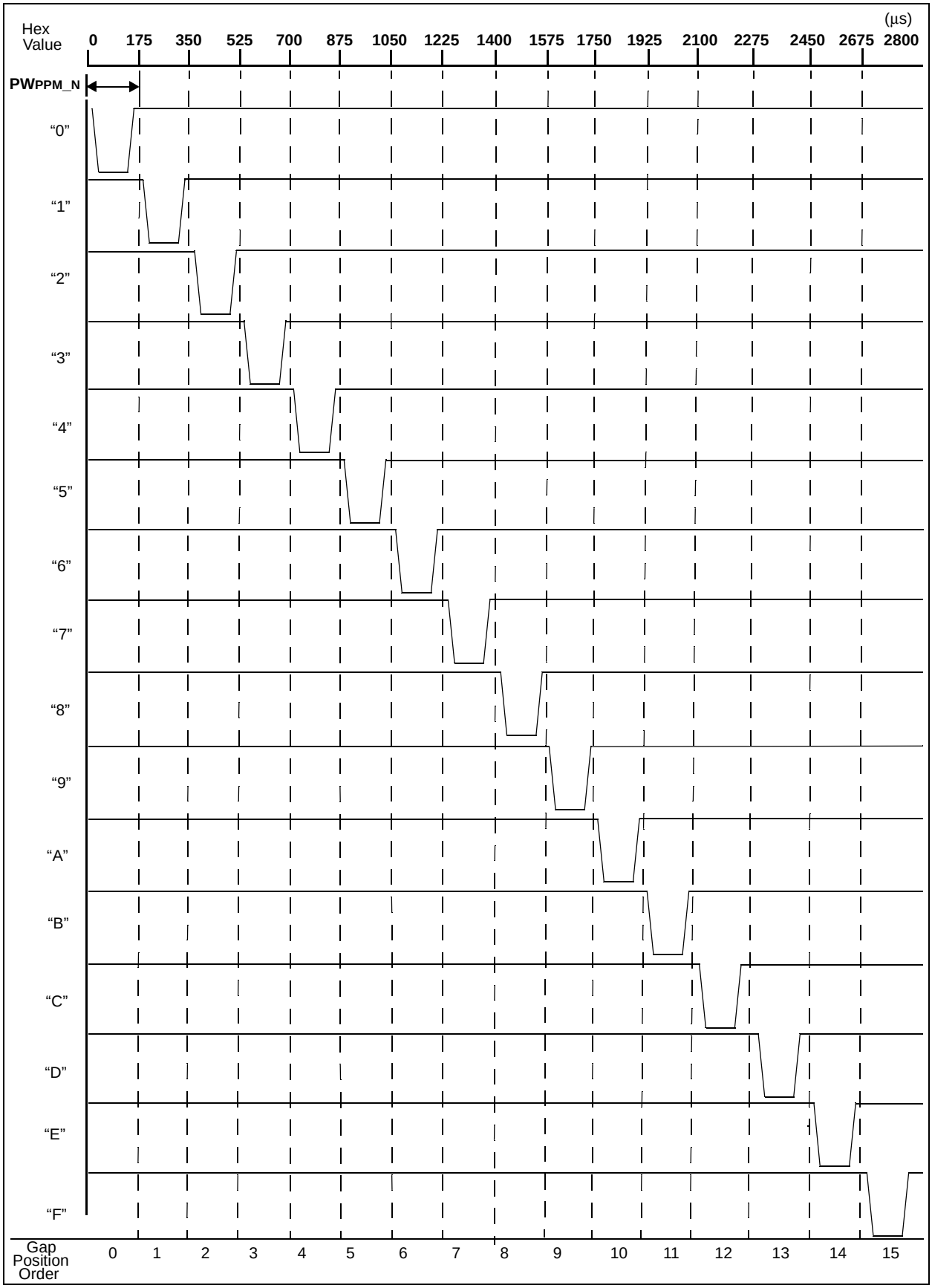
4.2.3.4 1-OF-16 PPM

The interrogator uses 1-of-16 Pulse Position Modulation (PPM) for matching codes (MC1 and MC2), End Process (EP), and also commands in Table 4-2. 1-of-16 PPM uses only one gap pulse in one of sixteen possible pulse positions for sending 4-bit symbols (2^4=16). This means one symbol (one data packet) represents 4 bits of binary data. One symbol lasts for 2.8 ms and 160 µs for normal speed and fast speed mode, respectively. All communications begin with time calibration pulses (TCP) composed of three pulses in positions zero, six and fourteen of a 1-of-16 PPM symbol as shown in Figure 4-10.

TABLE 4-9: 1-OF-16 PPM PULSE SPECIFICATIONS

	Normal Mode	**Fast Mode**
Modulation depth	100%	100%
Pulse width	175 µs	10 µs
Gap width	100 µs	6 µs
Pulse positions per symbol	16	16
Symbol width	2.8 ms	160 µs
Calibration sequence	Pulses in positions 0,6,14	Pulses in positions 0,6,14

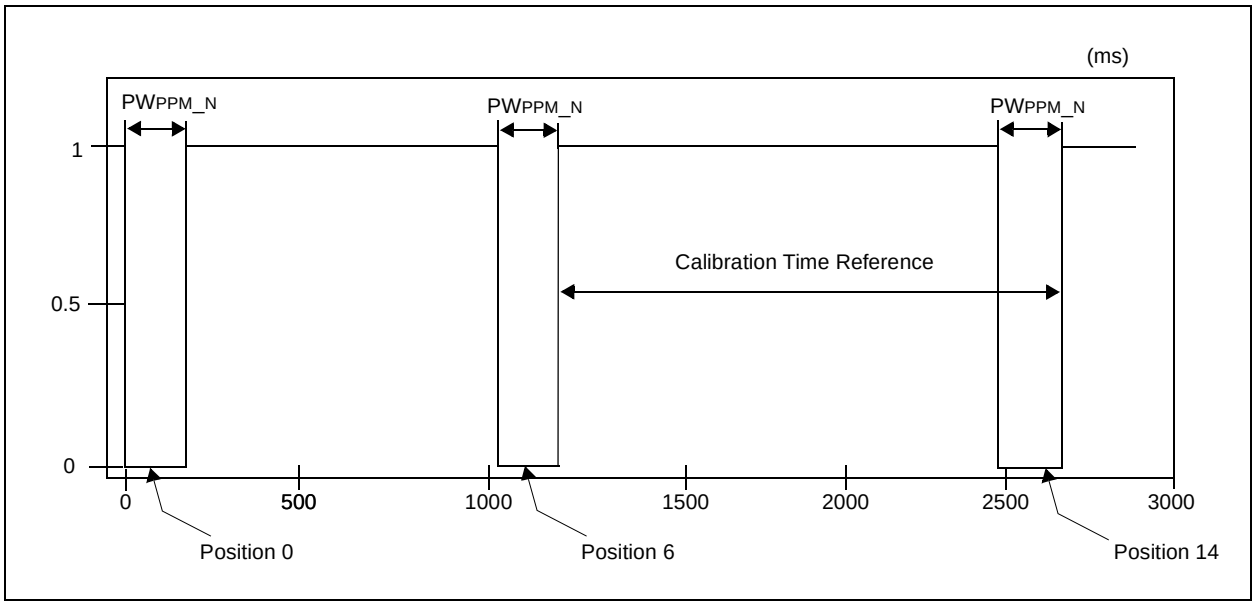
FIGURE 4-9: 1-OF-16 PPM REPRESENTATION FOR HEX VALUES FOR NORMAL SPEED MODE



4.2.3.5 CALIBRATION OF TIME REFERENCE FOR DECODING

The device uses time calibration pulses (TCP) to match its internal decoder timing to the interrogator timing. The interrogator transmits the timing pulses at the start of all commands and at least every 17 symbols. The TCP uses a code violation of the 1-of-16 PPM signal consisting of three gap pulses within one symbol. The first gap pulse is located at position 0, the second gap pulse at position 6, and the third at position 14 of the symbol. The time period between the last two gap pulses is used to calibrate the device's timing for decoding. Figure 4-10 shows the calibration pulses for normal speed mode. The waveform of the gap pulses is the same as the 1-of-16 PPM signal as shown in Figure 4-2. For the fast speed mode, the gap positions are the same. PW_{PPM_F} is the gap pulse width and SW_{PPM_F} is the symbol width of the fast mode.

FIGURE 4-10: CALIBRATION PULSES FOR NORMAL SPEED MODE



4.2.3.6 CALCULATION OF MATCHING CODE

When the interrogator receives the FR response from a device, it sends a matching code (MC) to select the device. The MC is sent during the device's listening window. There are two different types of matching codes. They are MC1 and MC2. Both MC1 and MC2 are used in the Detection loop and MC2 is used in the Reactivation loop as detailed in Figure 4-1. The MC1 command is used to send the device to the Sleeping loop, and MC2 is used to send the device to the Processing loop.

The MC is an 8-bit "match" of tag ID followed by 4-bit matching code type and parity bit such that:

> Matching code (12 bits) = "match (8 bits of tag ID)" + matching code type (3 bits)+ parity (1 bit)

The matching code type and parity bit is bit-wise structured as follows:

- MC1: 010P
- MC2: 100P

where P represents the parity bit of all match bits (8 bits) plus the MC type (3 bits).

The "match" part of the MC is eight bits of the 32-bit Tag ID. The interrogator selects the 8 bits from the 32-bit Tag ID by calculating the bit range of the Tag ID. Equation 4-1 shows the equation for selecting the bit range using the transmission counter (TC). Both the 32-bit Tag ID and TC are included in the FR response. An example for the calculation of the matching code is given in Section 7-2.

EQUATION 4-1: BIT-WISE EQUATION FOR "MATCH"

"Match" = Tag ID bit range a: b
{4*TC} modulo 32: {4 (TC +1) + 3} modulo 32

where {} modulo 32 means the remainder of {} divided by 32. For example, {28} modulo 32 and {35}modulo 32 are 28 and 3, respectively.

4.2.4 TIME SLOT GENERATOR

This block generates time slots for the device. The time slot represents the time delay between the end of the FRR command and the beginning of the FR response. The available time slots are 1, 16, or 64. One time slot represents 2.5 ms. The device calculates the actual time slot based on the TSMAX, TC, and Tag ID. The maximum time slot (TSMAX) is assigned to the device by the FRR command (see Figs. 4-3 to 4-7), or set to 16 if the talk first (TF) bit is set.

Four or six bits of the Tag ID are used at a time to calculate the time slot, with TC being the shift parameter to choose which portion of the 32-bit Tag ID is used as shown in Equation 4-2.

EQUATION 4-2: EQUATION FOR TIME SLOT CALCULATION

TSMAX	Time Slot = Tag ID bit range a:b
64	{[4(TC+1)+1] modulo 32: [4 TC] modulo 32} XOR TC LSB
16	{[4(TC+1)-1] modulo 32: [4 TC] modulo 32} XOR TC LSB
1	0

Note: The exclusive-or (XOR) in the above equation in Equation 4-2. This is called "semi-inverting" that randomizes worst case tag IDs, e.g. a Tag ID of '77777777' or '00000000'. Table 4-10 shows examples of the calculation.

TABLE 4-10: EXAMPLE: TAG ID = H'825FE1A0'

TC	Relevant Tag ID		Selected Tag ID before XOR with LSB of TC		Calculated Time Slot (TS) (after XOR with LSB of TC)			
	Hexadecimal	Binary	TSMAX=16	TSMAX=64	TSMAX=16		TSMAX=64	
0	h'825FE1(A0)'	b'1010 0000'	h'0'	h'20'	h'0'	d'0'	h'20'	d'32'
1	h'825FE(1A)0'	b'0001 1010'	h'A'	h'1A'	h'5'	d'5'	h'25'	d'37'
2	h'825F(E1)A0'	b'1110 0001'	h'1'	h'21'	h'1'	d'1'	h'21'	d'33'
3	h'825(FE)1A0'	b'1111 1110'	h'E'	h'3E'	h'1'	d'1'	h'01'	d'1'
4	h'82(5F)E1A0'	b'0101 1111'	h'F'	h'1F'	h'F'	d'15'	h'1F'	d'31'
5	h'8(25)FE1A0'	b'0010 0101'	h'5'	h'25'	h'A'	d'10'	h'1A'	d'26'
6	h'(82)5FE1A0'	b'1000 0010'	h'2'	h'02'	h'2'	d'2'	h'02'	d'2'
7	h'(08)25FE1A'	b'0000 1000'	h'8'	h'08'	h'7'	d'7'	h'37'	d'55'

In Table 4-10, h'x..x' represents hexadecimal number, d'x..x' represents decimal number, and b'x..x' represents binary number.

Table 4-10 shows the calculated time slot (TS) is 5 for TC=1 and TSMAX=16 with Tag ID =h'825FE1A0'. This means the device waits for 12.5 ms (5 x 2.5 ms = 12.5 ms) in a non-modulating condition between the end of FRR and the start of the FR response.

Also the TS is 37 for TC=1 and TSMAX=64. This means the device waits for 92.5 ms (37 x 2.5 ms = 92.5 ms) between the end of FRR and the start of the FR response in a non-modulating condition.

4.2.5 TIME SLOT COUNTER

This section generates the sleep time (2.5 ms x TS) of the device. During the sleep time, the device remains in a non-modulating condition.

5.0 MEMORY SECTION

The memory section is organized into two groups: (1) Main memory section and (2) Stored CRC Memory section.

5.1 Main Memory Section

The main section is organized into 32 blocks as shown in Table 5-1. Each block has 32 bits. The first 3 blocks (0 - 2) are used for predefined parameters and device operation. The next three blocks (3 - 5) are used as the fast read fields. The blocks from 6 to 29 (24 blocks) are used for user data memory. The remaining last 2 blocks (30 - 31) are reserved for future use. The memory is read or written in 32-bit selectable units, with the exception of the fast read (FR) bit and the talk first (TF) bit, which are individually selectable.

5.2 Stored CRC (SCRC) Memory Section

This memory section is used to store the CRC of the main memory section, and organized into 32 blocks. Each block has 16 bits. Each block contains the CRC in the corresponding block of the main memory section. The stored CRC (SCRC) corresponds to the interrogator command (write 32-bit block) and data.

TABLE 5-1: MEMORY ORGANIZATION

Main Memory Section (32 blocks x 32 bits)	Stored CRC (SCRC) Section (32 blocks x 16 bits)	Comments
MSB ... LSB	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
FR | TF | Tag Parameters | FR Response CRC		Block 0 (Tag Parameters/FR)
SNR 3 | SNR 2 | SNR 1 | SNR 0		Block 1 (Tag ID = Serial Number)
31 30 29 28 27 26 25 24 | 23 22 21 20 19 18 17 16 | 15 14 13 12 11 10 9 8 | 7 6 5 4 3 2 1 0		Block 2 (Write Protect 1st kb)
Fast | Read | Field | (LS Block)		Block 3 (FR Field Least Significant Block)
		Block 4 (FR Field)
Fast | Read | Field | (MS Block)		Block 5 (FR Field Most Significant Block)
		Block 6 (User Data)
		Block 7 (User Data)
		Block 8 (User Data)
		Block 9 (User Data)
		Block 10 (User Data)
		Block 11 (User Data)
. . . . .	. . . . .	. . . . .
		Block 29 (User Data)
		Block 30 (Reserved for future use)
		Block 31 (Reserved for future use)

5.3 BIT LAYOUT

5.3.1 BLOCK 0

The bit layout in block 0 is given in the following table. FR and TF bits are not write-protectable.

TABLE 5-2: BIT LAYOUT OF BLOCK 0

B0:31	B0:30	B0:29	B0:28	B0:27	B0:26	B0:25	B0:24
FR	TF	TFT1	TFT0	DF1	DF0	MT1*	MT0*
B0:23	B0:22	B0:21	B0:20	B0:19	B0:18	B0:17	B0:16
TM2*	TM1*	TM0*					
B0:15	B0:14	B0:13	B0:12	B0:11	B0:10	B0:9	B0:8
FRR CRC 15	FRR CRC 14	FRR CRC 13	FRR CRC 12	FRR CRC 11	FRR CRC 10	FRR CRC 9	FRR CRC 8
B0:7	B0:6	B0:5	B0:4	B0:3	B0:2	B0:1	B0:0
FRR CRC 7	FRR CRC 6	FRR CRC 5	FRR CRC 4	FRR CRC 3	FRR CRC 2	FRR CRC 1	FRR CRC 0

Note: * These are 'hardwired' bits, not EEPROM bits.

5.3.1.1 DESCRIPTION OF BITS

TABLE 5-3: FR BIT (B0:31)

FR	Answer to Fast Read Request signal
1	Yes (e.g. "Item" is unpaid in retail EAS applications)
0	No (e.g. "Item" has been purchased in retail EAS applications)

Note: FR bit is not write-protectable.

TABLE 5-4: TF BIT (B0:30)

TF	Talk first
0	Wait for FRR command
1	Send Fast Read Response without waiting for FRR command

Note: TF bit is not write-protectable.

TABLE 5-5: TFT BITS (B0:29 - B0:28)

TFT1	TFT0	Talk First TCMAX [1]
0	0	1
0	1	2
1	0	4
1	1	Never Elapses (Default) [2]

Note 1: Only applicable in tag talks first (TTF) mode. If FRR, TCMAX in command applies. Maximum time slot (TSMAX) parameter is set to 64 for TTF mode.

2: The device continuously sends its FR response until it receives its correct matching code. On average, the device will send its FR response every 80 ms.

TABLE 5-6: DF BITS (B0:27 - B0:26)

DF1	DF0	FR Data Field Length
0	0	32 bits (Default)
0	1	48 bits
1	0	64 bits
1	1	96 bits

TABLE 5-7: MT BITS (B0:25 - B0:24)

MT1	MT0	Memory type
0	0	Single level EEPROM (Default)
0	1	Reserved for future uses (e.g.; multi level EEPROM)
1	0	Reserved for future uses (e.g.; FRAM)
1	1	Reserved for future uses

Note: The MT bits are "hardwired".

TABLE 5-8: TM BITS (B0:23 - B0:21)

TM2	TM1	TM0	Total memory size
0	0	0	512 bits
0	0	1	1 Kbit (Default)
0	1	0	TBD
0	1	1	TBD
1	0	0	TBD
1	0	1	TBD
1	1	0	TBD
1	1	1	TBD

Note: The TM bits are “hardwired”.

TABLE 5-9: B0: (20-16) AND B0: (15-0)

B0:(20-16)	Available for user
B0:(15-0)	CRC for the Fast Read Response

5.3.2 BLOCK 1: UNIQUE 32-BIT TAG ID

Block 1 contains 32 bits of unique Tag ID with stored CRC (SCRC). The ID is uniquely serialized.

5.3.3 BLOCK 2: WRITE PROTECT FOR THE FIRST KBITS

Each bit corresponds to a 32-bit block, i.e. bit 0 to block 0, bit 1 to block 1, etc. Write protection is a one way process, i.e. once a block is write protected, it cannot be modified. It should be noted that the write protect block itself can be write protected. TF and FR bits in block 0 are not write-protectable even if the write-protection bit in the block is set.

TABLE 5-10: WRITE PROTECT

Block X Write Status	Bit X of Write Protect Block
Block X writable	1
Block X write protected	0

5.3.4 BLOCKS 3-5: FAST READ FIELDS

These blocks contain data bits for the FR response. The state of the DF bits (see Table 5-6) in block 0 determines the actual number of bits to be sent. This block can be used as a customer ID or also as additional tag ID numbers.

6.0 DEVICE TESTING

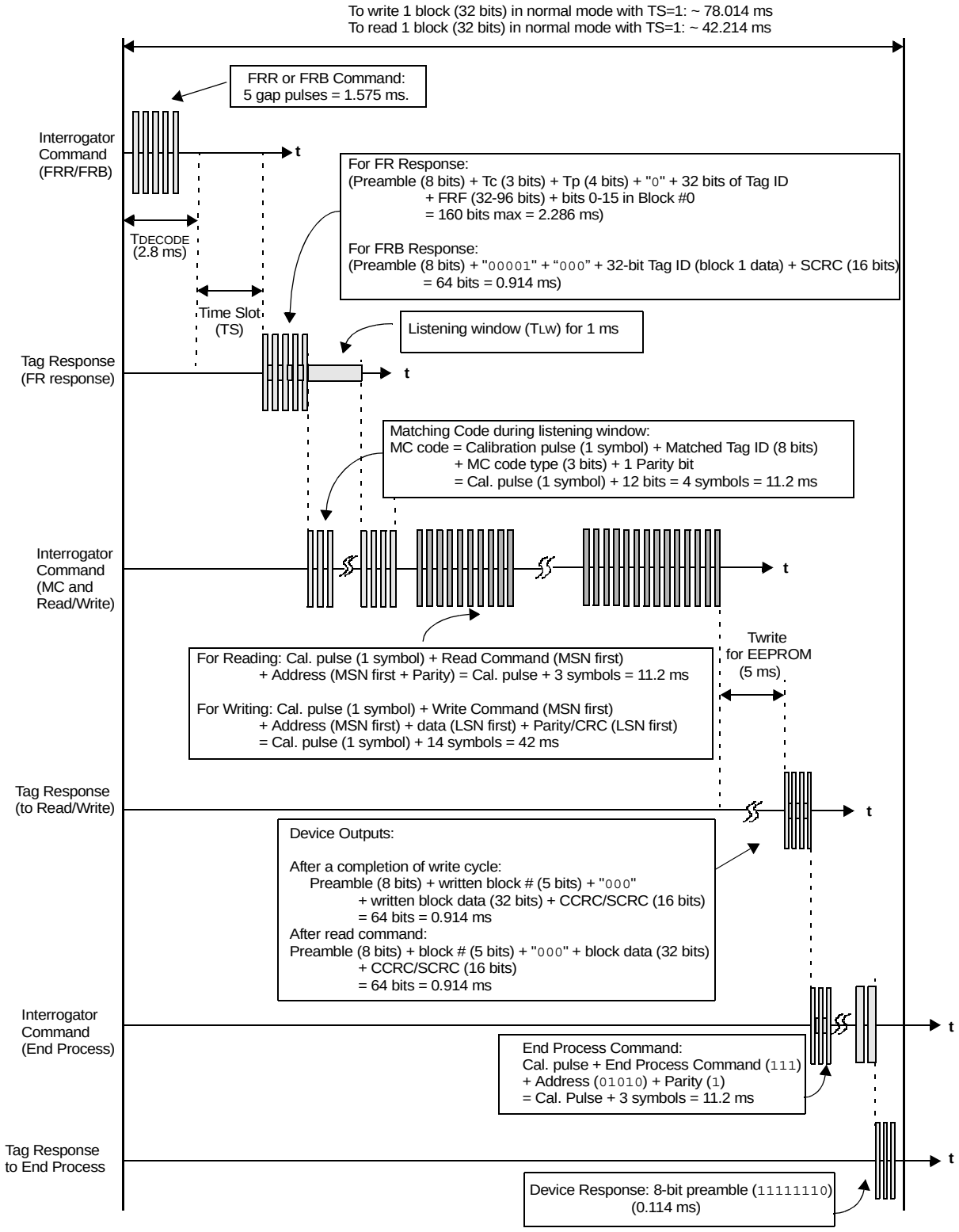
The device will be shipped to customers with the Fast Read (FR) bit set, and with block 1 write-protected.

The following bits are factory programmed prior to shipping:

1. DF0(B0:26) and DF1(B0:27) are set to “0”.
2. TFT0(B0:28) and TFT1(B0:29) bits are set to “1”.
3. All bits in the FR field (blocks 3-5) are programmed to “1”s.
4. The FRR_CRC(B0:0 - B0:15) bits are also programmed according to the Tag ID and item (3) above.

7.0 EXAMPLES

EXAMPLE 7-1: READ/WRITE PULSE SEQUENCE



EXAMPLE 7-2: CALCULATION OF MATCHING CODE FOR TAG ID = 825FE1A0 (HEX, MSB FIRST)

The “match” part of the matching code is calculated by the Bit-Wise Equation in Equation 4-1:

“Match (8 bits)” = Tag ID bit range a:b = {4(TC)}modulo 32: {4(TC + 1) + 3}modulo 32

For TC = 2, the above equation gives a = 8, and b = 15.

The “Match (8 bits)” is chosen from (8th 9th 10th 11th) and (12th 13th 14th 15th) bits of the Tag ID.

Therefore, for the Tag ID = 825FE1A0 (hex) = b/1000 0010 0101 1111 1110 0001 1010 0000/,

“Match (8 bits)” = b/1110 0001/ = 1E (hex).

Using this “Match” part, a complete set of matching code is assembled as:

1E5 for MC1, and

1E9 for MC2

where: 5 in the MC1 was from b/0101/ (010 for MC1 and the last “1” is a parity bit),
and 9 in the MC2 was from b/1001/ (100 for MC2 and the last “1” is a parity bit).

Gap position in the 1-of-16 PPM signal for the calculated MC codes:

The gap position numbers in the 1-of-16 PPM for the calculated MC codes are (see Figure 4-9 for 1-of-16 PPM):

Positions 1, 14, and 5 for 1E5 for MC1 code

Positions 1, 14, and 9 for 1E9 for MC2 code.

The “Match” part of the matching code for various TCs are given in Table 7-1.

TABLE 7-1: CALCULATED “MATCH” FOR TAG ID = 825FE1A0 (HEX)

TC	“Match (8 bits) in hex”
0	0A
1	A1
2	1E
3	EF
4	F5
5	52
6	28
7	80

EXAMPLE 7-3: TO WRITE DATA INTO THE DEVICE

The interrogator command structure for writing (see Section 4.2.1) is:

Calibration pulse + Writing Command (MSN first) + Address (MSN first) + Data (LSN first) + Parity/CRC (LSN first)

If the interrogator wants to write data “0123cdef (Hex, MSB to LSB)” to block 5, the following message will be sent:

Calibration pulse + Write Command (MSN first) + Address (MSN first) + Data (LSN first) + Parity/CRC (LSN first)

= `101` (write command) + `00101` (address) + f e d c 3 2 1 0 (data, hex) + CRC

= Calibration pulse + a 5 f e d c 3 2 1 0 6 0 2 e (hex string)

The hex string above is encoded with the 1-of-16 PPM signals. See Figure 4-10 for the 1-of-16 PPM representation of hex values.

Referring to Figure 4-10, the gap positions in the 1-of-16 PPM for the above hex string are:

Positions 10 (a), 5 (5), 15 (f), 14 (e), 13 (d), 12 (c), 3 (3), 2 (2), 1 (1), 0 (0), 6 (6), 0 (0), 2 (2), e (14).

EXAMPLE 7-4: TO READ DATA FROM THE DEVICE

To read the content of block 5 that has been programmed in the previous example, the interrogator sends the following command:

Calibration pulse + Read Command (`110`) + Address (`00101`) + Parity (`0`)

= Calibration pulse + C50 (hex)

The gap positions in the 1-of-16 PPM signal for the above hex string are:

12 (C), 5 (5), 0 (0).

Device Response:

When the device receives the above interrogator command, the device outputs the following 70 kHz Manchester encoded data string (see Section 4.2.2 for the structure of device response):

Preamble (8 bits) + Block number (5 bits, LSB first) + ‘000’ + Block Data (32 bits, LSB first) + SCRC (16 bits)
= `1-1-1-1-1-1-1-0` (f7) + `1-0-1-0-0-0-0-0` (5 0) + `1-1-1-1 0-1-1-1 1-0-1-1...` `1-0-0-0 0-0-0-0` (f e d c 3 2 1 0)
+ `0-1-1-0 0-0-0-0 0-1-0-0 0-1-1-1` (602e).

EXAMPLE 7-5: TO SEND THE “END PROCESS” COMMAND

The interrogator command structure (see Section 4.2) for the End Process is:

Calibration pulse + End Process Command (`111`) + Address (`01010`) + Parity (`1`)

= Calibration pulse + EA1 (hex)

The gap positions in the 1-of-16 PPM signal for the above hex string are:

14 (E), 10 (A), 1 (1).

Device Response:

The device outputs the 8-bit preamble (“`11111110`”) when it receives the End Process command, and enters the Sleeping loop.

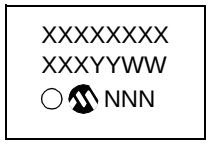
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

8-Lead PDIP (300 mil)

Example

8-Lead SOIC (150 mil)



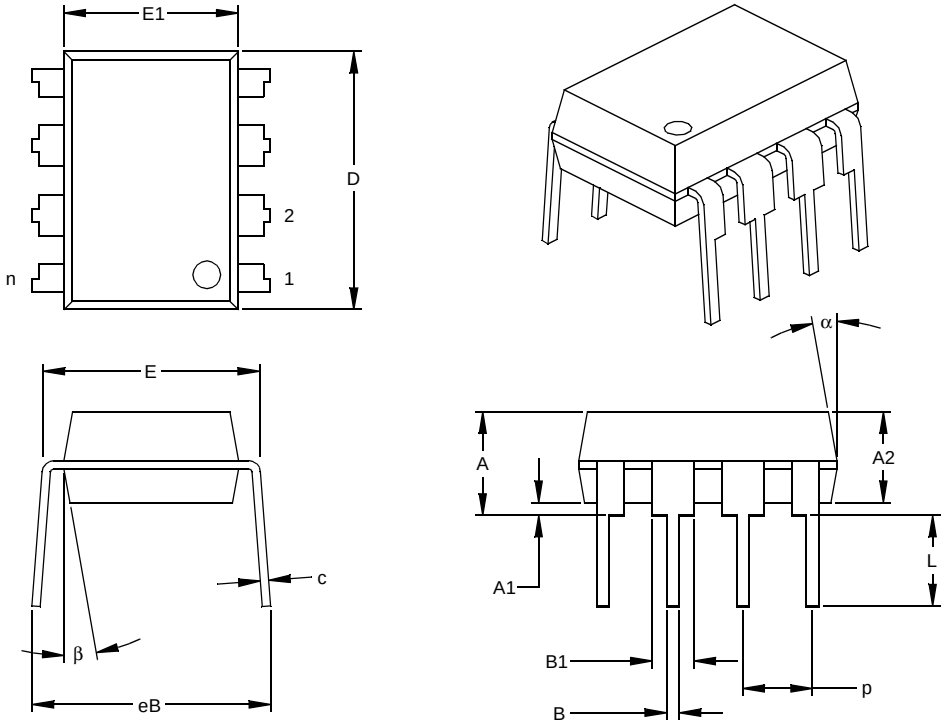
Example

Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard OTP marking consists of Microchip part number, year code, week code, and traceability code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

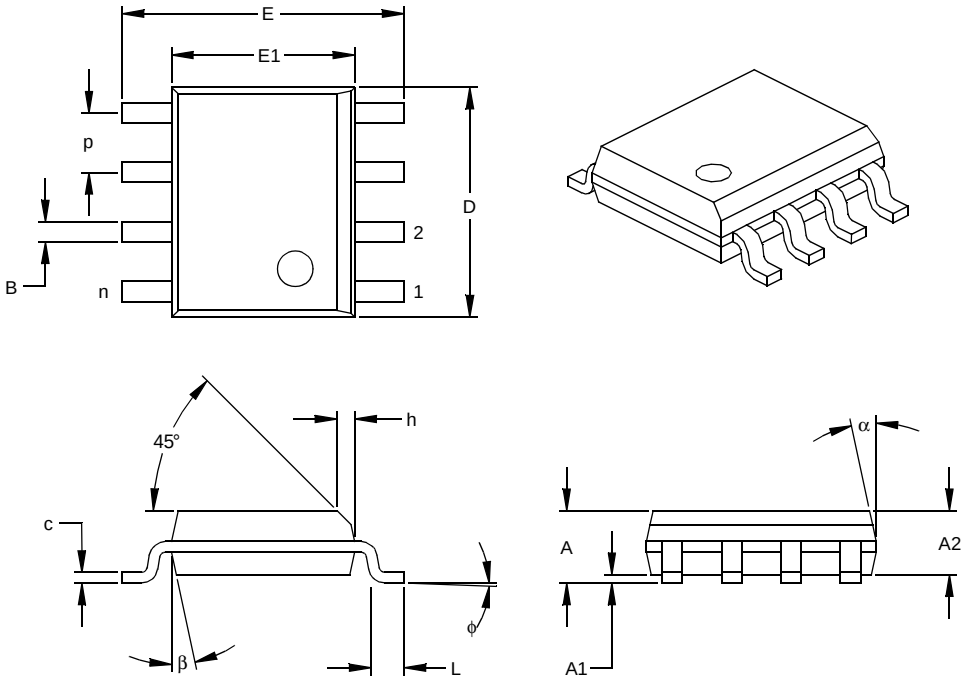


UNITS		INCHES*			MILLIMETERS		
DIMENSION LIMITS		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



UNITS		INCHES*			MILLIMETERS		
DIMENSION LIMITS		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	.10	.18	.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	.25	.38	.51
Foot Length	L	.019	.025	.030	.48	.62	.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	.20	.23	.25
Lead Width	B	.013	.017	.020	.33	.42	.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
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	WFB	=	Bumped, sawed 8” wafer on frame (11 mil backgrind)	
	W	=	8” wafer (11 mil backgrind)	
	WB	=	Bumped 8” wafer (11 mil backgrind)	
	S	=	Dice in waffle pack	
	SB	=	Bumped die in waffle pack	
	SN	=	SOIC, 8-lead, 300 mil body	
	P	=	PDIP, 8-lead, 150 mil body	
Device:	MCRF450/451/452/455	=	13.56 MHz Read/Write Anti-collision device	

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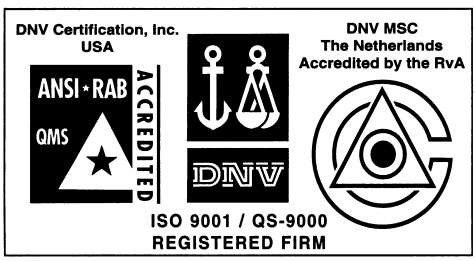

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