National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC415A-X REV 1A0

Original Creation Date: 02/03/99
Last Update Date: 11/02/00
Last Major Revision Date: 02/03/99

QUAD, WIDEBAND MONOLITHIC OP AMP

General Description

The CLC415 is a wideband, quad, monolithic operational amplifier designed for intermediate-gain applications where power and cost per channel are of primary concern. Benefitting from Comlinear's current feedback architecture, the CLC415 offers a gain range of ±1 to ±10 while providing stable, oscillation-free operation without external compesation, even at unity gain.

Operating from ±5V supplies, the CLC415 consumes only 50mW of power per channel, yet maintains a 160MHz small-signal bandwidth and a 1500V/us slew rate. High density applications requiring an integrated solution will enjoy the CLC415's 70dB channel isolation(input referred @ 5MHz).

With its exceptional differential gain and phase, typically 0.03% and 0.03degree @ 3.58MHz, the CLC415 is designed to meet the performance and cost per channel requirements of high volume composite video applications. The CLC415's large-signal bandwidth, high slew rate and high drive capability are features well suited for RGB-video applications.

The CLC415 is a quad version of the high speed CLC406 while the CLC414 is a lower power quad version of the same. Both of these quads afford the designer lower power consumption and lower cost per channel with the additional benefit of requiring less board space per amplifier.

Constructed using an advanced, complementary bipolar process and Comlinear's proven current feedback architectures, the CLC415 is available in several versions to meet a variety of requirements.

Industry Part Number

CLC415A

NS Part Numbers

CLC415AJ-QML

Prime Die

UB1562A

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 160MHz small signal bandwidth
- 0.05% setting in 12ns
- Low power, 160mW (40mW disabled)
- Low distortion, -60dBc at 20 MHz
- Fast disable (200ns)
- Differential gain/phase: 0.01% / 0.01degrees
- ±1 to ±8 closed-loop gain range

CONTROLLING DOCUMENTS:

CLC415AJ-QML	5962-9305501MCA

Applications

- Video switching and distribution
- Analog bus driving (with disable)
- Low power "standby" using disable
- Fast, precision A/D conversion
- D/A current-to-voltage conversion
- IF processors
- High-speed communications

(Absolute Maximum Ratings)
(Note 1)

Supply voltage (Vs)	±7 V dc
Output current (Iout)	70 mA
Common mode input voltage (Vcm)	±Vs
Differential input voltage (Vid)	10 V
Maximum Power dissipation (Pd) (Note 2)	1.2 W
Lead temperature (soldering, 10 seconds)	+300C
Junction temperature (Tj)	+175C
Storage temperature range	-65C to +150C
Thermal Resistance	
Junction -to-ambient (ThetaJA)	
Ceramic DIP (Still Air)	TBD
(500 LFPM)	TBD
Junction-to-case (ThetaJC)	
Ceramic DIP	TBD
Package Weight (typical)	
Ceramic DIP	TBD
ESD Tolerance (Note 3)	
ESD Rating	1000V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) / ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply voltage (Vs)	±5 V dc
Gain Range (Av)	±1 to ±10
Ambient Operating Temperature Range (Ta)	-55C to +125C

Electrical Characteristics

(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vs = ±5 V dc, Av = +6, and Rf = 500 Ohms. -55 C ≤ Ta ≤ +125C . (NOTE 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Iin	Input bias current (noninverting)				-13	13	uA	1, 2
					-25	+25	uA	3
-Iin	Input bias current (inverting)				-10	10	uA	1
					-15	15	uA	2
					-18	18	uA	3
Vio	Input offset voltage	Rs = 50 Ohms			-5.0	5.0	mV	1
					-10.0	10.0	mV	2
					-9.0	9.0	mV	3
Tc	Average + input bias current drift		1		-50	50	nA/C	2
(+Iin)	Average + input bias current drift		1		-100	100	nA/C	3
Tc	Average -input bias current drift		1		-50	50	nA/C	2
			1		-125	125	nA/C	3
(-Iin)	Average -input bias current drift		1		-125	125	nA/C	3
Tc	Average input offset voltage drift		1		-50	50	uV/C	2, 3
(Vio)	Average input offset voltage drift		1		-50	50	uV/C	2, 3
Is	Supply current (all channels)	No load				26	mA	1
						24	mA	2
						27	mA	3
+Rin	Input resistance		1		600		kOhms	1, 2
			1		300		kOhms	3
Iout	Output current		1		50		mA	1, 2, 3
PSRR	Power supply rejection ratio	+Vs = +4.5V to +5.0V, -Vs = -4.5V to -5.0V			47		dB	1, 3
					45		dB	2
CMRR	Common mode rejection ratio	Vcm = ±1V	1		45		dB	4, 6
			1		43		dB	5

Electrical Characteristics

(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vs = ±5 V dc, Av = +6, and Rf = 500 Ohms. -55 C ≤ Ta ≤ +125C . (NOTE 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
SSBW	Small signal bandwidth	-3 dB bandwidth, Vout < 2.0 Vpp			105		MHz	4
			2		80		MHz	5
			2		105		MHz	6
LSBW	Large signal bandwidth	-3 dB bandwidth, Vout < 5.0 Vpp	1		95		MHz	4
			1		80		MHz	5
			1		85		MHz	6
GFPL	Gain flatness peaking low	0.1 MHz to 25 Mhz, Vout <2.0 Vpp				0.2	dB	4
			2			0.2	dB	5, 6
GFPH	Gain flatness peaking high	> 25 MHz, Vout <2.0 Vpp				0.5	dB	4
			2			0.5	dB	5, 6
GFR	Gain flatness rolloff	At 0.1 MHz to 50 MHz				0.9	dB	4
			2			1.2	dB	5
			2			0.9	dB	6
HD2	Second harmonic distortion	2 Vpp at 20 MHz				-38	dBc	4
			2			-34	dBc	5
			2			-38	dBc	6
HD3	Third harmonic distortion	2 Vpp at 20 MHz				-46	dBc	4
			2			-42	dBc	5
			2			-46	dBc	6
SNF	Total noise floor	At > 1 MHz	1			-155	dBm (1Hz)	4, 6
			1			-154	dBm (1Hz)	5
INV	Total integrated noise	At 1 MHz to 100 MHz	1			38	uV	4, 6
			1			38	uV	5
VN	Input noise, non-inverting voltage	> 1 MHz	1			3.6	nVsqRtHz	1, 3
			1			4.0	nVsqRtHz	2
ICN	Input noise, inverting current	> 1 MHz	1			14	pA/sqRtHz	1, 3
			1			16	pA/sqRtHz	2

Electrical Characteristics

(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vs = ±5 V dc, Av = +6, and Rf = 500 Ohms. -55 C ≤ Ta ≤ +125C . (NOTE 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
NCN	Input noise, non-inverting current	> 1 MHz	1			2.6	pA/sq RtHz	1, 3
			1			3.0	pA/sq RtHz	2
LPD	Linear phase deviation	0.1 MHz to 75 Mhz	1			1.0	Deg	4, 6
			1			1.3	Deg	5
DG1	Differential gain	At 3.58 MHz, Rl = 150 Ohms, Av = +2	1			0.08	%	4, 5, 6
DG2	Differential gain	At 4.43 MHz, Rl = 150 Ohms, Av = +2	1			0.1	%	4, 5, 6
DP1	Differential phase	At 3.58 MHz, Rl = 150 Ohms, Av = +2	1			0.08	Deg	4, 5, 6
DP2	Differential phase	At 4.43 MHz, Rl = 150 Ohms, Av = +2	1			0.1	Deg	4, 5, 6
XT	Crosstalk	At 5 MHz, all hostile, input referred	1, 4			60	dB	4, 6
			1, 4			59	dB	5
CXT	Crosstalk	At 5 MHz, channel to channel	1, 5			63	dB	4, 6
			1, 5			62	dB	5
+Vout	Output voltage swing	Rl = 100 Ohms	2		+2.5		V	4, 5
			2		+2.3		V	6
-Vout	Output voltage swing	Rl = 100 Ohms	2			-2.5	V	4, 5
			2			-2.3	V	6
Cin	Input capacitance		1			2.0	pF	4, 5, 6
RO	Output impedance	dc	1			0.3	Ohms	4
			1			0.2	Ohms	5
			1			0.6	Ohms	6
CMIR	Common mode input voltage range		1		-2.0	2.0	V	4, 5
			1		-1.4	1.4	V	6
SR	Slew Rate	Measured ±1 V with ±4 V step	1		1200		V/us	4, 6
			1		1000		V/us	5
TRS	Rise and fall time	2 V step	1			3.0	ns	9, 11
			1		8	4.0	ns	10

Electrical Characteristics

(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vs = ±5 V dc, Av = +6, and Rf = 500 Ohms. -55 C ≤ Ta ≤ +125C . (NOTE 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
TRL	Rise and fall time	5 V step	1			3.6	ns	9
			1			4.5	ns	10
			1			4.0	ns	11
tS	Settling time	2 V step at 0.1 percent of the fixed value	1			18	ns	9, 11
			1			22	ns	10
OS	Overshoot	2 V step	1			12	%	9, 10, 11

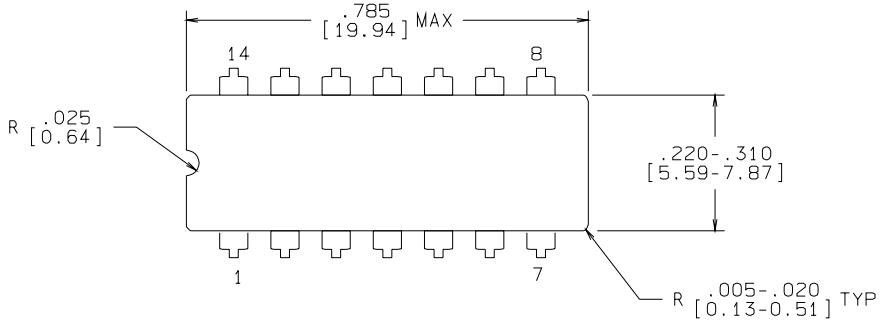
Note 1: If not tested, shall be guaranteed to the limits specified in table 1 herein.
Note 2: Group A testing only.
Note 3: The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.
Note 4: Three channels are driven simultaneously while observing the output of the undriven fourth channel.
Note 5: One channel is driven with a 2Vpp pulse while the output of the most affected channel is observed.

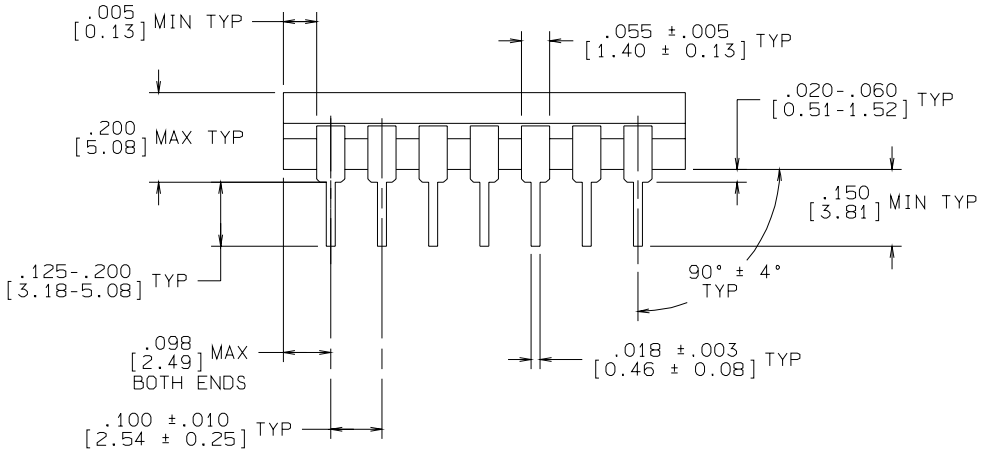
Graphics and Diagrams

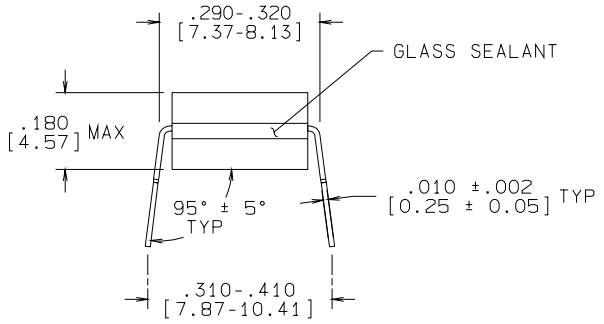
GRAPHICS#	DESCRIPTION
07066HRA2	CERDIP (J), 14 LEAD (B/I CKT)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000414A	CERDIP (J),14 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

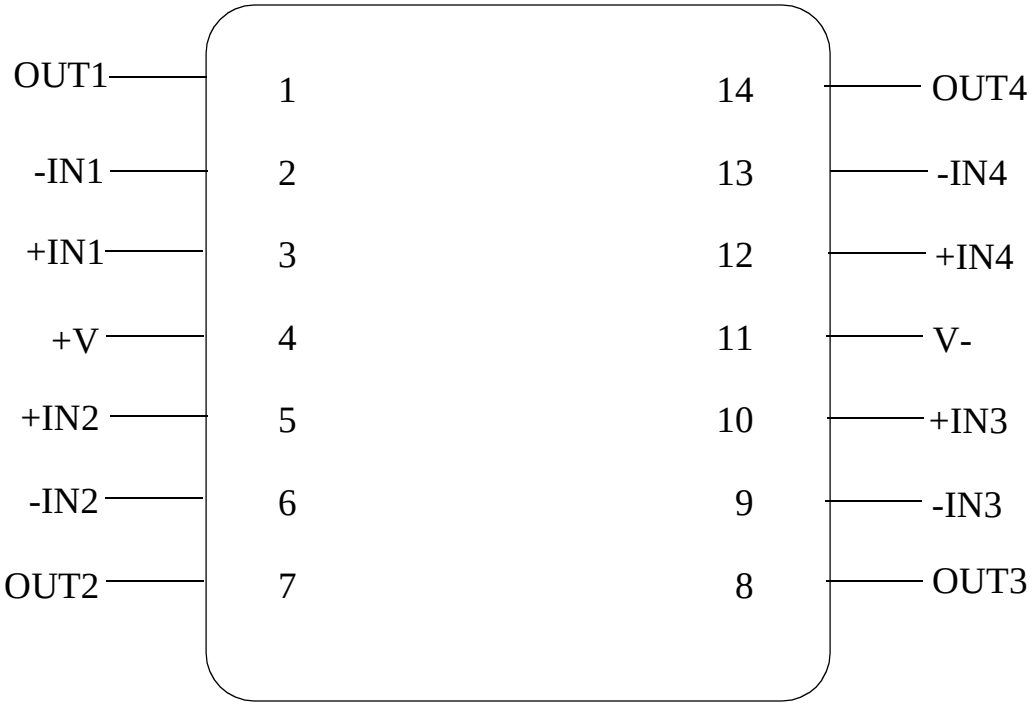
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



CLC415J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000414A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A0	M0003769	11/02/00	Rose Malone	Initial MDS Release: MNCLC415A-X, Rev. 1A0. Limits for SSBW are 105MHz for rm/cold and 85MHz for hot, and for GRF are 0.9dBat foom/cold and 1.2dB at hot. For +Iin Subgroup 3 Min. is -25uA and Max. is +25uA.