ST50160

ADSL RESIDENTIAL COMBO GATEWAY PROCESSOR

DATA BRIEF

1 GENERAL FEATURES

- WAN modem feature set
- Embedded ADSL transceiver ANSI T1.413, ITU G.dmt Annex A, B, C and Deutsche Telecom UR-2 compliant, splitterless ITU G.Lite
- Compatibility:
  – MTC20174, ADSL front end, 7th generation, integrated line driver, DCXO

1.1 Session Control

- PPPoE point to point protocol over Ethernet
- PPPoA point to point protocol over ATM
- PPPoA relay via PPP session control on terminal

1.2 ATM features

- Adaptation Layers: AAL5 (data), supported in hardware
- Encapsulation: RFC1483 and RFC2684, multi protocol encapsulation over ATM AAL5 bridged and routed modes
- ATM circuit: 8 PVC
- Data Qos: UBR, VBR, CBR

1.3 LAN feature set

- 1 Ethernet 10/100 (R)MII port (HPNA compatible)
- 1 USB port (bridged with LAN/WLAN port)
- Wireless support with Reverse MII port
- 2 UARTs, Bluetooth compatible
- Bridging: IEEE 801.1d, spanning tree WAN to LAN on Ethernet or USB
- Embedded router: RIP1, RIP2, static routing
- NAT/PAT with extended ALG support
- DHCP server/client
- IP protocol: TCP/IP ARP sharing access, IGMP, ICMP
- Support up to 128 stations
- Embedded http server for configuration

1.4 Configuration and Provisioning

- Configuration: remote configuration via Java™
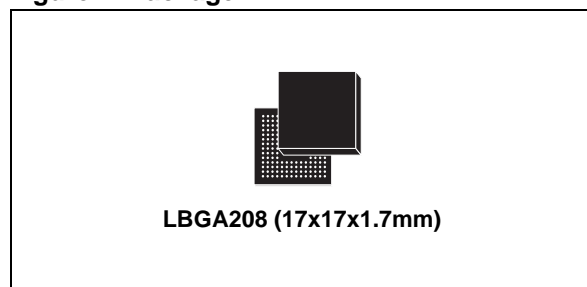
Figure 1. Package

LBGA208 (17x17x1.7mm)

Table 1. Order Codes

Part Number	Description
ST50160PF	LBGA208 (17x17x1.7mm)

enabled browser
- Firmware remote upload via network.
- Management: SNMP, UNI3.1, ILMI 4.0 (management and auto configuration)

1.5 Customization

- Customization with comprehensive API
- Development tool based on windows environment on PC
- Posix compatible RTOS
- Exposed BSP layer
- Flexible development licenses based on kernel software in object or source format

2 APPLICATIONS

- Low cost ADSL residential gateway (RG)
- Residential gateway with broadband ADSL WAN transceiver
- Wan to LAN bridge and router with ADSL WAN transceiver and Ethernet MII
- Wireless LAN access point with ADSL WAN transceiver and Ethernet MII
- ADSL WAN to USB bridge
- Dual Ethernet/USB bridge with bridged our routed WAN ADSL transceiver

3 DESCRIPTION

The ST50160 is a low cost ADSL bridge and LAN router. One 10/100Mbits Ethernet port allows the connection of a LAN to the WAN in bridged or routed mode. The data traffic can be routed through a local terminal by using the LAN /WLAN port or the USB port. The presence of NAT and DHCP and the API slots for firewall functions allow for a high-speed connection of LAN connected devices like PC to the public Internet in an isolated and secure environment. The chip is built around an ARM 946ES RISC processor. It embeds an ADSL, a complete ADSL transceiver and multiple LAN interfaces allowing multiple medium exploitation. The data traffic can be routed through a local terminal by using the LAN/WLAN ports or the USB port. A comprehensive software package is available with the SOC solution. The solution has been developed with the customization in mind. Several software license plans are proposed as well as a user friendly development environment.

Figure 2. BLOCK DIAGRAM
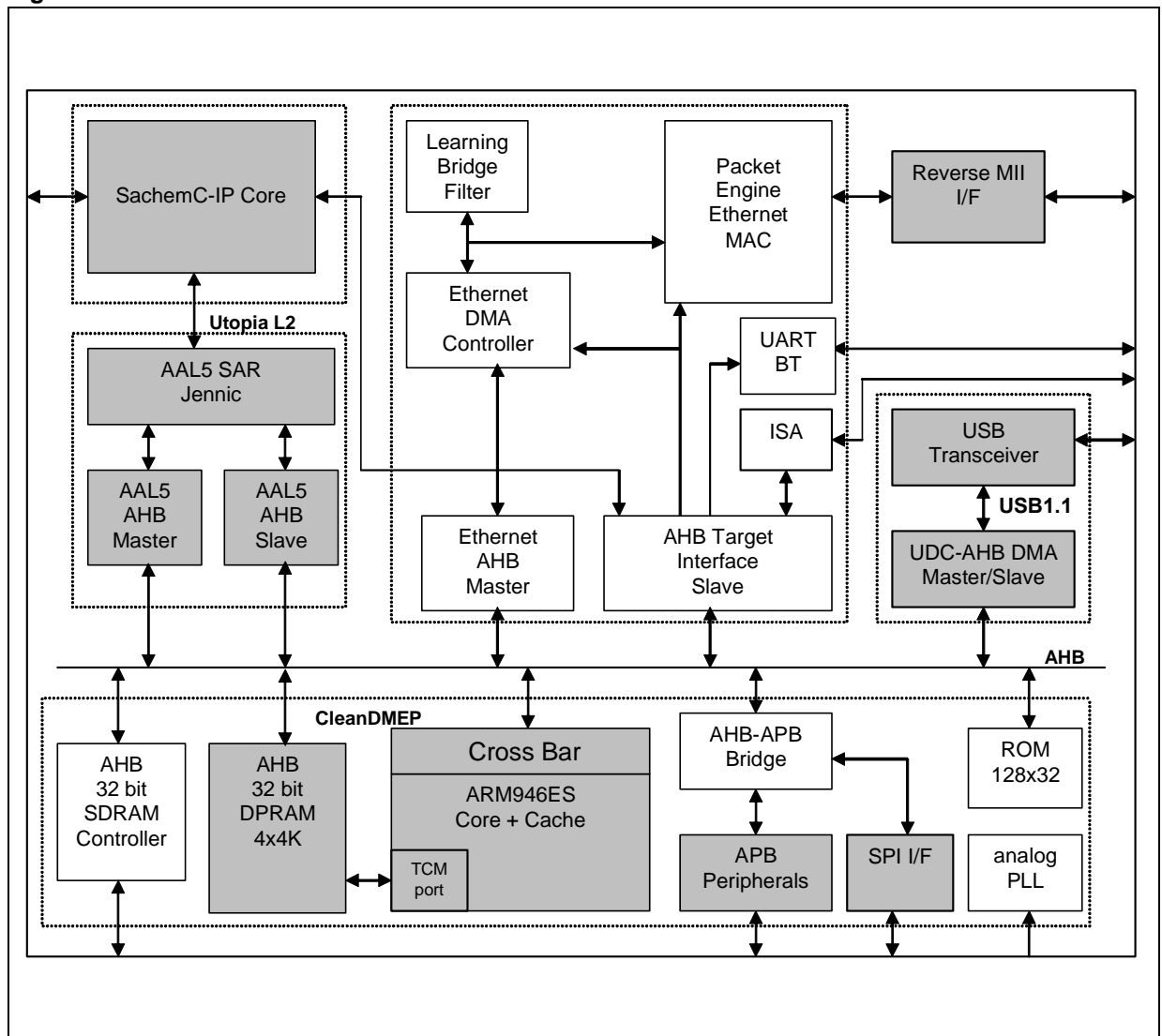
4 HARDWARE DESCRIPTION

The ST50160 processor combines a DynaMiTe™ ADSL transceiver with a dedicated ARM946ES RISC processor. In order to maintain high data throughput, a16Kbyte Cache memory for program and a 16Kbyte memory for data are attached to the RISC processor. The processing of most of the layer 2 protocols on the ATM (SAR and AAL) and IP (Mac filter and bridge) sides are performed by specific hardware blocks, relieving the processors from these tasks. The chip provides minimal external components and maximum flexibility. The chip contains one Ethernet 10/100 Base-T MAC. The exposed MII interface allows the connection to alternate LAN mediums like HPNA and HPLUG. A USB interface allows an easy serial connection. The USB port is bridged with the Ethernet MAC. A specific interface allow the connection of wireless LAN transceiver line 802.11b, Wifi. The ST50160 device is targeted for low-cost residential gateway. Its primary design goal is to minimize cost. Secondary design goals are:

- Low system cost solution (reduced BOM, optimized SOC technology)
- Low power to facilitate primary service capabilities and thermal system issues
- Low EMI to simplify packaging and qualification of systems.

4.1 Hardware features

- ARM 946ES RISC processor dedicated to network processing, API and DSL modem control
- Hardware ATM processor: SAR function with AAL5 processing.
- Hardware packet processor: Ethernet MAC, learning and filter bridge.
- One 10/100 Base-T Ethernet MACs with MII interface for external PHY or multi port switch
- One USB port V1.1 compatible (glue-less interface to external transceiver)
- One 802.11b wireless LAN interface.
- One serial or 8(*) or 16(*) bit wide Flash port, ISA compatible. Up to 16Mbyte addressable memory. (*) packaging option.
- One 32 bit wide SDRAM interface with 32Mbyte addressable memory.
- Interface to DynaMiTe™ ADSL analog front end (AFE) chip MTC20174.
- Multi channel DMA engine integrated with peripherals
- Low power: 1.8V +/-10% core voltage, 3.3V +/- 10% I/O voltage
- 128 instructions (32 bits) of boot ROM
- GPIO with support for LED
- Cc-based Multi ICE/compiler support with assembler and debugger
- Software chip and system simulators for software development and debug
- JTAG board-level test interface
- 140MHz system clock (processor cycle clock)
- Sleep mode with wake on LAN wake on WAN feature
- Programmable system frequency clock: 140, 105, 70, 35 and 129MHz (fall back mode).

5 SOFTWARE ARCHITECTURE

The software is organized in 5 clusters.

- User interface API
- System services
- Network services
- TCP/IP socket
- ATM encapsulation
- ATM drivers

A description of the clusters contents is given in the software features section

Figure 3. Embedded software block diagram
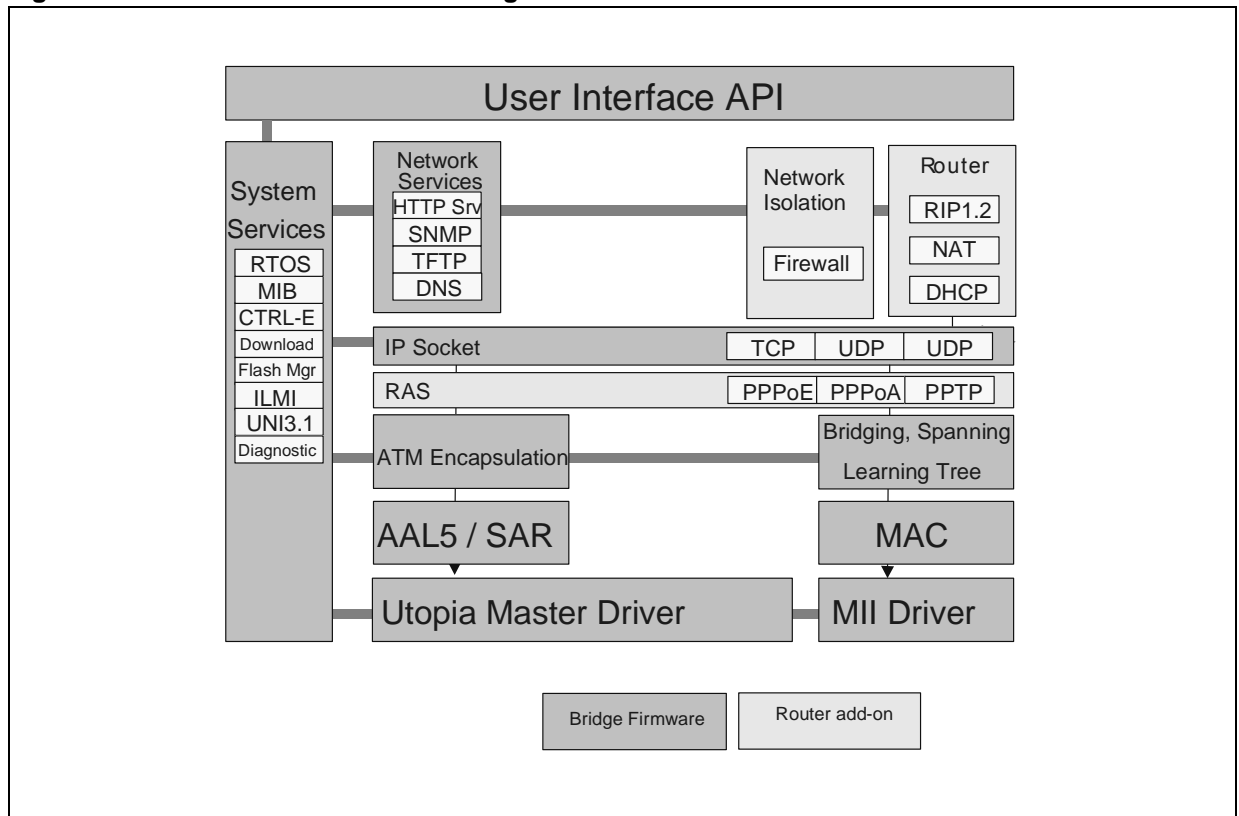
6 SOFTWARE DEVELOPMENT ENVIRONMENT

The ST50160 presents a comprehensive set of software features. In order to allow manufacturer to customize further the system, a set of API functions are made available. The exploitation of the API functions requires the acquisition of a development environment. The development environment is based on the elements depicted hereunder.

– ARM Developer Suite (ADS) v1.1 or higher

– ATI Development license

– ATI EDE (Embedded Development Environment)

– MS Developer Studio (VC++) v6.0 or higher

Along with the development environment a number of specific tools are provided to allow the diagnostic and the downloading operation of the executable on the nonvolatile memory attached to the ST50160.

7 NOMINAL CHARACTERISTICS

The ST50160 processor is available in a 208-pin LBGA (plastic ball grid array) package. All I/Os are 3.3V CMOS levels, with all inputs and 3-states having 5V tolerance. No pins have internal pull-ups and pull-downs.

Supply	- Typical power supply voltage 1.8V - Typical pad power supply voltage 3.3V
Threshold	- Input low voltage -0.5V -1.0V - Input high voltage 2.3V- 5.5V
Consumption	- Core consumption: 1400mW. Reduced power mode available.
Environment	- Commercial grade: 0C - 70C (32F – 158F) - Industrial grade: -45C - 85C. (-49F - 185F)
Packages	- 208-pin plastic BGA package (8/16 bus flash)
Technology	- CMOS 0.18 micron

8 APPLICATION EXAMPLE

The following example shows the reference design developed for the evaluation board. It is a complete ADSL-based data gateway kit connecting to an ADSL enabled phone jack and provides a connection to a 10/100bT Ethernet port. It utilizes a set of 2 ASSP available from ST.

The ST50160 is composed of the following elements: A DynaMiTe™ ADSL modem AFE (MTC2074). Additional components are SDRAM and Flash memory. Discrete components and connectors are not shown on the block diagram. Larger SDRAM can be connected to the ST50160 to store and execute additional (custom) application.

Figure 4. Application Block Diagram
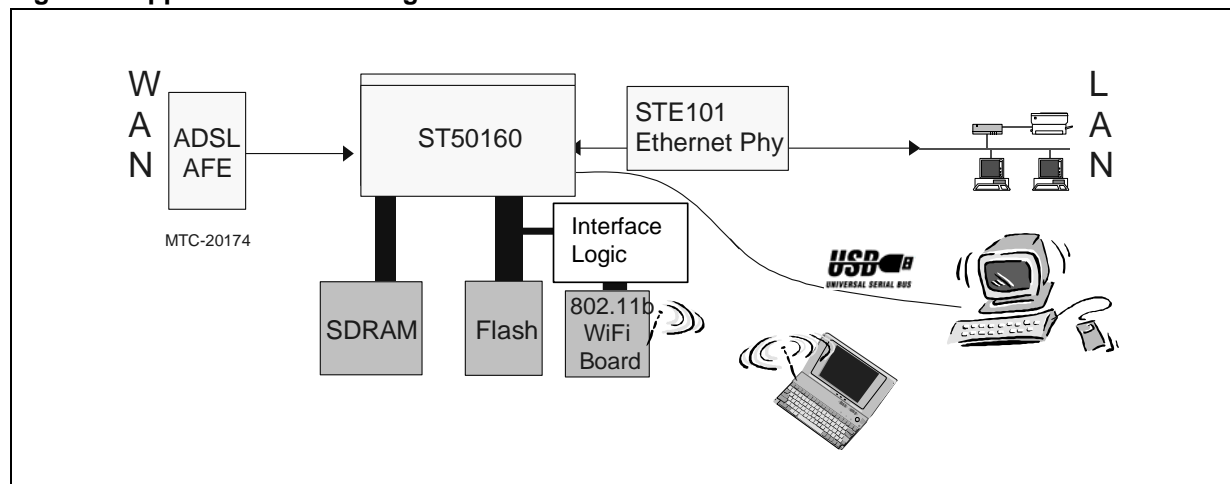
Intensive qualification efforts have been spent on this reference design insuring users of the platform maximum interoperability and smooth, rapid design-in, hence reducing engineering effort and Total Time to Market (TTM).

Table 2. Pin List

Name	Pin BGA 208	B	Buffer Type	Description
SDRAM Interface (57)				
SD_nRAS	N2	O	PRT08DGZ	SDRAM Row Address Strobe
SD_CLK	P2	B	PRB08DGZ	SDRAM Clock
SD_nCAS	N1	O	PRT08DGZ	SDRAM Column Address Strobe
SD_nWE	N3	O	PRT08DGZ	SDRAM Write Strobe
SD_D31 / FS CLK #16	R8	BD	PRDW08DGZ	SDRAM Data Bit 31 / Full Scan Clock #16
SD_D30 / FS CLK #17	T8	BD	PRDW08DGZ	SDRAM Data Bit 30 / Full Scan Clock #17
SD_D29 / FS_IN #16	P8	BD	PRDW08DGZ	SDRAM Data Bit 29 / Full Scan Input #16
SD_D28	N8	BD	PRDW08DGZ	SDRAM Data Bit 28
SD_D27	T9	BD	PRDW08DGZ	SDRAM Data Bit 27
SD_D26	R9	BD	PRDW08DGZ	SDRAM Data Bit 26
SD_D25	N10	BD	PRDW08DGZ	SDRAM Data Bit 25
SD_D24	P10	BD	PRDW08DGZ	SDRAM Data Bit 24
SD_D23	T10	BD	PRDW08DGZ	SDRAM Data Bit 23
SD_D22	T11	BD	PRDW08DGZ	SDRAM Data Bit 22
SD_D21	R11	BD	PRDW08DGZ	SDRAM Data Bit 21
SD_D20	N12	BD	PRDW08DGZ	SDRAM Data Bit 20
SD_D19	P12	BD	PRDW08DGZ	SDRAM Data Bit 19
SD_D18	T12	BD	PRDW08DGZ	SDRAM Data Bit 18
SD_D17	R12	BD	PRDW08DGZ	SDRAM Data Bit 17
SD_D16	P13	BD	PRDW08DGZ	SDRAM Data Bit 16
SD_A0	T7	O	PRT08DGZ	SDRAM Address Bit 00
SD_A1	N6	O	PRT08DGZ	SDRAM Address Bit 01
SD_A2	P6	O	PRT08DGZ	SDRAM Address Bit 02
SD_A3	T6	O	PRT08DGZ	SDRAM Address Bit 03
SD_A4	R6	O	PRT08DGZ	SDRAM Address Bit 04
SD_A5	T5	O	PRT08DGZ	SDRAM Address Bit 05
SD_A6	R5	O	PRT08DGZ	SDRAM Address Bit 06
SD_A7	N4	O	PRT08DGZ	SDRAM Address Bit 07
SD_A8	T4	O	PRT08DGZ	SDRAM Address Bit 08
SD_A9	P4	O	PRT08DGZ	SDRAM Address Bit 09
SD_A10	R4	O	PRT08DGZ	SDRAM Address Bit 10
SD_A11	T3	O	PRT08DGZ	SDRAM Address Bit 11
SD_A12	R3	O	PRT08DGZ	SDRAM Address Bit 12
SD_A13	T2	O	PRT08DGZ	SDRAM Address Bit 13
SD_A14	T1	O	PRT08DGZ	SDRAM Address Bit 14
SD_D15	G1	BD	PRDW08DGZ	SDRAM Data Bit 15
SD_D14	G3	BD	PRDW08DGZ	SDRAM Data Bit 14
SD_D13	G4	BD	PRDW08DGZ	SDRAM Data Bit 13
SD_D12	H2	BD	PRDW08DGZ	SDRAM Data Bit 12
SD_D11	H1	BD	PRDW08DGZ	SDRAM Data Bit 11

Table 2. Pin List (continued)

Name	Pin BGA 208	B	Buffer Type	Description
SD_D10	H3	BD	PRDW08DGZ	SDRAM Data Bit 10
SD_D9	H4	BD	PRDW08DGZ	SDRAM Data Bit 09
SD_D8	J4	BD	PRDW08DGZ	SDRAM Data Bit 08
SD_D7	J2	BD	PRDW08DGZ	SDRAM Data Bit 07
SD_D6	K4	BD	PRDW08DGZ	SDRAM Data Bit 06
SD_D5	K3	BD	PRDW08DGZ	SDRAM Data Bit 05
SD_D4	K1	BD	PRDW08DGZ	SDRAM Data Bit 04
SD_D3	L4	BD	PRDW08DGZ	SDRAM Data Bit 03
SD_D2	L3	BD	PRDW08DGZ	SDRAM Data Bit 02
SD_D1	L1	BD	PRDW08DGZ	SDRAM Data Bit 01
SD_D0	L2	BD	PRDW08DGZ	SDRAM Data Bit 00
SD_nCS	P1	O	PRT08DGZ	SDRAM Chip Select
SD_CKE	R1	O	PRT08DGZ	SDRAM Clock Enable
SD_DQM0	M1	O	PRT08DGZ	SDRAM Data Mask 0 (Byte Enable)
SD_DQM1	M2	O	PRT08DGZ	SDRAM Data Mask 1 (Byte Enable)
SD_DQM2	P7	O	PRT08DGZ	SDRAM Data Mask 2 (Byte Enable)
SD_DQM3	N7	O	PRT08DGZ	SDRAM Data Mask 3 (Byte Enable)
ARM/Miscellaneous Interface (3)				
ARMDEBUG	B7	I	PDIDGZ	ARM Debug Test mode (multiplexes the ARM TAP onto the JTAG pins) Tied to '0' in functional mode (JTAG TAP mode) Input with pad monitor only (JTAG compliancy pin)
FLASHBOOT / PLL_CTR_RUN / FS CLK #1	A7	I / I / I	PDIDGZ	Boot from external parallel Flash PROM (ISA) rather than from internal ROM (UART or SPI) / Starts/Stops the PLL test counter Tied to '1' in functional mode Full Scan Clock #1 Input with BS only
BYPASSPLL / FS IN #1	C5	I / I	PDIDGZ	Bypass CPU clock generation PLL Tied to '0' in functional mode Full Scan Input #1 With BS and padmonitor
JTAG/Test Interface (5)				
TCK	E3	IU	PDUWDGZ	Boundary ScanTest Clock
TDI	F3	IU	PDUWDGZ	Boundary Scan Test Data In
TDO	E1	OZ	PRT08DGZ	Boundary Scan Test Data Out
TMS	E4	IU	PDUWDGZ	Boundary Scan Test Mode Shift
NTRST	F4	ID	PDDWDGZ	Boundary Scan Reset
ADSL Interface (13)				
AF_RXD3 / FS CLK #2	B1	I / I	PDIDGZ	ADSL AFE Receive Data Bit 3 / Full Scan Clock #2
AF_RXD2 / FS CLK #3	A1	I / I	PDIDGZ	ADSL AFE Receive Data Bit 2 / Full Scan Clock #3
AF_RXD1 / FS CLK #4	A2	I / I	PDIDGZ	ADSL AFE Receive Data Bit 1 / Full Scan Clock #4
AF_RXD0 / FS CLK #5	B3	I / I	PDIDGZ	ADSL AFE Receive Data Bit 0 / Full Scan Clock #5

Table 2. Pin List (continued)

Name	Pin BGA 208	B	Buffer Type	Description
AF_TXD3 / FS OUT #11	E2	O / O	PRT08DGZ	ADSL AFE Transmit Data Bit 3 / Full Scan Out #11
AF_TXD2 / FS OUT #12	D4	O / O	PRT08DGZ	ADSL AFE Transmit Data Bit 2 / Full Scan Out #12
AF_TXD1 / FS OUT #13	D1	O / O	PRT08DGZ	ADSL AFE Transmit Data Bit 1 / Full Scan Out #13
AF_TXD0 / FS OUT #14	D3	O / O	PRT08DGZ	ADSL AFE Transmit Data Bit 0 / Full Scan Out #14
AF_CLWD / FS CLK #6	C1	I / I	PDIDGZ	ADSL Start Of Word Indication / Full Scan Clock #6
AF_CTRLDATA / FS OUT #16	C2	O / O	PRT08DGZ	ADSL Serial Data Transmit Channel / Full Scan Out #16
MCLK	B4	IS	PDISDGZ	ADSL Master Clock
MnRST	A3	IS	PDISDGZ	ADSL Master (Chip) Reset
AF_nPOWERLOW/ FS OUT #15	D2	O / O	PRT08DGZ	ADSL Power Down Analog FrontEnd (Active High) / Full Scan Out #15
Ethernet MII/Reverse MII Interface (18)				
M_TXCLK	P15	IS	PDISDGZ	MII Transmit Clock
M_TXEN / FS OUT #9 PLL_DIV_OUT	T14	O / O	PRT08DGZ	MII / Reverse MII Transmit Enable / Full Scan Out #9 / Divided clock in PLL test mode
M_TXD3 / FS OUT #8	R14	O / O	PRT08DGZ	MII / Reverse MII Transmit Data Bit 3 / Full Scan Out #8
M_TXD2 / FS OUT #7	T15	O / O	PRT08DGZ	MII / Reverse MII Transmit Data Bit 2 / Full Scan Out #7
M_TXD1 / FS OUT #6	T16	O / O	PRT08DGZ	MII / Reverse MII Transmit Data Bit 1 / Full Scan Out #6
M_TXD0 / FS OUT #5	R16	O / O	PRT08DGZ	MII / Reverse MII Transmit Data Bit 0 / Full Scan Out #5
M_TXER / FS OUT #10 PLL_NOM_OUT	T13	O / O	PRT08DGZ	MII / Reverse MII Transmit Error / Full Scan Out #10 / PLL output clock in PLL test mode
M_CRS/ FS_IN #15	M14	BD ID	PRDW08DGZ	MII / Reverse MII Carrier Sense / Full Scan Input #15
M_COL / FS IN #14	M13	BD ID	PRDW08DGZ	MII / Reverse MII Collision Detection / Full Scan Input #14
M_RXCLK	N15	IS	PDISDGZ	MII Receive Clock
M_RXDV / FS CLK #7	P16	I / I	PDIDGZ	MII / Reverse MII Receive Data Valid / Full Scan Clock #7
M_RXD3 / FS CLK #8	N14	I / I	PDIDGZ	MII / Reverse MII Receive Data Bit 3 / Full Scan Clock #8
M_RXD2 / FS CLK #9	N16	I / I	PDIDGZ	MII / Reverse MII Receive Data Bit 2 / Full Scan Clock #9
M_RXD1 / FS CLK #10	N13	I / I	PDIDGZ	MII / Reverse MII Receive Data Bit 1 / Full Scan Clock #10
M_RXD0 / FS CLK #11	M15	I / I	PDIDGZ	MII / Reverse MII Receive Data Bit 0 / Full Scan Clock #11
M_RXER / FS CLK #12	M16	I / I	PDIDGZ	MII / Reverse MII Receive Error / Full Scan Clock #12

Table 2. Pin List (continued)

Name	Pin BGA 208	B	Buffer Type	Description
M_MDC	L14	B	PRB08DGZ	MII / Reverse MII Management Clock
M_MDIO / FS IN #13	L13	B / I	PRB08DGZ	MII / Reverse MII Management Data / Full Scan Input #13 **External pull down resistor of 2 K is required**
GPIO Interface (11)				
GPIO10 / FCS2 /	-	BD O	PRDW08DGZ	General Purpose Pin 10 / Serial Flash Chip Select #2 /
GPIO9 /	-	BD/	PRDW08DGZ	General Purpose Pin 9 /
GPIO8 /	-	BU/ I	PRUW08DGZ	General Purpose Pin 8 / Boot from UART or SPI
GPIO7 /	-	BU / I	PRUW08DGZ	General Purpose Pin 7 / Boot from UART or SPI
GPIO6 / SER2SI / FS IN #6	H16	B / I / O / I	PRB08DGZ	General Purpose Pin 6 / CleanDMEP Serial Interface 2 – serial input / ISA-Like Interface Reset Output Full Scan Input #6
GPIO5 / SER2SO / FS IN #7	H14	B / O / I / I	PRB08DGZ	General Purpose Pin 5 / CleanDMEP Serial Interface 2 – serial output / Restore Defaults/Version Select Input Full Scan Input #7
GPIO4 / M_LINK/ FS IN #8	F16	B / I / I / I	PRB08DGZ	General Purpose Pin 4 / Ethernet Link Status Input / ISA-Like Interface IREQ# Full Scan Input #8
GPIO3 / PB1/ FS IN #9	F14	B / O / I / I	PRB08DGZ	General Purpose Pin 3 / Main Clock Control PB1 / Dying Gasp interrupt input / Full Scan Input #9
GPIO2 / PB0 / FS IN #10	A13	B / O / O / I	PRB08DGZ	General Purpose Pin 2 / Main Clock Control PB0 / Software reset ouput / Full Scan Input #10
GPIO1 / SI_RCLK / SER2nCTS/ FS IN #11	F13	B / I / I / I	PRB08DGZ	General Purpose Pin 1 / External UART (BT) Clock / CleanDMEP Serial Interface 2 nRTS / Full Scan Input #11
GPIO0 / SER2nRTS / FS IN #12	G16	B / O / O / I	PRB08DGZ	General Purpose Pin 0 / ISA-Like Interface A6 CleanDMEP Serial Interface 2 nCTS / Full Scan Input #12
SPI (Serial Flash Interface) (4)				
SPI_CS \	-	O /	PRT08DGZ	Flash Chip select #1
SPI_CLK /	-	O /	PRT08DGZ	SPI Clock
SPI_TXD /	-	O /	PRT08DGZ	SPI Transmit Data (to Serial Flash)
SPI_RXD /	-	ID /	PDDWDGZ	SPI Receive Data (from Serial Flash)
UART1/UART_BT SI Serial Interface (4)				
SI_SIN / SER1SI / FS CLK #14	C7	I / I	PDIDGZ	Serial Interface Serial Data Input / CleanDMEP Serial Interface 1 – serial input / Full Scan Clock #14

Table 2. Pin List (continued)

Name	Pin BGA 208	B	Buffer Type	Description
SI_SOUT / SER1SO	B8	O	PRT08DGZ	Serial Interface Serial Data Output / Andtree output CleanDMEP Serial Interface 1 – serial output
SI_nRTS / SER1nRTS / FS OUT #1	A8	O / O	PRT08DGZ	Serial Interface Not Ready To Send / CleanDMEP Serial Interface 1 nRTS / Full Scan Output #1
SI_nCTS / SER1nCTS / FS CLK #15	D7	I / I	PDIDGZ	Serial Interface Not Clear To Send / CleanDMEP Serial Interface 1 nCTS / Full Scan Clock #15
ISA-like Interface (42)				
ISA_nCS	H15	O	PRT08DGZ	ISA bus Chip Select / Address Enable With BS - deactivated by nSEL_ISA
ISA_nRD / **FS OUT #4**	B13	O	PRT08DGZ	ISA bus Read Strobe / Output Enable With BS - deactivated by nSEL_ISA / **Full Scan Out #4**
ISA_nWR / **FS OUT #3**	C13	O	PRT08DGZ	ISA bus Write Strobe With BS - deactivated by nSEL_ISA / **Full Scan Out #3**
ROM_nCS / **FS OUT #2**	A14	O	PRT08DGZ	Flash PROM Chip Select / Address Enable With BS - deactivated by nSEL_ISA / **Full Scan Out #2**
ROM_ADDR21	D14	O	PRT08DGZ	Flash PROM Address Bit 21 With BS - deactivated by nSEL_ISA
ROM_ADDR20	E15	O	PRT08DGZ	Flash PROM Address Bit 20 With BS - deactivated by nSEL_ISA
ROM_ADDR19	E16	O	PRT08DGZ	Flash PROM Address Bit 19 With BS - deactivated by nSEL_ISA
ROM_ADDR18	E14	O	PRT08DGZ	Flash PROM Address Bit 18 With BS - deactivated by nSEL_ISA
ROM_ADDR17	G14	O	PRT08DGZ	Flash PROM Address Bit 17 With BS - deactivated by nSEL_ISA
ROM_ADDR16	G13	O	PRT08DGZ	Flash PROM Address Bit 16 With BS - deactivated by nSEL_ISA
ROM_ADDR15	D13	O	PRT08DGZ	Flash PROM Address Bit 15 With BS - deactivated by nSEL_ISA
ROM_ADDR14	B12	O	PRT08DGZ	Flash PROM Address Bit 14 With BS - deactivated by nSEL_ISA
ROM_ADDR13	A12	O	PRT08DGZ	Flash PROM Address Bit 13 With BS - deactivated by nSEL_ISA
ROM_ADDR12	C12	O	PRT08DGZ	Flash PROM Address Bit 12 With BS - deactivated by nSEL_ISA
ROM_ADDR11	A11	O	PRT08DGZ	Flash PROM Address Bit 11 With BS - deactivated by nSEL_ISA
ROM_ADDR10	C11	O	PRT08DGZ	Flash PROM Address Bit 10 With BS - deactivated by nSEL_ISA
ROM_ADDR9	B10	O	PRT08DGZ	Flash PROM Address Bit 9 With BS - deactivated by nSEL_ISA
ROM_ADDR8	A10	O	PRT08DGZ	Flash PROM Address Bit 8 With BS - deactivated by nSEL_ISA

Table 2. Pin List (continued)

Name	Pin BGA 208	B	Buffer Type	Description
ROM_ADDR7	C10	O	PRT08DGZ	Flash PROM Address Bit 7 With BS - deactivated by nSEL_ISA
ROM_ADDR6	D10	O	PRT08DGZ	Flash PROM Address Bit 6 With BS - deactivated by nSEL_ISA
ROM_ADDR5	A9	O	PRT08DGZ	Flash PROM Address Bit 5 With BS - deactivated by nSEL_ISA
ISA_ADDR4 / ROM_ADDR4	B9	O	PRT08DGZ	ISA / Flash PROM Address Bit 4 With BS - deactivated by nSEL_ISA
ISA_ADDR3 / ROM_ADDR3	C9	O / O	PRT08DGZ	ISA / Flash PROM Address Bit 3 With BS - deactivated by nSEL_ISA
ISA_ADDR2 / ROM_ADDR2	D9	O / O	PRT08DGZ	ISA / Flash PROM Address Bit 2 With BS - deactivated by nSEL_ISA
ISA_ADDR1 / ROM_ADDR1	D8	O / O	PRT08DGZ	ISA / Flash PROM Address Bit 1 With BS - deactivated by nSEL_ISA
ISA_ADDR0 / ROM_ADDR0	C8	O / O	PRT08DGZ	ISA / Flash PROM Address Bit 0 With BS - deactivated by nSEL_ISA
ISA_DATA15 / ROM_ADDR23	H13	BD/ O	PRDW08DGZ	ISA / Flash PROM Data bus Bit 15 / Flash PROM Address bit 23 in 8 bit mode With BS&Andtree - deactivated by nSEL_ISA
ISA_DATA14 / ROM_ADDR22	J13	BD/ O	PRDW08DGZ	ISA / Flash PROM Data bus Bit 14 / Flash PROM Address bit 22 in 8 bit mode/ With BS&Andtree - deactivated by nSEL_ISA
ISA_DATA13	-	BD	PRDW08DGZ	ISA / Flash PROM Data bus Bit 13 With BS&Andtree - activated by SEL_ISA16 when nSEL_ISA active
ISA_DATA12	-	BD	PRDW08DGZ	ISA / Flash PROM Data bus Bit 12 With BS&Andtree - activated by SEL_ISA16 when nSEL_ISA active
ISA_DATA11	-	BD	PRDW08DGZ	ISA / Flash PROM Data bus Bit 11 With BS&Andtree - activated by SEL_ISA16 when nSEL_ISA active
ISA_DATA10	-	BD	PRDW08DGZ	ISA / Flash PROM Data bus Bit 10 With BS&Andtree - activated by SEL_ISA16 when nSEL_ISA active
ISA_DATA9	-	BD	PRDW08DGZ	ISA / Flash PROM Data bus Bit 9 With BS&Andtree - activated by SEL_ISA16
ISA_DATA8	-	BD	PRDW08DGZ	ISA / Flash PROM Data bus Bit 8 With BS&Andtree - activated by SEL_ISA16
ISA_DATA7	B14	BD	PRDW08DGZ	ISA / Flash PROM Data bus Bit 7 With BS&Andtree - deactivated by nSEL_ISA
ISA_DATA6 /	A15	BD	PRDW08DGZ	ISA / Flash PROM Data bus Bit 6 With BS&Andtree - deactivated by nSEL_ISA
ISA_DATA5 /	A16	BD	PRDW08DGZ	ISA / Flash PROM Data bus Bit 5 With BS&Andtree - deactivated by nSEL_ISA
ISA_DATA4 / **FS IN #2**	B16	BD	PRDW08DGZ	ISA / Flash PROM Data bus Bit 4 With BS&Andtree - deactivated by nSEL_ISA **Full Scan Input #2**
ISA_DATA3 / **FS IN #3**	C15	BD	PRDW08DGZ	ISA / Flash PROM Data bus Bit 3 With BS&Andtree - deactivated by nSEL_ISA **Full Scan Input #3**

Table 2. Pin List (continued)

Name	Pin BGA 208	B	Buffer Type	Description
ISA_DATA2 / **FS IN #4**	C16	BD	PRDW08DGZ	ISA / Flash PROM Data bus Bit 2 With BS&Andtree - deactivated by nSEL_ISA **Full Scan Input #4**
ISA_DATA1 / **FS IN #5**	D16	BD	PRDW08DGZ	ISA / Flash PROM Data bus Bit 1 With BS&Andtree - deactivated by nSEL_ISA **Full Scan Input #5**
ISA_DATA0 / **FS CLK #13**	D15	BD	PRDW08DGZ	ISA / Flash PROM Data bus Bit 0 With BS&Andtree - deactivated by nSEL_ISA **Full Scan Clock #13**
USB Interface (5)				
USB_DP	J15	B	PUSBF11DG	USB Data +
USB_DM	J16	B		USB Data -
USB_CLK	J14	IS	PDISDGZ	48 MHz UDC input clock
VDD_AN_USB	K14	P	PVDD6DG	3.3V (AUVDD)
VSS_AN_USB	K13	P	PVSS6DG	0 V (not common with VSS_CORE or VSS_IO) (AUVSS)
Miscellaneous Test Pins (4)				
IDDQMode	C6	I	PDIDGZ	IDDQ mode activation with padmonitor only (Jtag compliancy pin)
FSSHIFT	A6	ID	PDDWDGZ	Full Scan Shift Enable with padmonitor only (Jtag compliancy pin)
SELECT106M	-	ID	PDDWDGZ	Activates 106 MHz CPU clock if connected to '1', with padmonitor only (Jtag compliancy pin)
SELECT70M	-	ID	PDDWDGZ	Activates 70 MHz CPU clock if connected to '1', with padmonitor only (Jtag compliancy pin)
Core Power Supply Pins (26) [1.8V]				
VDD_CORE	F2 K2 R2 P5 N9 R10 R15 L15 E13 B15 D12 B6 B2	P	PVDD1DGZ	1.8V (VDD)
VSS_CORE	F1 N5 P9 K10 L16 F15 G10 B11 D5 G9 H9 J10 H10	P	PVSS3DGZ	0 V, common with VSS_IO (VSS)

Table 2. Pin List (continued)

Name	Pin BGA 208	B	Buffer Type	Description
I/O Power Supply Pins (26) [3.3V]				
VDD_IO	C3 G2 J3 M3 P3 R7 N11 P14 K15 G15 C14 D11 D6 K16	P	PVDD2DGZ	3.3 V (VD33)
VSS_IO	H8 H7 J1 M4 K7 K8 P11 J9 G8 G7 J7 J8 K9 R13	P	PVSS3DGZ	0 V, common with VSS_CORE (VSS)
PLL Digital and Analog Power Supply Pins (4) [1.8V]				
VDD_DIG_PLL	A5	P	PVDD1P PVDD5P	1.8V (DVDD)
VSS_DIG_PLL	B5	P	PVSS1P PVSS5P	0 V (not common with VSS_CORE or VSS_IO) (DVSS)
VDD_AN_PLL	A4	P	PVDD1P	1.8V (AVDD)
VSS_AN_PLL	C4	P	PVSS1P	0 V (not common with VSS_CORE or VSS_IO) (AVSS)
Unconnected Pads with an internal pull-down resistor				
SWMODE0	-	ID	PDDWDGZ	do not bond; '0' default value, bond to nearby VDD_IO to get '1' value (allow SW to differentiate between Bridge/Router mode) Input with pad monitor only
SELRSTDLY	-	ID	PDDWDGZ	do not bond; '0' default value; bond to nearby VDD_IO to get '1' value (activates prolonged external reset delay) Input with pad monitor only
SEL_C184	-	ID	PDDWDGZ	do not bond; '0' default value, bond to nearby VDD_IO to get '1' value (activates IOs & test logic for C184 support) Input with pad monitor only

Table 2. Pin List (continued)

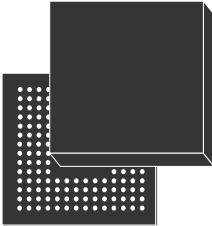| Name	Pin BGA 208	B	Buffer Type	Description
nSEL_ISA	-	ID	PDDWDGZ	**Do not bond** '0' default value; activates IOs & test logic for 8 bit parallel flash support **Bond to nearby VDD_IO (K14) in BGA180** Desactivates IOs & test logic for parallel flash support Input with pad monitor only
SEL_ISA16	-	ID	PDDWDGZ	do not bond; '0' default value; bond to nearby VDD_IO to get '1' value (activates IOs & test logic for 16 bit parallel flash support when nSEL_ISA is not bonded). This feature might be activates for higher pincount package (256BGA). Input with pad monitor only
SEL_SPI	-	ID	PDDWDGZ	**Do not bond** '0' default value; desactivates IOs & test logic for serial flash support **Bond to nearby VDD_IO (B13) in BGA180** Activates IOs & test logic for serial flash support Input with pad monitor only
AF_RXD4	-	ID	PDDWDGZ	ADSL AFE Receive Data Bit4 With BS&Andtree - activated by SEL_C184
AF_RXD5	-	ID	PDDWDGZ	ADSL AFE Receive Data Bit5 With BS&Andtree - activated by SEL_C184
AF_RXD6	-	ID	PDDWDGZ	ADSL AFE Receive Data Bit6 With BS&Andtree - activated by SEL_C184
AF_RXD7	-	ID	PDDWDGZ	ADSL AFE Receive Data Bit7 With BS&Andtree - activated by SEL_C184
AF_RXD8	-	ID	PDDWDGZ	ADSL AFE Receive Data Bit8 With BS&Andtree - activated by SEL_C184
AF_RXD9	-	ID	PDDWDGZ	ADSL AFE Receive Data Bit9 With BS&Andtree - activated by SEL_C184
AF_CTRLDATA_IN	-	ID	PDDWDGZ	ADSL Serial Data Receive Channel With BS&Andtree - activated by SEL_C184

Figure 5.
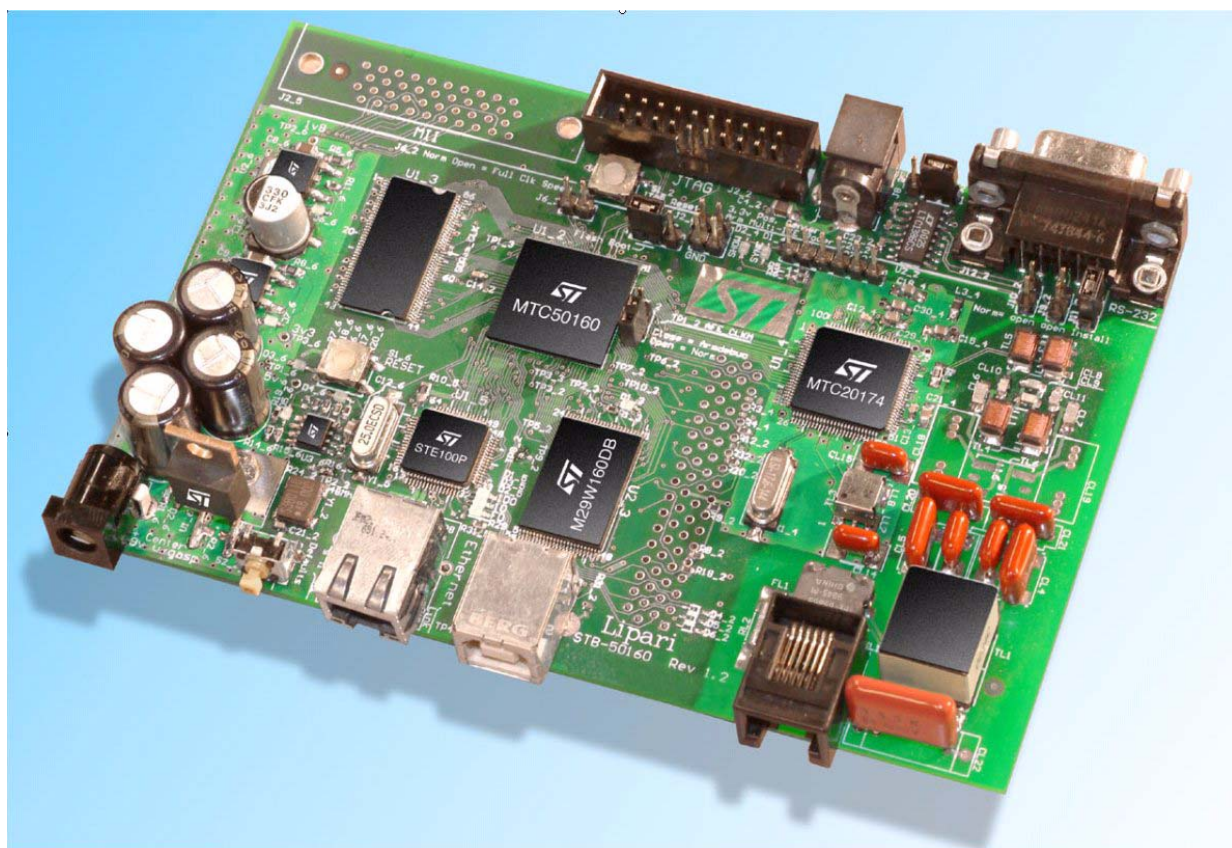
Figure 6. LBGA208 (17x17x1.7mm) Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.210		1.700	0.048		0.067
A1	0.270			0.011		
A2		1.120			0.044	
b	0.450	0.500	0.550	0.018	0.020	0.022
D	16.80	17.00	17.20	0.661	0.669	0.677
D1		15.00			0.590	
E	16.80	17.00	17.20	0.661	0.669	0.677
E1		15.00			0.590	
e	0.90	1.00	1.10	0.035	0.039	0.043
f	0.75	1.00	1.250	0.029	0.039	0.049
ddd			0.200			0.008

OUTLINE AND MECHANICAL DATA

**LBGA208 (17x17x1.70)
Low Profile Ball Grid Array**

ø b (208 BALLS)

A1 CORNER INDEX AREA
(See NOTE 1)

ddd C

16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

A B C D E F G H J K L M N P R T

A1

E E1

e

f

D1

D

A2

C SEATING PLANE

BOTTOM VIEW

NOTE 1
- The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
- A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner.
- Exact shape of each corner is optional.

LBGA208M

7184626B

Table 3. Revision History

Date	Revision	Description of Changes
September 2004	1	First Issue in EDOCS dms.