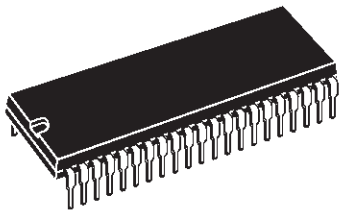
STV8203

MULTISTANDARD TV SOUND DEMODULATOR

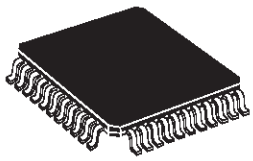
PRELIMINARY DATA

- PERFORMS FM MONO, FM 2 CARRIERS AND NICAM RECEPTION
- B/D/G/H/I/K/K1/K2/L/L'
- UP TO 500kHz DEVIATION FM DEMODULATOR
- ALL PRE AND POST-PROCESSING INTEGRATED FILTERS, ALIGNMENT FREE
- STANDARD RECOGNITION FLAG
- SINGLE QUARTZ CRYSTAL
- I^2C BUS CONTROLLED
- AM AND DOUBLE SCART AUDIO MATRIX
- STAND-BY WITH THRU MODE
- SINGLE BIT DACS
- EASY IMPLEMENTATION OF AUTOSTANDARD MODE
- ADVANCED OPERATING MODE FOR FULL CUSTOMIZATION
- SIF AGC WITH WIDE RANGE



SHRINK42
(Plastic Package)

ORDER CODE : STV8203



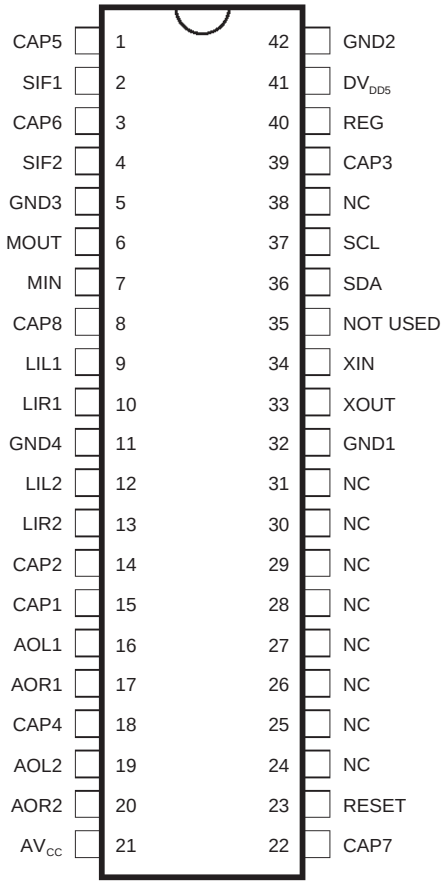
TQFP44 (10 x 10 x 1.4mm)
(Full Plastic Quad Flat Pack)

ORDER CODE : STV8203D

DESCRIPTION

The STV8203 provides all the necessary circuitry for demodulation of all Nicam and German stereo audio transmission. It is very suitable for TV applications as well as for VCR, Personal Computer or Set Top Box applications. Different transmission standards are automatically detected and demodulated without user intervention. The recovered audio signals can be made available in analog form. More, the STV8203 integrates an audio matrix with a THRU mode when the IC is in stand-by. Very flexible applications are possible thanks to smart I^2C program modes and large choice of appropriate audio processing ICs.

SDIP42 PIN CONNECTIONS



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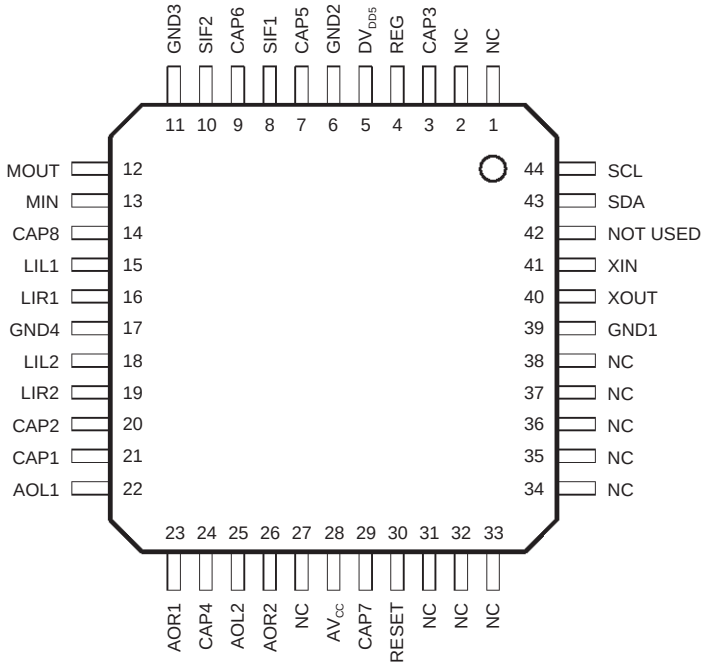
TQFP44 PIN CONNECTIONS



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PIN LIST

Pin Number		Name	Type	Function
SDIP42	TQFP44			
1	7	CAP5	Analog	Decoupling for ADC Supply Regulator Output
2	8	SIF1	Analog	Subcarrier 1 Input
3	9	CAP6	Analog	Decoupling for Input Amplifier Reference
4	10	SIF2	Analog	Subcarrier 2 Input
5	11	GND3	Power	Ground for Input Amplifier
6	12	MOUT	Analog	Mono Audio Output
7	13	MIN	Analog	Mono Audio Input
8	14	CAP8	Analog	ADC Vtop Decoupling
9	15	LIL1	Analog	Line 1 Left Input (SCART 1)
10	16	LIR1	Analog	Line 1 Right Input (SCART 1)
11	17	GND4	Power	Audio Ground
12	18	LIL2	Analog	Line 2 Left Input (SCART 2)
13	19	LIR2	Analog	Line 2 Right Input (SCART 2)
14	20	CAP2	Analog	Decoupling for Audio Matrix
15	21	CAP1	Analog	Decoupling for Bandgap Reference
16	22	AOL1	Analog	Line 1 Left Output (SCART 1)
17	23	AOR1	Analog	Line 1 Right Output (SCART 1)
18	24	CAP4	Analog	Audio Matrix V_{DD} (5V)
19	25	AOL2	Analog	Line 2 Left Output (SCART 2)
20	26	AOR2	Analog	Line 2 Right Output (SCART 2)
-	27	NC	-	Not Connected
21	28	AV_{CC}	Power	Audio Matrix Supply
22	29	CAP7	Analog	Decoupling for Digital Regulator Output
23	30	RESET	Input	Power On Reset
24	31	NC	-	Not Connected
25	32	NC	-	Not Connected
26	33	NC	-	Not Connected
27	34	NC	-	Not Connected
28	35	NC	-	Not Connected
29	36	NC	-	Not Connected
30	37	NC	-	Not Connected
31	38	NC	-	Not Connected
32	39	GND1	Power	Digital Ground
33	40	XOUT	Analog	Crystal Oscillator Output
34	41	XIN	Analog	Crystal Oscillator Input
35	42	Not used	Input	To be connected to ground
36	43	SDA	Bi-directional	I^2C Serial Data
37	44	SCL	Input	I^2C Serial Clock
-	1	NC	-	Not Connected
38	2	NC	-	Not Connected
39	3	CAP3	Analog	Decoupling for Digital 3V (regulator output)
40	4	REG	Analog	Base Drive for External Regulator Transistor
41	5	DV_{DD5}	Power	5V Supply
42	6	GND2	Power	Digital Ground

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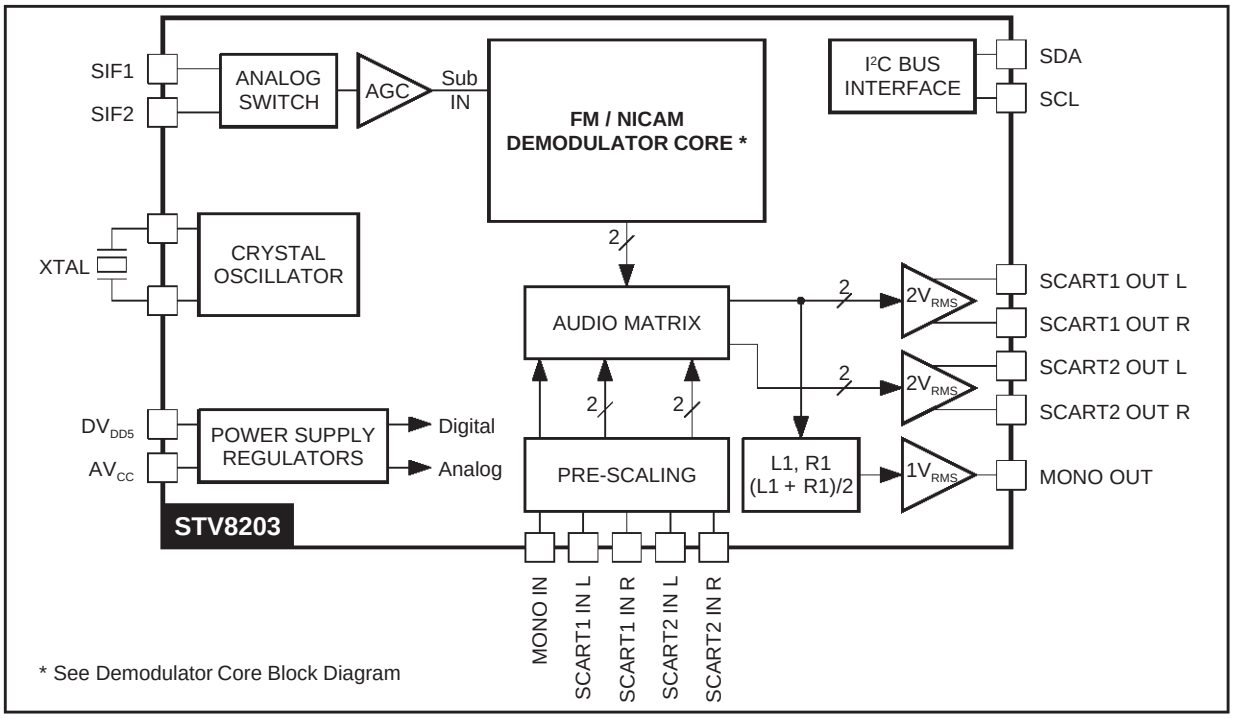
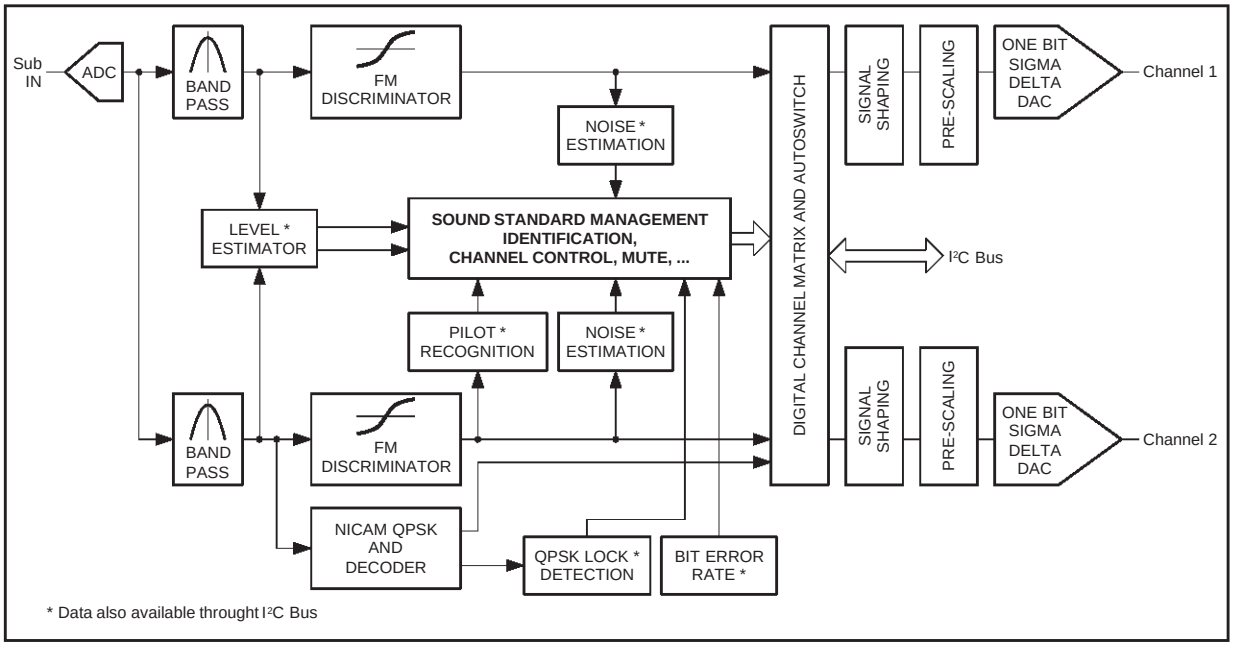
BLOCK DIAGRAM



DEMODULATOR CORE BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

As can be seen from the block diagram, the input to the demodulator section is selectable from one of two I.F. sources via the I^2C bus. The selected signal is then passed through an AGC block, having a range of 28dB, before being digitised in the ADC unit. A single quartz crystal (suggested value : between 24.712MHz and 27MHz) is used for the all the digital processing, including demodulation, identification, control, filtering. This has the advantage of a single clock signal source for the whole IC which eliminates problems of multiple clock. The single clock can be chosen to minimize interference in the TV IF and RF stages of the tuner system.

The demodulator system can identify and demodulate all the standard described in the Table 1. The result of the recognition is flagged up to the host system via the I^2C bus communication system.

In the case of NICAM transmissions, in the event of a failure of the received signal or a degradation of the bit error rate (BER) below a prescribed level, the system will automatically default to the reserve sound transmission on mono FM or AM.

For FM demodulation, the discriminator can normally handle signals having 250kHz deviation. This covers all European standards, and ensure an optimized compromise for the signal to noise ratio in one hand, and over modulation in the other hand. However, it is possible to extand the deviation range up to 500kHz (I^2C programmable) in order to cover requests of some broadcasters.

Fully automatic standard recognition and setting can be achieve using simple routines.

Appropriate de-emphasis networks in the digital domain are applied to the resulting demodulated signals (50µs, J17), followed by dematrixing if required. The digital datastream is then passed through 2 x 16bits DACs before the audio matrix.

All this first section is working at 3.3V thanks to an integrated voltage regulator. In stand-by mode, the voltage regulator pulls the voltage down to zero, ensuring no power dissipation in this part.

An audio matrix allows the selection of inputs applied on the outputs SCART1, SCART2 and MONO according to the diagram shown in Figure 1.

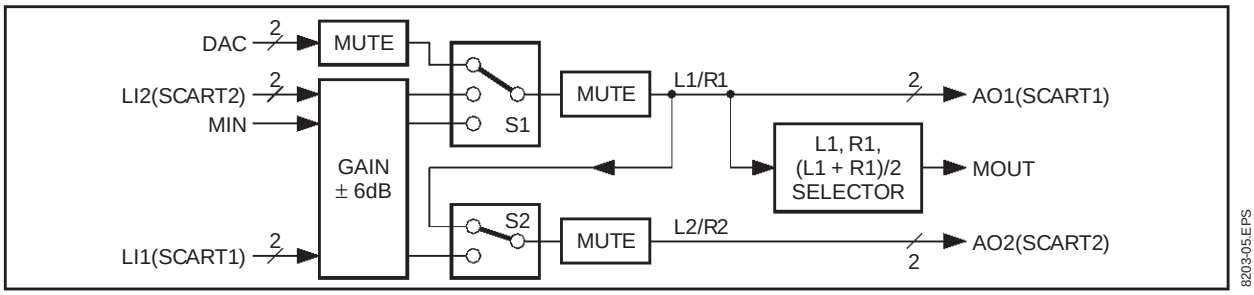
The "MOUT" outputs either the signal L1, or R1 or (L1+R1)/2. This allows to record the selected channel in mono mode, for example on the linear channel of a VCR simultanously with the stereo mode. Maximum output swing is $1V_{RMS}$.

The audio matrix section has its own power supply regulator, allowing to keep this part working even when the rest is in stand-by mode. This achieves a "THRU" mode from input "SCART1" to output "SCART2" and input "SCART2" to output "SCART1".

The maximum output swing of both SCART1 and SCART2 is $2V_{RMS}$.

Remark : Circuit operation is possible with only a single 5V supply. In this case, the AV_{CC} supply pin is connected to 5V. Maximum output swing is then limited to $1V_{RMS}$ and a 6dB attenuation is automatically added to the DAC output. In that case, the resistor shown as R2 = 39Ω in the Application Diagram (between Pin 8 and Pin 21) must be replace by a short circuit to avoid clipping.

Figure 1 : Audio Matrix



FUNCTIONAL DESCRIPTION (continued)

Table 1 : Demodulated TV Sound Norms

System	Sound Type	Type Name	Carrier 1 (kHz)	Carrier 2 (kHz)	FM Deviation (kHz)			Deemphasis	Roll-off	Pilot Frequency (kHz)
					Nom.	Max.	Over			
B/G	FM mono		5.5							
	FM/NICAM		5.5	5.850	27	50	80	J17	40	
	FM 2 carriers	A2	5.5	5.742	27	50	80	50µs		54.6875
B/H	FM/NICAM		5.5	5.850	27	50	80	J17	40	
D/K	FM mono		6.5							
	FM/NICAM		6.5	5.850	27	50	80	J17	40	
D/K1	FM 2 carriers	A2*	6.5	6.258				50µs		54.6875
D/K2	FM 2 carriers		6.5	6.742				50µs		54.6875
I	FM/NICAM		6.0	6.552	27	50	80	J17	100	
	FM mono		6.0					50µs		
L	NICAM		6.5 (1)	5.850				J17	40	
M/N	FM mono		4.5 (2)		15	25	50	(2)		

Notes : 1. STV8203 performs only limited AM demodulation. Report to Application Note.
2. 50µs only, instead of 75µs.

USING STV8203

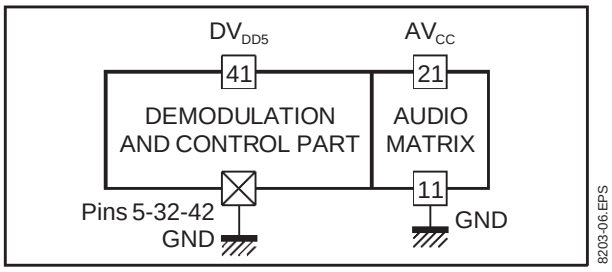
1 - Hardware

1.a - Power Supplies (see Figure 2)

The IC is using two main power supplies :

- DV_{DD5} supplies all the digital part $V_{Nom.}$ = 5V. This power supply can be switched-off in stand-by mode.
- AV_{CC} supplies the audio matrix part : if $V_{Nom.}$ = 8V then the output voltage swing on output pins can reach $2V_{RMS}$, if $V_{Nom.}$ = 5V then the output voltage swing on output pins can reach $1V_{RMS}$.

Figure 2



1.b - Sound Subcarrier Filters

Sound demodulation and decoding are very easy with this device providing all the necessary functions for that purpose, including the channel filters. These FIR base-band filters give the best selectivity of the desired channel and provides in NICAM mode the correct cosine roll-off response.

This implies that no external filters are required (except may be a simple high-pass filter, if the saw filters and sound IF demodulators used in the application create picture interferences).

The filters can be automatically set for B/G/H/I/L/L' standards. They can also be easily tuned through I^2C for M, D, K, K1.

1.c - Audio Matrix

The mono output (MOUT) can output L1, R1 or (L1+R1)/2 signal. A typical application is the possibility to record a selected channel in mono mode on the linear track of a VCR separately from the recording of the stereo signal, providing the facility to select between stereo or mono signals in the playback mode in case of marginal noise conditions.

1.d - Stand-by

Stand-by with THRU mode : the analog part of the device has its own power supply (AV_{CC}) allowing this part to keep working even when the digital part, powered by the 5V power supply (DV_{DD5}), is in stand-by.

In this case, the audio matrix is put in a special setting :

- LIL1 to AOL2,
- LIR1 to AOR2,
- LIL2 to AOL1,
- LIR2 to AOR1,
- input gain = 0dB.

This allows to achieve a "THRU" mode from SCART1 input to SCART2 output and SCART2 input to SCART1 output, providing a copy facility from SCARTIN to SCARTOUT.

2 - Software

Two modes of operation are available :

2.a - Optimized Program Mode

Four standards have default setting stored in order to allow a very easy programmation. Only some registers may have to be programmed (these registers are shown in bold in the Figure 3) but in most cases, the reset values will be sufficient. In Figure 3, CTL and STAT represent registers which are controlled by the "standard processor". These registers are located between address 23Hex and 3CHex in the complete list of registers.

2.b - Advanced Operation Mode

In that mode, all the read/write registers (as mentionned in the complete list) can be programmed manually and changed from their reset values.

The additionnal registers accessible in this mode are shown in bold in Figure 4. This mode can be selected by putting the bits [3:0] of AO-CONTROL register to 0.

USING STV8203 (continued)

Figure 3 : Optimized Program Mode

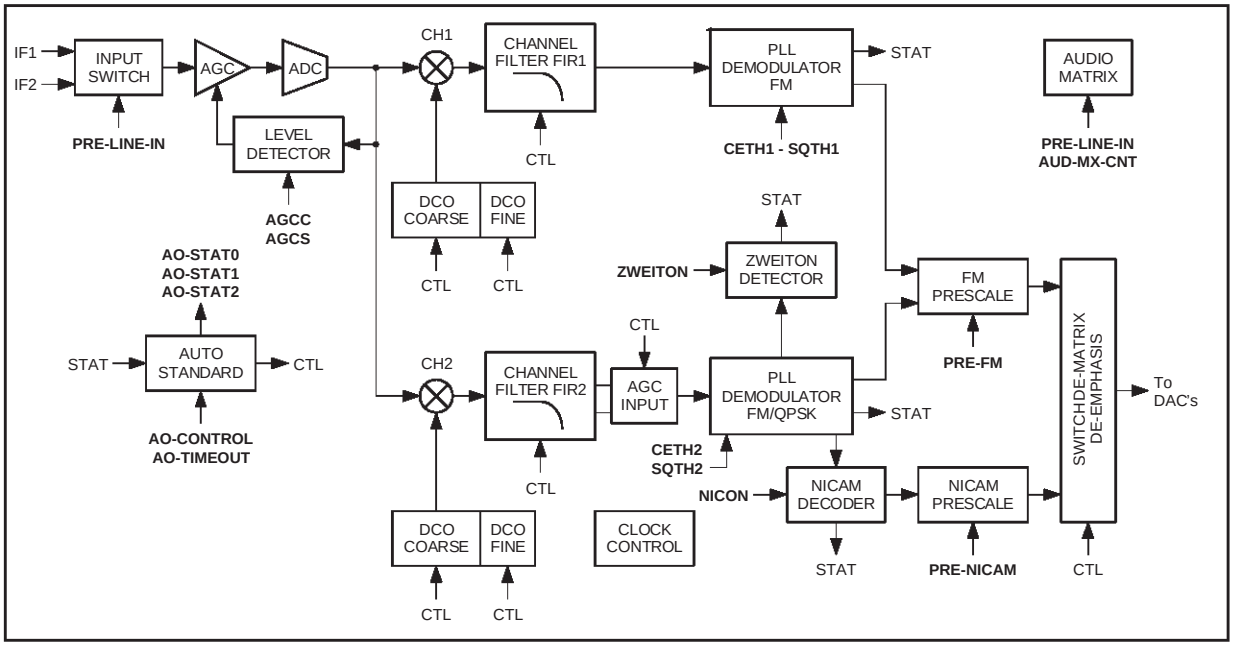
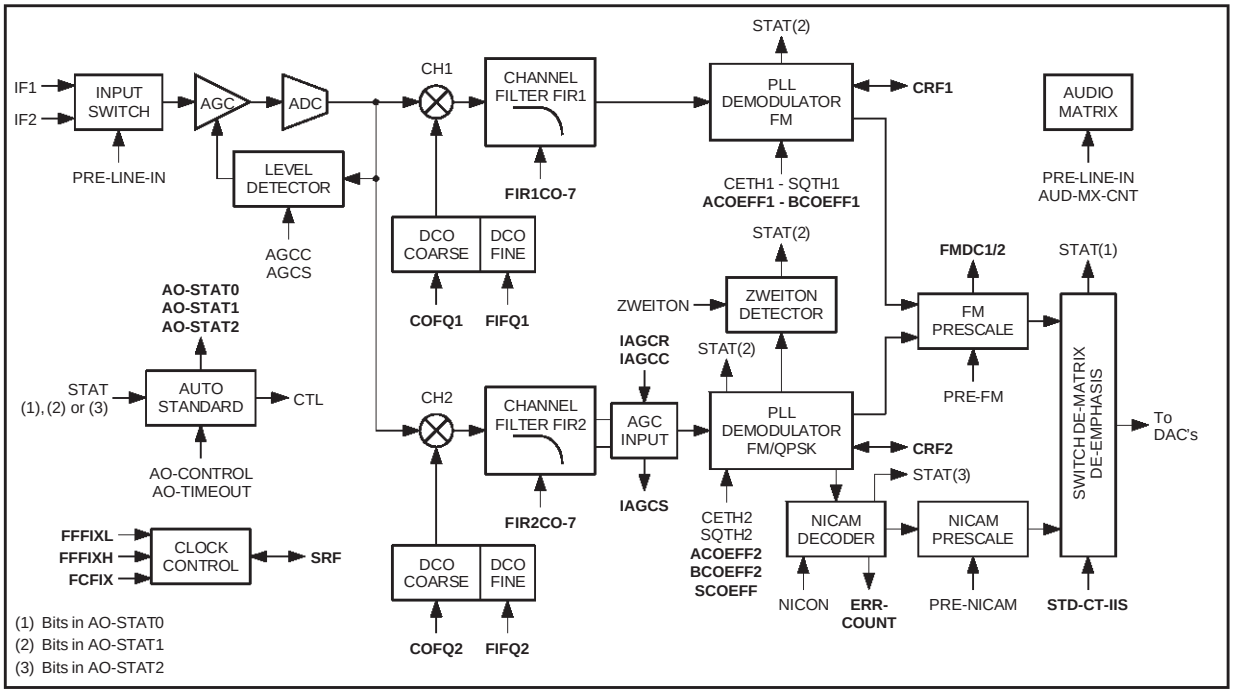


Figure 4 : Advanced Operation Mode

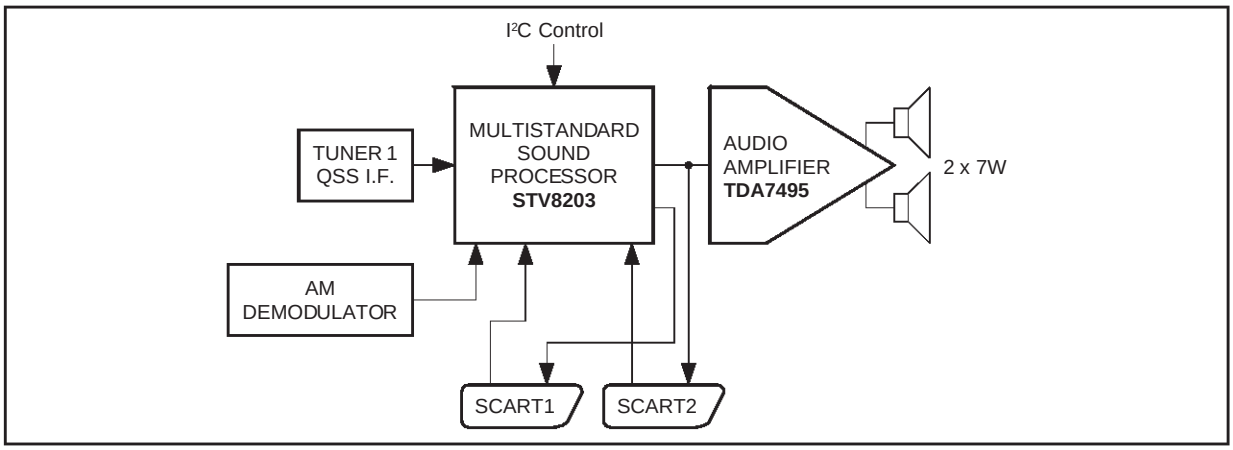


USING STV8203 (continued)

3 - Example of Applications

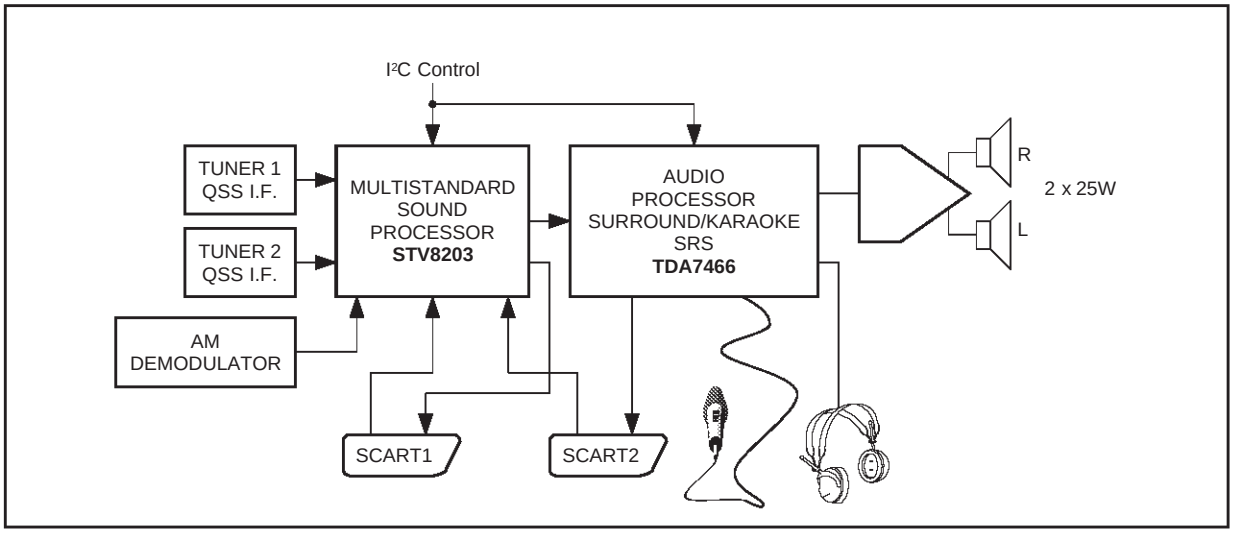
3.a - Very Low Cost TV Application

Figure 5



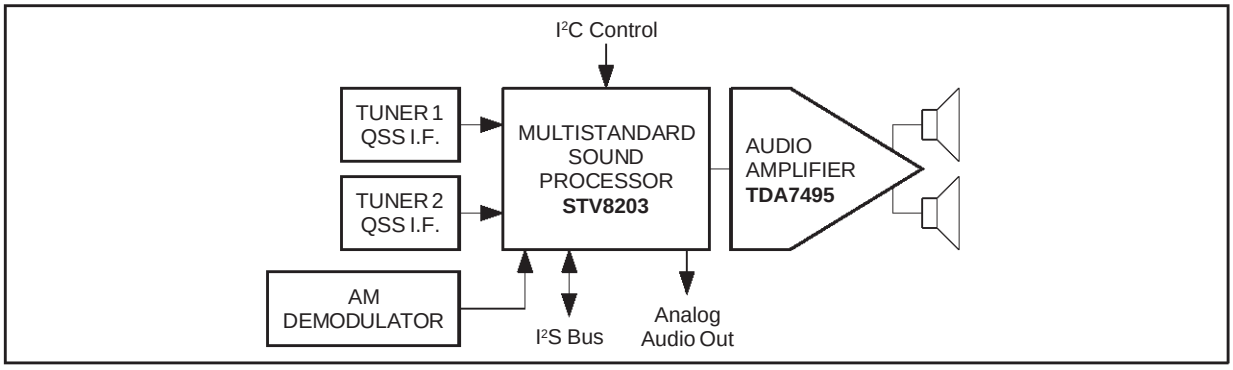
3.b - High-End TV Application

Figure 6



3.c - TV Application in PC

Figure 7



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
AV_{DD5}	Analog Supply Voltage	7	V
DV_{DD5}	Digital Supply Voltage	7	V
AV_{CC}	Scart Interface Supply Voltage	9.5	V
P_{tot}	Power Total Dissipation	0.8	W
T_{oper}	Operating Temperature	0, +70	^oC
T_{stg}	Storage Temperature	-20, +150	^oC

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THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-p)}$	Junction to Pins Thermal Resistance	Max. SDIP42 TQFP44	 55 68	 °C/W °C/W

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min.	Typ.	Max.	Unit
AV_{DD5}	Analog V_{DD}		4.75	5.0	5.25	V
DV_{DD5}	Digital V_{DD}		4.75	5.0	5.25	V
AV_{CC}	Audio Interface Supply	for $2V_{RMS}$ outputs for $1V_{RMS}$ outputs	7.6 4.75	8.0 5.0	8.4 5.25	V V

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ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
I_{AIN}	Input Current on AV_{CC}	AV_{CC} = 5V AV_{CC} = 8V		58 75		mA mA
I_{DIN}		DV_{DD5} = 5V		120		mA
IF INPUTS						
R_{IN}	Input Resistance			6		kΩ
C_{IN}	Input Capacitance			10		pF
SWISO	Switch Isolation	f = 10MHz		40		dB
SIF FR	Input Frequency Range	For FM demodulation	4		8	MHz
$V_{IN\ (Min.)}$ $V_{IN\ (Max.)}$	Minimum Input Level Maximum Input Level		25		 630	mV_{RMS} mV_{RMS}
AGC	AGC Range			28		dB

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ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
FM DEMODULATION PATH (see Figure 8)						
f_{RESP}	Frequency Response	20Hz - 15kHz	-1.0		+1.0	dB
SNR FM	Signal to Noise	100mV$_{RMS}$, unweighted 20Hz-15kHz, Output 2V$_{RMS}$ @ 1kHz	65			dB
THD FM	Total Harmonic Distortion	Output signal 1V$_{RMS}$ @ 1kHz, 50kHz FM deviation			0.2	%
SEP FM	German Stereo Channel Separation		40			dB
AMR	AM Rejection	SIF = 100mV$_{RMS}$ 30% modulation @ 1kHz		60		dB
V_{FMOUT}	Maximum Output Swing			2		V_{RMS}
NICAM DEMODULATION PATH (see Figure 8)						
SNR NIC	Signal to Noise	100mV$_{RMS}$, unweighted 20Hz-15kHz, Output 2V$_{RMS}$ @ 1kHz	72			dB
THD NIC	Total Harmonic Distortion	Output signal 1V$_{RMS}$ @ 1kHz			0.07	%
V_{NICOUT}	Maximum Output Swing			2		V_{RMS}
SEP NIC	Channel Separation		60			dB
AUDIO MATRIX (see Figure 9)						
RIN	Input Resistance			30		kΩ
V_{CL}	Input Clipping Level	AV_{CC} = 8V AV_{CC} = 5V	2 1			V_{RMS} V_{RMS}
GMAT		Prescaling = 0 V_{IN} = 1V$_{RMS}$, 15Hz to 15kHz	-0.5	0	0.5	dB
R_{OUT}	Output Resistance	All audio output except Mono output Mono output		200 400		Ω Ω
SNR	Signal to Noise Ratio	Preline in = 0, V_{OUT} = 2V$_{RMS}$, unweighted 20Hz-15kHz		90		dB
XLR	Audio L to R Channel Crosstalk	2V$_{RMS}$ @ 1kHz	60			dB
X12	Audio Crosstalk from Channel 1 to Channel 2		80			dB

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Figure 8 : Synoptic A

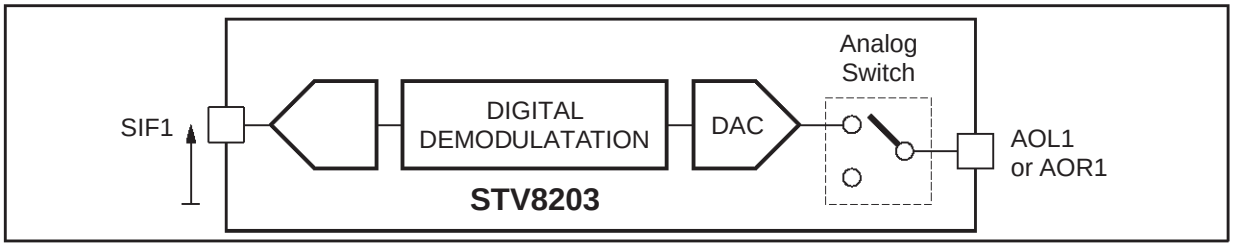

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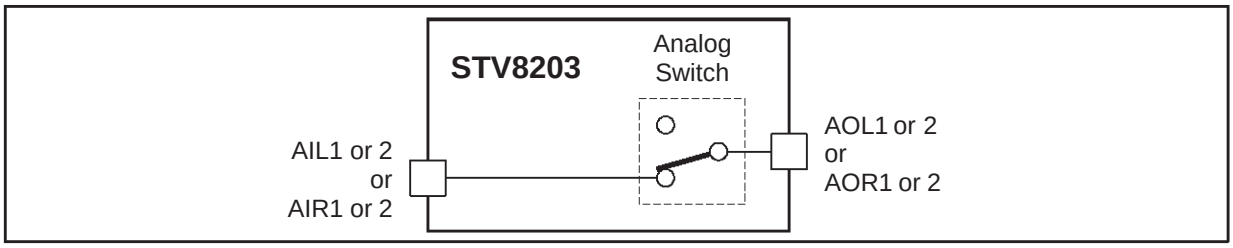
Figure 8 : Synoptic A



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PROGRAMMING THE DEVICE

1 - I²C Address and Protocol

Write

S	80	A	SUB-ADDRESS	A	DATA	A	DATA	A	P

Read

S	80	A	SUB-ADDRESS	A	P	S	81	A	DATA	A	DATA	N

S = Start, A = Acknowledge, P = Stop, N = No acknowledge.
Sub-address is the register address pointer ; this value auto-increments for both write and read.

2 - List of Registers

Registers not controlled by AUTOSTANDARD, except bits marked "*" which are controlled

Name	Addr. (Hex)	Reset (Bin)	Register Function /Description							
			bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SWD (Switch, Dematrix & De-emphasis)										
PRE-FM	2	0001 1101	0	0	0	Fm Prescale [4:0]				
PRE-NICAM	3	0001 1101	0	0	0	Nicam Prescale [4:0]				
STD-CT-IIS	4	0001 1000	0	0	gain	demoff	mute *	SWD [2:0] *		
FMDC1	5	read only	FM DC level 1							
FMDC2	6	read only	FM DC level 2							
AUDIO MATRIX										
PRE-LINE-IN	7	0000 1000	IF Switch	AGC Switch off	0	0	Line Inputs Gain [3:0]			
AUD-MX-CNT	8	0010 0010	mout1	S1 o/p select			mout0	S2 o/p select		
NICAM										
NICON	9	0000 0000	dif-pol	0	TSCTRL [1:0]		ECT	MAE	0	0
ERR-COUNT	A	read only	error [7:0]							
AUTOSTANDARD										
AO-STAT0	B	read only	std-det	sid1	sid0	aomute	am-mono	SWD [2:0] (monitor)		
AO-STAT1	C	read only	fm2-car	fm2-sq	fm1-car	fm1-sq	qpsk-lk	zw-det	zw-st	zw-dm
AO-STAT2	D	read only	nic-det	f-mute	LOA	Nicam CBI [4:1]				n-mute
AO-CONTROL	E	0001 1111	mute ov	mono ov	unmute	C4 ov	standard check [3:0]			
AO-TIMEOUT	F	1010 0101	Time 2 setting (1280ms)				Time 1 setting (160ms)			
ZWEITON										
ZWEITON	10	1000 1000	Thresh-Sig [3:0]				Thresh-ST [3:0]			
DEMODULATOR										
AGCC	11	0001 0001	agc-cmd*	0	0	agc-ref [2:0]			agc-cst[1:0]	
AGCS	12	0100 00xx	0	agc-err [4:0]					sig-ovr	sig-und
IAGCR	14	1000 1000	Iagc-ref [7:0]							
IAGCC	15	0000 0011	iagc-off*	0	0	0	0	Iagc-cst[2:0]		
IAGCS	16	read only	Iagc-Ctrl [7:0]							
FFFIXL	17	0000 0000	Clock Generator Fine Frequency (8 lsb's)							
FFFIXH	18	0110 1110	0	demod mode M2:M0*			clock gen fine freq (4 msb's)			
FCFIX	19	0001 0001	0	0	Clock Generator Coarse Frequency					
CRF2	20	0000 0000	Channel 2 Carrier Recovery Frequency							
CETH2	21	0011 0101	Channel 2 carrier-th [7:0]							
SQTH2	22	0011 1100	Channel 2 squelch-th [7:0]							
Range of Registers Controlled by AUTOSTANDARD Function (address 23 Hex to 3C Hex)										
CRF1	3D	0000 0000	Channel 1 Carrier Recovery Frequency							
CETH1	3E	0011 0101	Channel 1 carrier-th [7:0]							
SQTH1	3F	0011 1100	Channel 1 squelch-th [7:0]							

PROGRAMMING THE DEVICE (continued)

Registers controllable by AUTOSTANDARD

Name	Addr. (Hex)	Reset (Bin)	Register Function/Description							
			bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DEMODULATOR CHANNEL 2										
FIR2CO	23	0000 0000	FIR2 coefficient 0							
FIR2C1	24	0000 0000	FIR2 coefficient 1							
FIR2C2	25	0000 0000	FIR2 coefficient 2							
FIR2C3	26	0000 0000	FIR2 coefficient 3							
FIR2C4	27	1111 1111	FIR2 coefficient 4							
FIR2C5	28	0000 0100	FIR2 coefficient 5							
FIR2C6	29	0001 0100	FIR2 coefficient 6							
FIR2C7	2A	0010 0101	FIR2 coefficient 7							
COFQ2	2B	0000 1100	0	0	Channel 2 DCO Coarse Frequency					
FIFQ2	2C	1100 0100	Channel 2 DCO Fine Frequency (8lsb's)							
ACOEFF2	2D	1001 0000	dmd sw2	0	Coarse A2		Sign A2	Fine A2		
BCOEFF2	2E	1010 1100	sat sw2	0	dco2 gain			B2		
SCOEFF	2F	0001 1100	dmx-of	0	plf_A			plf_B		
SRF	30	0000 0000	Symbol Recovery Frequency							
DEMODULATOR CHANNEL 1										
FIR1CO	31	0000 0000	FIR1 coefficient 0							
FIR1C1	32	1111 1110	FIR1 coefficient 1							
FIR1C2	33	1111 1100	FIR1 coefficient 2							
FIR1C3	34	1111 1101	FIR1 coefficient 3							
FIR1C4	35	0000 0010	FIR1 coefficient 4							
FIR1C5	36	0000 1101	FIR1 coefficient 5							
FIR1C6	37	0001 1000	FIR1 coefficient 6							
FIR1C7	38	0001 1111	FIR1 coefficient 7							
COFQ1	39	0000 1011	0	0	Channel 1 DCO Coarse Frequency					
FIFQ1	3A	1100 0111	Channel 1 DCO Fine Frequency (8lsb's)							
ACOEFF1	3B	0010 0011	dmd sw1	0	Coarse A1		Sign A1	Fine A1		
BCOEFF1	3C	0001 0010	sat-sw1	0	dco1 gain			B1		

Note : This register must be kept to "0".

RESERVED	1	00000000	0	0	0	0	0	0	0	0

PROGRAMMING THE DEVICE (continued)

3 - Register Description

3.1 - Registers Not Controlled By Autostandard (except some mentioned bits)

PRE-FM *(Prescale FM Level)*

Address : 02
Type : R/W
Reset : 0001 1101

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	FM PRESCALE				

FM PRESCALE : 00000 0dB
01100 +12dB
10100 -12dB
(step size = 1dB, range = ±12dB in 2's complement)

Sets the reference level for an FM signal. Note, this is also dependant on the PLL programming. For example, with default settings for the PLL, an FM deviation of 27kHz will result in a signal 17dB below full scale before de-emphasis. At 1kHz, the internal de-emphasis gain is 14dB giving a level of -3dB. Full scale output from the DAC is $2V_{RMS}$ corresponding to 0dB. and so for $1V_{RMS}$, PRE-FM should be set to -3dB.

PRE-NICAM *(Prescale NICAM Level)*

Address : 03
Type : R/W
Reset : 0001 1101

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	NICAM PRESCALE				

NICAM PRESCALE : 00000 0dB
01100 +12dB
10100 -12dB
(step size = 1dB, range = ±12dB in 2's complement)

Sets the reference level for a NICAM signal. For example, a full scale NICAM signal at 1kHz would be received at -12dB before de-emphasis. Internal de-emphasis gain at this frequency is 9dB so for $1V_{RMS}$, pre-nicam should be set to -3dB.

PROGRAMMING THE DEVICE (continued)

STD-CT-IIS *(SWD Control)*

Address : 04
Type : R/W
Reset : 0001 1000

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	GAIN	DEMOFF	MUTE	SWD		

GAIN : which should normally be set to its default value, can be used to change the dematrix gain for CH1 = L+R.
dematrix gain : 0 : channel 1 = L/2+R/2, 1 : channel 1 = L+R

DEMOFF : bypasses the FM or Nicam de-emphasis : 1 = de-emphasis off

MUTE : mutes the DAC (FM or Nicam) : 1 = DAC muted
(only effective if the AUTOSTANDARD function is off)

SWD : Bits allow control of the mode of the switch/dematrix function as shown below.
(only effective if the AUTOSTANDARD function is off)

[2:0]	De-emphasis	Description	NICON[1:0]	Left	Right
000	50µs	FM CH1 mono	X	D1	D1
001		Zweiton mono	X	D1	D1
010		Zweiton dual mono	00	D1	D2
			01	D2	D2
			10	D1	D1
			11	D2	D1
011		Zweiton stereo	X	DSL	DSR
100	not used				
101	J17	Nicam mono	X	N1	N1
110		Nicam dual mono	00	N1	N2
			01	N2	N2
			10	N1	N1
			11	N2	N1
111		Nicam stereo	X	NSL	NSR

D1 = FM audio from CH1, D2 = FM audio from CH2, DS = dematrixed Zweiton stereo.
N1 = Nicam M1, N2 = Nicam M2, NS = Nicam stereo.
These bits are controlled by AUTOSTANDARD when this function is activated.

FMDC1, FMDC2 *(FM DC Level)*

Address : 05-06
Type : R

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FM DC LEVEL 1 OR FM DC LEVEL 2							

FM Frequency offset (dependent on the PLL coefficients).
This value (2's complement) is proportional to the DC offset, measured below 20Hz, of an FM signal. It could be used to implement an AFC for FM signals.

PROGRAMMING THE DEVICE (continued)

PRE-LINE-IN *(IF Input Selection and Audio Matrix Gain Control)*

Address : 07
Type : R/W
Reset : 0000 1000

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IF SWITCH	AGC SWITCH OFF	0	0	LINE INPUTS GAIN			

IF SWITCH : IF Input Switch
controls the IF input selection (0 = IF1).

AGC SWITCH OFF : can be used to switch-off the AGC amplifier..

LINE INPUTS GAIN : allow the levels of the analog line inputs (SCART1, SCART2 and MONO) to be adjusted simultaneously.
1000 0dB (default setting)
0010 -6dB
1110 +6dB
(step size = 1dB, range = ±6dB)

AUD-MX-CNT *(Audio Matrix Control)*

Address : 08
Type : R/W
Reset : 0010 0010

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
MOUT1	S1 O/P SELECT			MOUT0	S2 O/P SELECT		

These 8 bits are used to control the audio matrix configuration (see Figure 1).

Data bits								Actual Function Selected
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	Reset : AO1 and AO2 = DAC and MOUT = (L1+R1)/2
X	X	X	X	X	0	0	0	AO2 = Muted
X	X	X	X	X	0	0	1	AO2 = Muted
X	X	X	X	X	0	1	0	AO2 = AO1 (reset state)
X	X	X	X	X	0	1	1	AO2 = LI1 (Scart 1 input)
X	X	X	X	X	1	0	0	AO2 = Muted
X	X	X	X	X	1	0	1	AO2 = Muted
X	X	X	X	X	1	1	0	AO2 = Muted
X	X	X	X	X	1	1	1	AO2 = Muted
X	0	0	0	X	X	X	X	AO1 = Muted
X	0	0	1	X	X	X	X	AO1 = MIN
X	0	1	0	X	X	X	X	AO1 = DAC (reset state)
X	0	1	1	X	X	X	X	AO1 = Muted
X	1	0	0	X	X	X	X	AO1 = LI2 (Scart 2 input)
X	1	0	1	X	X	X	X	AO1 = Muted
X	1	1	0	X	X	X	X	AO1 = Muted
X	1	1	1	X	X	X	X	AO1 = Muted
0	X	X	X	0	X	X	X	MOUT = (L1+R1)/2 (reset state)
0	X	X	X	1	X	X	X	MOUT = R1
1	X	X	X	0	X	X	X	MOUT = L1
1	X	X	X	1	X	X	X	Not used

PROGRAMMING THE DEVICE (continued)

NICON *(NICAM Control)*

Address : 09
Type : R/W
Reset : 0000 0000

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIF-POL	0	TSCTRL		ECT	MAE	0	0

DIF-POL : controls the polarity of the Q channel in the DQPSK decoder. Its default value is correct for Nicam B/G/L and so does not need to be changed.

TSCTRL : These two bits are programmed to chose the decision mode for the zweiton detector as following :
00 : 2 decisions with 1024 samples accumulation
01 : 3 decisions with 1024 samples accumulation
10 : 2 decisions with 2048 samples accumulation
11 : 3 decisions with 2048 samples accumulation

ECT : bit error rate counting time : 0 = 128ms, 1 = 64ms

MAE : max allowed errors : 0 = 511, 1 = 255
Bits 2 and 3 adjust the bit error rate (approximate) at which the Nicam decoder mutes; a fixed hysteresis is provided so that the decoder will unmute only when the BER has dropped to one quarter of that for muting :

ECT	MAE	BER Muting Threshold
0	0	1 in 112
0	1	1 in 224
1	0	1 in 56
1	1	1 in 112

ERR-COUNT *(Nicam Error Counter)*

Address : 0A
Type : R

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ERROR							

Error Signals Count (averaged over time ECT above)

The value in this register, updated every 64ms or 128ms, gives an indication of the Nicam bit error rate. It can therefore be used to mute the decoder at an error rate below 1 in 56 (=FF if ECT= 64ms).

PROGRAMMING THE DEVICE (continued)

AO-STAT0 *(AUTOSTANDARD Status 0)*

Address : 0B
Type : R

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
STD-DET	SID1	SID0	AOMUTE	AM-MONO	SWD (MONITOR)		

STD-DET : Standard Detection :
0 = no standard detected
1 = indicates that an expected standard has been identified.

SID [1:0] : Standard Identification of the demodulator input
indicate the standard which has been identified :

SID[1:0]	Standard
00	I FM/NICAM
01	B/G FM - Zweiton
10	B/G FM/NICAM
11	L/L' AM/NICAM

AOMUTE : Audio Output Mute
indicates that the audio outputs are muted (=1); only when the demodulator is selected as audio source. This would be the case during standard search or no signal found.

AM-MONO : AM selected
indicates if the AM input (MIN) has been selected (=1); normally used for system L.

SWD : Switch Dematrix Mode
indicate the setting of the SWD block :

SWD[2:0]	Mode description	De-emphasis
000	FM CH1 mono	50µs
001	Zweiton mono (CH1)	
010	Zweiton dual mono	
011	Zweiton stereo	
100	Unused	Unused
101	NICAM mono	J-17
110	NICAM dual mono	
111	NICAM stereo	

AO-STAT1 *(AUTOSTANDARD Status 1 ; demodulator signal detectors)*

Address : 0C
Type : R

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FM2-CAR	FM2-SQ	FM1-CAR	FM1-SQ	QPSK-LK	ZW-DET	ZW-ST	ZW-DM

FM2-CAR : FM2 Carrier Detector Lock
FM2-SQ : FM2 Squelch Detector Lock
FM1-CAR : FM1 Carrier Detector Lock
FM1-SQ : FM1 Squelch Detector Lock
QPSK-LK : QPSK Lock
ZW-DET : Zweiton Pilot Lock
ZW-ST : Zweiton Stereo Lock
ZW-DM : Zweiton Dual Mono Lock

This register allows direct access to the demodulator signal detectors ; 1 = detected.

PROGRAMMING THE DEVICE (continued)

AO-STAT2 *(AUTOSTANDARD Status 2 ; NICAM)*

Address : 0D
Type : R

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
NIC-DET	F-MUTE	LOA	NICAM CBI				N-MUTE

NIC-DET : NICAM detected
indicates a valid NICAM signal found (1 = detected).

F-MUTE : Frame Mute
indicates the NICAM decoder is muted because the superframe alignment has been lost.

LOA : Loss of frame Alignment word
indicates loss of alignment to the frame alignment word in the NICAM decoder; the bit error rate is too high or no signal is present.

NICAM CBI : indicates the received NICAM control bits with the following interpretation :

CBI[4:1]	Nicam Signal Description
X000	Stereo
X001	ch1 = mono, ch2 = data
X010	Dual Mono
X011	704Kbit/s data
X1XX	FM selected during additional coding options
0XXX	Nicam different to FM mono
1XXX	Nicam mono(M1) or stereo = FM mono

N-MUTE : NICAM Mute
indicates that the NICAM decoder is muted (it may be unmuted by AO-CONTROL bit 5).

PROGRAMMING THE DEVICE (continued)

AO-CONTROL *(AUTOSTANDARD Control)*

Address : 0E
Type : R/W
Reset : 0001 1111

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
MUTE OV	MONO OV	UNMUTE	C4 OV	STANDARD CHECK			

AUTOSTANDARD controls the audio matrix when the user has selected the DAC as source (AUD-MX-CNT bits[6:4] = 010). In this case it will mute the outputs or select MIN. These functions can be overriden by bits 6 and 7 below.

MUTE OV : Mute override, 1 = mute (override AUTOSTANDARD) forces the audio signal to be muted.

MONO OV : FM/AM Mono override, 1 = mono (override AUTOSTANDARD) forces can be used to force to analogue sound. This may be useful in the case of marginal NICAM reception to prevent automatic switching.

AUD-MX-CNT bits[6:4]	bit 7	bit 6	AO1 source
010	0	0	DAC
	X	1	MIN (in case of L/L' standard)
	0	1	FM (in case of B/G or I standard)
	1	1	Muted (in case of B/G or I standard)
	1	0	Muted

UNMUTE : Nicam Un-mute, 1 = unmute allows the NICAM decoder to be unmuted if the bit error rate is higher than the preset limit; this overrides the automatic switching to FM or AM which would normally occur.

C4 OV : CBI4 override, 1 => CBI[4] forced to 1 internally is used to override the 4th NICAM control bit (reserve sound switch) if required. This bit is transmitted by the broadcaster to indicate that the analogue sound carrier is a backup of the NICAM signal; this is usually the case. If the NICAM signal fails, the STV8203 will automatically switch to backup sound if the received bit was set to 1. If this bit was set to 0 and bit 4 set to 0, the decoder will stay switched to analogue sound. If bit 4 is set to 1, the received CBI4 is ignored. Note that if automatic standard is off, switching between analogue and NICAM audio must be done manually.

STANDARD CHECK : Control the choice of transmission standards to be searched for by the automatic standard function (standard search active when bit = 1). The more choices, the longer the search time. If the system in use can be identified by the characteristics of the video signal, for example by the chroma demodulator, then only a single bit needs to be set. In this case, the AUTOSTANDARD function will program the demodulator for the chosen standard. **If no bits are set, the AUTOSTANDARD function is disabled** and all registers need to be set manually.
bit 3 - Run check for standard 3 (L/L' - AM/NICAM)
bit 2 - Run Check for Standard 2 (B/G - FM/NICAM)
bit 1 - Run check for standard 1 (B/G - Stereo)
bit 0 - Run check for standard 0 (I - FM/NICAM)

AO-TIMEOUT *(AUTOSTANDARD Timer Adjustment)*

Address : 0F
Type : R/W
Reset : 1010 0101

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
TIME 2 SETTING				TIME 1 SETTING			

Time 1 is used for NICAM and FM mono validation and time 2 for Zweiton. If the standard is not found within this time limit, the next standard will be tried. Time 1 = decimal [bit 3:0] x 32ms. Time 2 = decimal [bit 7:4] x 128ms. Time 1 default value is 160ms. Time 2 default value is 1280ms.
A time of 0ms should not be programmed.

PROGRAMMING THE DEVICE (continued)

ZWEITON *(Pilot Carrier and Tone Detector Thresholds)*

Address : 10
Type : R/W
Reset : 1000 1000

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
THRESH-SIG				THRESH-ST			

THRESH-SIG : Pilot Carrier Level Threshold
Set the sensitivity for the pilot carrier detector.

THRESH-ST : Detected Tone Level Threshold
Set the detection threshold level for stereo and dual mono (bi-lingual) tones.

Power on default values give a detection threshold corresponding to a modulated pilot carrier S/N of 0dB (700Hz BW) and a S/N of 40dB for the recovered audio.

AGCC *(AGC Control for ADC)*

Address : 11
Type : R/W
Reset : 0001 0001

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
AGC-CMD	0	0	AGC-REF			AGC-CST	

AGC-CMD : 1 = manual/forced mode, 0 = automatic mode
Normally set to 0 enabling automatic mode. In the case of system L/L', due to the presence of the AM sound carrier, the AGC should be switched off. In this case, a fixed gain value should be set using the AGCS register (see below).
This bit is controlled by AUTOSTANDARD when this function is activated.

AGC-REF : Defines the clipping level.
Adjust the allowable proportion of samples at the input of the ADC which will be clipped; the AGC tries to maximise the use of the full scale range of the ADC. The default setting gives a ratio of 1/256.

AGC-REF [4:2]	Clipping Ratio
000	1/16 (single carrier)
001	1/32
010	1/64
011	1/128
100	1/256
101	1/512
110	1/1024
111	1/2048 (multiple carriers)

AGC-CST : AGC time constant between each step of 1.25dB.
For a 27MHz XTAL => 00 = 1.21ms, 01 = 2.43ms, 10 = 4.85ms, 11 = 9.7ms.
The adjustment is a compromise between settling time and noise immunity.

PROGRAMMING THE DEVICE (continued)

AGCS *(AGC Control and Status for ADC)*

Address : 12
Type : R/W
Reset : 0100 00XX

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	AGC-ERR					SIG-OVR	SIG-UND

AGC-ERR : Gain Control Signal of amplifier before ADC. There are 32 steps of 1.25dB.

AGC-ERR [6:2]	Gain (dB)
00000	0
00001	1.25
.....	.....
11110	37.50
11111	38.75

When AGC_CMD = 0, AGC-ERR can be read thus indicating the input level. It can also be written to thus presetting the AGC level which will then adjust itself to the final value. When AGC_CMD = 1, the AGC is off and thus writing to AGC-ERR directly controls the AGC amplifier gain. Reading AGC_ERR just confirms the fixed value.

SIG-OVR : 1 = agc overloaded - signal too BIG
SIG-UND 1 = agc under loaded - signal too SMALL
When the AGC is in automatic mode (agc_cmd=0), bit 0 indicates if the input signal is too small and bit 1 if the AGC is too big. These bits could be used when setting the input level to the STV8203.

IAGCR *(Internal AGC Reference for QPSK)*

Address : 14
Type : R/W
Reset : 1000 1000

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IAGC-REF							

Sets the mean value of the internal AGC, used for QPSK demodulation. The default setting corresponds to half full scale amplitude at the PLL input.

IAGCC *(Internal AGC Time Constant for QPSK)*

Address : 15
Type : R/W
Reset : 0000 0011

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IAGC-OFF	0	0	0	0	IAGC-CST		

IAGC-OFF : 1 = Internal agc = off
Only enabled when AUTOSTANDARD is off. Normally , the internal AGC should be OFF for FM and ON for QPSK.
This bit is controlled by AUTOSTANDARD when this function is activated.

IAGC-CST : Internal AGC Programmable Step Constant.
Set the internal AGC time constant; the compromise is between fast settling time (for the quickest Nicam identification) and noise immunity. The control range is about 45dB divided into 0.2dB steps. These bits control the time per step (values given for QPSK mode) :

AGC-CST [2:0]	Step time (µs)	Time Response (ms)
000	703	105
001	352	53
.....	.....	.....
111	5.5	0.82

PROGRAMMING THE DEVICE (continued)

IAGCS *(Internal AGC Control Value)*

Address : 16
Type : R

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IAGC-CTRL							

Indicates the value of the internal AGC control signal.
Normally, the mean value should equal the value set in the IAGCR register when a signal is being demodulated.

FFFIXL *(Clock Generator Fine frequency)*

Address : 17
Type : R/W
Reset : 0000 0000

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLOCK GENERATOR FINE FREQUENCY (8 LSB's)							

See FCFIX register for explanation.

FFFIXH *(Clock Generator and Fine Frequency Control)*

Address : 18
Type : R/W
Reset : 0110 1110

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	DEMOD MODE M2:M0			CLOCK GEN FINE FREQ (4 MSB's)			

DEMOD MODE M2:M0 : Controls the demodulator mode (only when register Ehex bits[3:0] = 0000) :

MODE[6:4]	CH1 FM	CH2 FM/QPSK
X00	Normal	FM Normal
X01	Wide	FM Wide
010	Normal	QPSK System B/G/L
011	Wide	QPSK System B/G/L
110	Normal	QPSK System I
111	Wide	QPSK System I

The FM discriminator modulation full range can be set at :
- narrow mode : 250kHz (± 125kHz),
- wide mode : 500kHz (± 250kHz).

CLOCK GEN FINE FREQ : Clock generator fine frequency (4 MSB's) (see FCFIX for explanation).

FCFIX *(Clock Generator Coarse Frequency)*

Address : 19
Type : R/W
Reset : 0001 0001

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	CLOCK GENERATOR COARSE FREQUENCY					

The bits [5:0] together with FFFIXH bits [3:0] and FFFIXL bits [7:0] can be used to programme the internal clock generator for different quartz crystal frequencies ; the default value is for 27MHz.

$P = 182 \cdot \frac{Fref}{Fqpsk} - 193$ with Fref = crystal frequency, Fqpsk = 32 x 728kHz = 23.296MHz.

FCFIX = INT(P) (INT: integer part)
FFFIX = 256 x (16 x REM(P) - 1) (REM: fractional remainder)

Note that 0 ≤ FFFIX <3840 so there is a small range of frequencies which cannot be used.
Example : Fref = 27MHz, FCFIX = 17, FFFIX = 3584.

PROGRAMMING THE DEVICE (continued)

CRF2 - CRF1 *(FM/QPSK PLL Demodulator Offset)*

Address : 20-3D
Type : R/W
Reset : 0000 0000

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CHANNEL 2 or CHANNEL 1 CARRIER RECOVERY FREQUENCY							

This register provides access to the instantaneous frequency of the PLL (2's complement). If written to, it will preset the DCO frequency; if read it provides the instantaneous frequency offset of the PLL's and could be used for an AFC function.

CETH2 - CETH1 *(FM Carrier Level Threshold)*

Address : 21-3E
Type : R/W
Reset : 0011 0101

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CHANNEL 2 or CHANNEL 1 CARRIER-THRESHOLD							

These registers, which perform the same function in channel 1 and channel 2, compare the carrier level in the channel against the threshold value. This level is measured after the channel filter and is relative to the full scale reference level (0dB).

This is used as part of the validation of an FM signal, if the carrier level is below the threshold, the signal is considered to be non-valid.

CETH	Threshold (dB)
255	-6
128	-12
64	-18
32	-24
....	....
0	OFF

If CETH is OFF, any carrier level will be accepted.
The reset value is 53, it means a threshold of -20dB.

SQTH2- SQTH1 *(FM Squelch Threshold)*

Address : 22-3F
Type : R/W
Reset : 0011 1100

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CHANNEL 2 or CHANNEL 1 SQUELCH-THRESHOLD							

The squelch detector measures the level of high frequency noise (>40kHz) and compares it to the threshold SQTH. If the level is below this value, the S/N of the FM signal is considered to be acceptable.

Values are given for FM with ±50kHz deviation :

SQTH	S/N (dB)
250	0
119	10
60	15
35	20
22	25

The reset value is 60, it means a SNR of 15dB.

PROGRAMMING THE DEVICE (continued)

3.2 - Registers Controllable by Autostandard

FIR2C - FIR1C *(FIR Coefficients)*

Address : 23-24-25-26-27-28-29-2A & 31-32-33-34-35-36-37-38
Type : R/W

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FIR2 or FIR1 COEFFICIENT 0							
FIR2 or FIR1 COEFFICIENT 1							
FIR2 or FIR1 COEFFICIENT 2							
FIR2 or FIR1 COEFFICIENT 3							
FIR2 or FIR1 COEFFICIENT 4							
FIR2 or FIR1 COEFFICIENT 5							
FIR2 or FIR1 COEFFICIENT 6							
FIR2 or FIR1 COEFFICIENT 7							

Each demodulator channel implements a 16 tap symetric FIR filter, each with 8 coefficients. The following table gives the default values provided by the AUTOSTANDARD function (ΔF = 50kHz in FM mode).

Tap Number	System I FM/NICAM		System B/G Zweiton		System B/G FM/NICAM		System L/L' AM/NICAM	
	CH1	CH2	CH1	CH2	CH1	CH2	CH1	CH2
0	0	0	0	0	0	0	0	0
1	-2	0	-2	-2	-2	0	-2	0
2	-4	0	-4	-4	-4	-1	-4	-1
3	-3	0	-3	-3	-3	3	-3	3
4	2	-1	2	2	2	0	2	0
5	13	4	13	13	13	-12	13	-12
6	24	20	24	24	24	10	24	10
7	31	37	31	31	31	61	31	61

COFQ2 - COFQ1 *(DCO Coarse Frequency)*

Address : 2B-39
Type : R/W
Reset : 0000 1100 for COFQ2 - 0000 1011 for COFQ1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	CHANNEL 2 or CHANEL 1 DCO COARSE FREQUENCY					

See FIFQ1/2 below for explanation.

PROGRAMMING THE DEVICE (continued)

FIFQ2 - FIFQ1 *(DCO Fine Frequency)*

Address : 2C-3A
Type : R/W
Reset : 1100 0100 for FIFQ2 - 1100 0111 for FIFQ1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CHANNEL 2 or CHANNEL 1 DCO FINE FREQUENCY (8LSB's)							

The DCO's, which are set to the carrier frequency to be demodulated, are adjusted in two parts as follows :

$C = \frac{Fc}{Fs} \cdot 48$, where Fc is the carrier frequency, Fs is the crystal frequency

Take the nearest integer, Ci, for the 6 bits of the COFQ register

$F = (C - Ci) \cdot \left(\frac{2^9}{3}\right)$

Take the nearest integer, Fi, for the 8 bits of the FIFQ register.
Common frequencies with Fs = 27MHz :

Fc (MHz)	Ci		Fi	
	decimal	binary	decimal	binary
5.5	10	001010	-38	11011010
5.74	10	001010	35	00100011
5.85	10	001010	68	01000100
6.0	11	001011	-57	11000111
6.552	12	001100	-60	11000100

ACOEFF2 - ACOEFF1 *(PLL Loop Filter Proportional Coefficient)*

Address : 2D-3B
Type : R/W
Reset : 10010000 for ACOEFF2 - 0010 0011 for ACOEFF1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DMD SW2 or 1	0	COARSE A2 or A1		SIGN A2 or A1	FINE A2 or A1		

DMD SW : Mode switch : 0 = FM, 1 = QPSK

COARSE A, SIGNA, FINE A : Program the PLL (FM/QPSK carrier recovery) loop filter proportional coefficient A :
A coefficient = coarse + (sign x fine)

COARSE	Value
00	0
01	1
10	1/2
11	1/4

SIGN	
0	+
1	-

FINE	Value
000	0
001	1/2
010	1/4
011	1/8
100	1/16
101	1/32
110	1/64
111	Not used

PROGRAMMING THE DEVICE (continued)

BCOEFF2 - BCOEFF1 *(PLL Loop Filter Integral Coefficient and DCO Gain)*

Address : 2E-3C
Type : R/W
Reset : 1010 1100 for BCOEFF2 - 0001 0010 for BCOEFF1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SAT SW2 or 1	0	DCO 2 or 1 GAIN			B2 or B1		

SAT SW : Saturation Switch : 0 = FM, 1 = QPSK

DCO GAIN : Programme the gain coefficient (K0) :

DCO [5:3]	Value
000	0
001	1
010	1/2
011	1/4
100	1/8
101	1/16
110	1/32
111	Not used

B : Programme the PLL (FM/QPSK carrier recovery) loop filter integral coefficient B :

B [2:0]	Value
000	0
001	1/4
010	1/8
011	1/16
100	1/32
101	1/64
11X	Not used

PROGRAMMING THE DEVICE (continued)

SCOEFF *(Symbol Tracking Loop Filter Coefficients)*

Address : 2F
Type : R/W
Reset : 0001 1100

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DMX-OF	0	PLF_A			PLF_B		

DMX-OF : Symbol tracking control : 0 = QPSK, 1 = FM.
In QPSK mode, the symbol tracking loop is closed.

PLF_A : A coefficient (proportional)
Programme the symbol tracking loop filter proportional coefficient A :

PLF_A [5:3]	Value
000	0
001	1
010	2
011	4
100	8
101	16
110	32
111	Not used

PLF_B : B coefficient (integral)
Program the symbol tracking loop filter integral coefficient B :

PLF_B [2:0]	Value
000	0
001	1/16
010	1/32
011	1/64
100	1/128
101	1/256
110	1/512
111	1/1024

SRF *(Symbol Tracking Loop Frequency)*

Address : 30
Type : R/W
Reset : 0000 0000

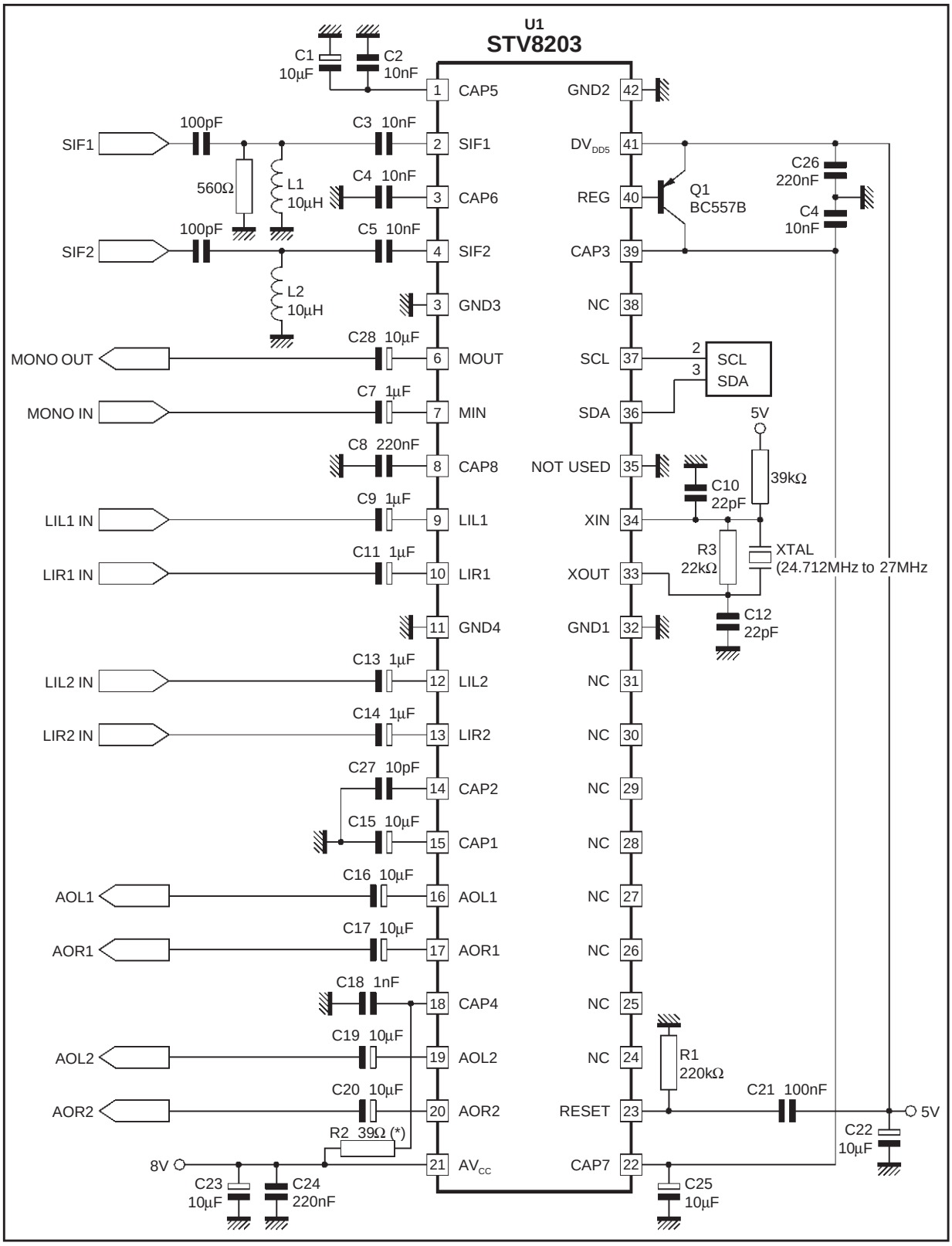
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SYMBOL RECOVERY FREQUENCY							

This register provides access to the control signal for the symbol tracking loop (2's complement). If read, it indicates a value proportional to the symbol tracking frequency error. If written to, it will preset the frequency error.

SRF [7:0]	Approx. Error (kHz)
10000000	-8
00000000	0
01111111	+8

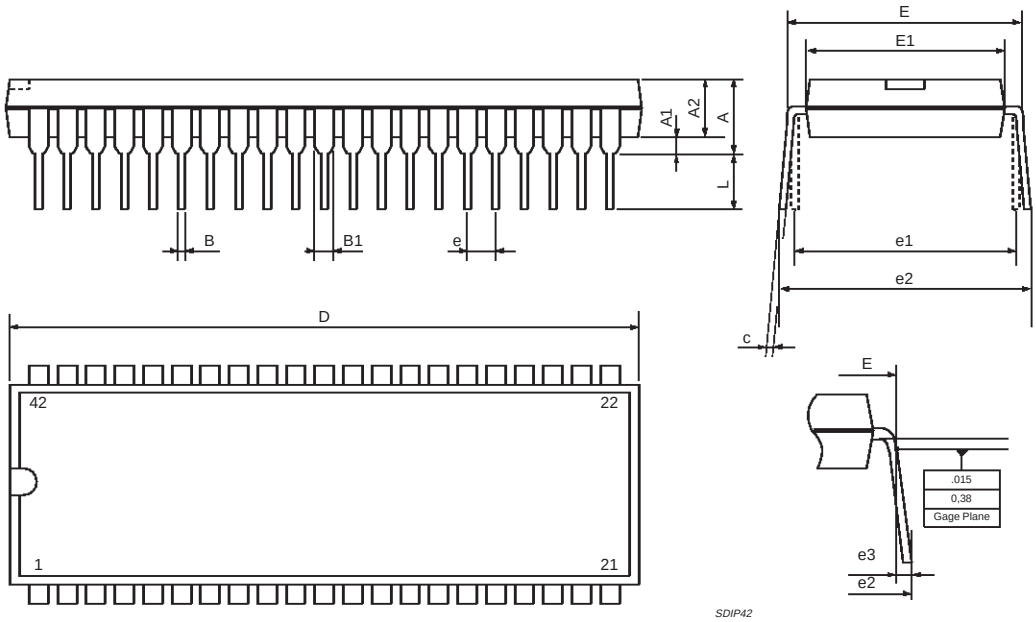
RESET
After a reset sequence, all the registers controllable by AUTOSTANDARD function (FIR, COFQ, FIFQ, ACOEFF, BCOEFF, SCOEFF, SRF) are adjusted for the standard I configuration (channel 1 to FM mono mode and channel 2 to QPSK mode).

APPLICATION DIAGRAM (SDIP42 PACKAGE)



(*) Note : Resistor R2 should be short-circuited in case of 5V only supply voltage application.

PACKAGE MECHANICAL DATA
42 PINS - PLASTIC SHRINK DIP



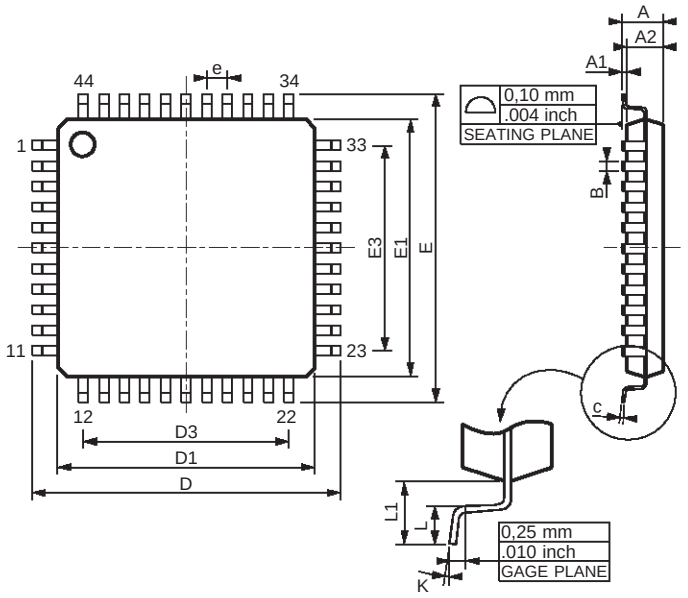
PMSDIP42.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.200
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.120	0.150	0.180
B	0.36	0.46	0.56	0.0142	0.0181	0.0220
B1	0.76	1.02	1.14	0.030	0.040	0.045
c	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	37.85	38.10	38.35	1.490	1.5	1.510
E	15.24		16.00	0.60		0.629
E1	12.70	13.72	14.48	0.50	0.540	0.570
e		1.778			0.070	
e1		15.24			0.60	
e2			18.54			0.730
e3			1.52			0.060
L	2.54	3.30	3.56	0.10	0.130	0.140

SDIP42.TBL

PACKAGE MECHANICAL DATA

44 PINS - FULL PLASTIC QUAD FLAT PACK (TQFP) (THIN)



PM-4Y.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.40	0.012	0.015	0.016
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0° (Min.), 7° (Max.)					

4Y.TBL