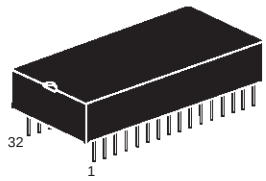
M48Z512A
M48Z512AY, M48Z512AV*

4 Mbit (512 Kbit x 8) ZEROPOWER® SRAM

FEATURES SUMMARY

- INTEGRATED, ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT, and BATTERY
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS OF DATA RETENTION IN THE ABSENCE OF POWER
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- TWO WRITE PROTECT VOLTAGES: (V_{PFD} = Power-fail Deselect Voltage)
  - M48Z512A: V_{CC} = 4.75 to 5.5V
    $4.5V \leq V_{PFD} \leq 4.75V$
  - M48Z512AY: V_{CC} = 4.5 to 5.5V
    $4.2V \leq V_{PFD} \leq 4.5V$
  - M48Z512AV: V_{CC} = 3.0 to 3.6V
    $2.8V \leq V_{PFD} \leq 3.0V$
- BATTERY INTERNALLY ISOLATED UNTIL POWER IS APPLIED
- PIN and FUNCTION COMPATIBLE WITH JEDEC STANDARD 512K x 8 SRAMs
- SURFACE-MOUNT CHIP SET PACKAGING (Figure 2) INCLUDES A 28-PIN SOIC and A 32-LEAD TSOP (SNAPHAT® Top to be ordered separately)
- SOIC PACKAGE PROVIDES DIRECT CONNECTION FOR A SNAPHAT TOP WHICH CONTAINS THE BATTERY
- SNAPHAT HOUSING (BATTERY) IS REPLACEABLE

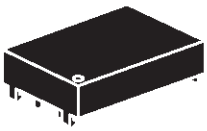
Figure 1. 32-pin PMDIP Module

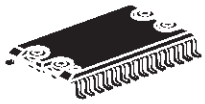


PMDIP32 (PM)
Module

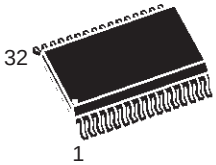
Figure 2. Surface-Mount (SMT) Solution

SNAPHAT (SH)
Crystal / Battery





SOH28 (MH)



TSOP II 32 (NC)
(10 x 20mm)

* Contact Local Sales Office

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DESCRIPTION

The M48Z512A/Y/V ZEROPOWER® RAM is a non-volatile, 4,194,304-bit Static RAM organized as 524,288 words by 8 bits. The device combines an internal lithium battery, a CMOS SRAM and a control circuit in a plastic, 32-pin DIP Module.

For surface-mount environments ST provides a Chip Set solution consisting of a 28-pin, 330mil SOIC NVRAM SUPERVISOR (M40Z300/W) and a 32-pin TSOP Type II (10 x 20mm) LPSRAM (M68Z512/W) packages. Both 5V and 3V versions are available (see Table 2, page 5).

The unique design allows the SNAPHAT® battery package to be mounted on top of the SOIC package after the completion of the surface-mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SNAPHAT battery package is shipped separately in plastic anti-static tubes or in Tape & Reel form. The part number is “M4Z32-BR00SH1.”

Figure 3. Logic Diagram

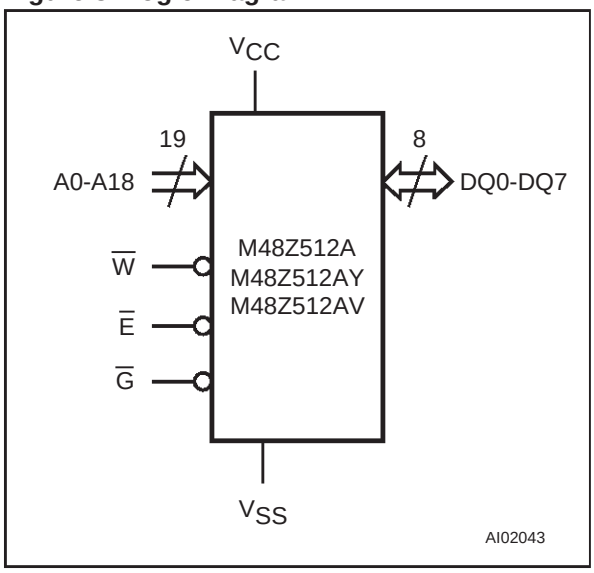


Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable Input
$\overline{G}$	Output Enable Input
$\overline{W}$	WRITE Enable Input
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 4. DIP Connections

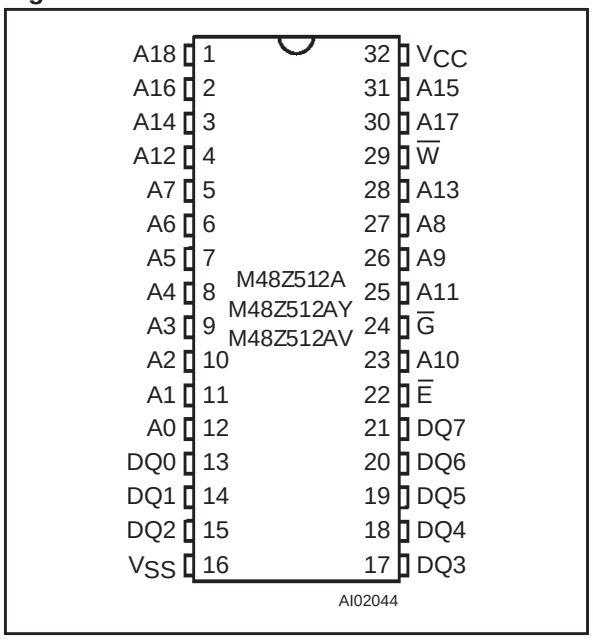


Figure 5. Block Diagram

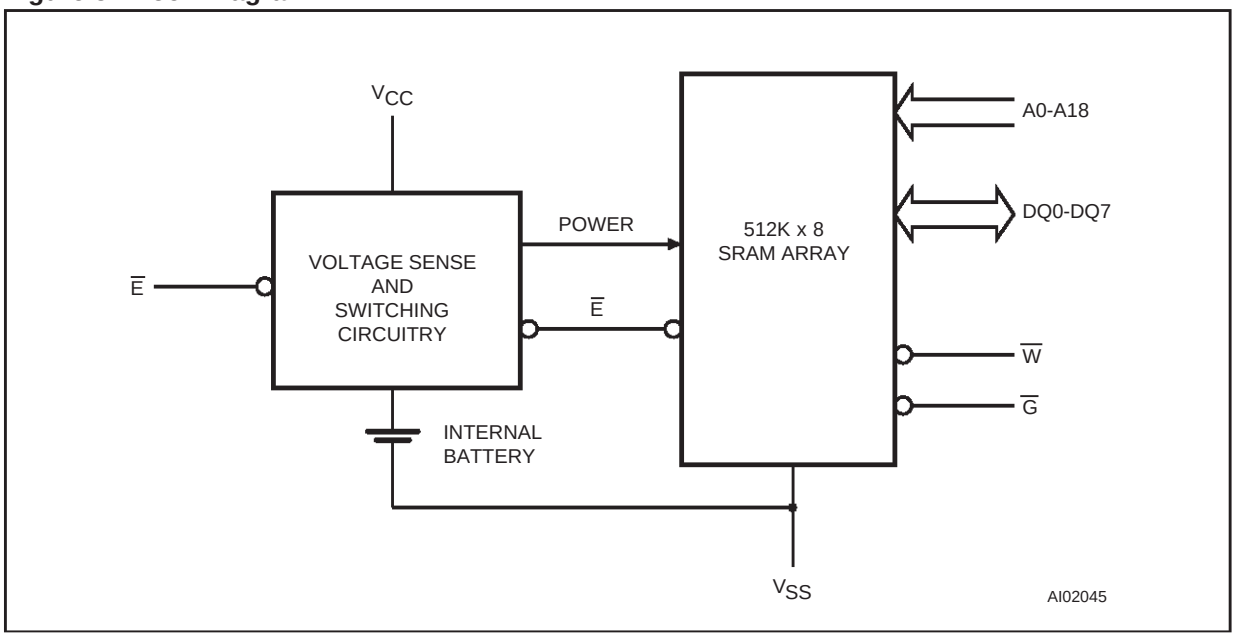
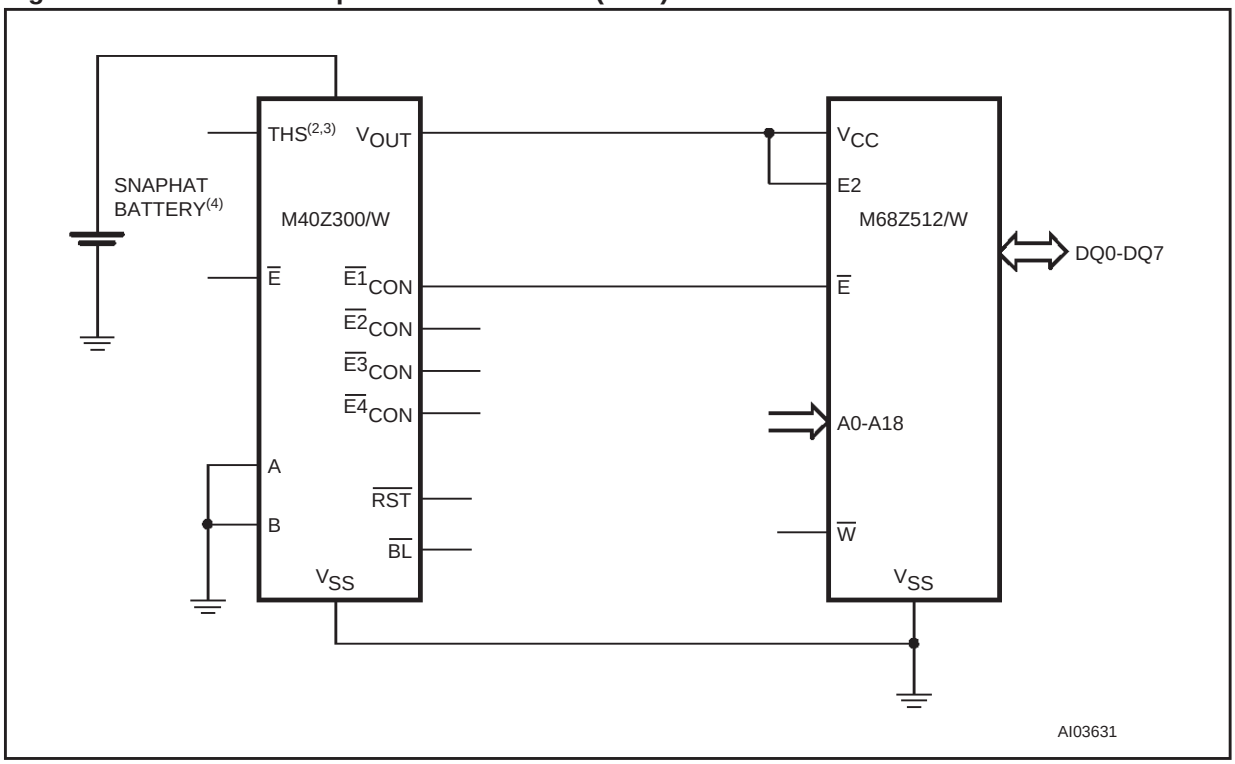


Figure 6. Hardware Hookup for Surface-Mount (SMT) Solution



Note: For pin connections, see individual data sheets for M48Z300/300W and M68Z512/512W at www.st.com.
1. Connect THS pin to V_{OUT} if $4.2V \le V_{PFD} \le 4.5V$ (M48Z512AY) or connect THS pin to V_{SS} if $4.5V \le V_{PFD} \le 4.75V$ (M48Z512A).
2. Connect THS pin to V_{SS} if $2.8V \le V_{PFD} \le 3.0V$ (M48Z512AV).
3. SNAPHAT® Top ordered separately.

Table 2. Surface-Mount (SMT) Solution

NVRAM	LPSRAM	SUPERVISOR	THS Pin(1)
M48Z512A	M68Z512	M40Z300	V_{SS}
M48Z512AY	M68Z512	M40Z300	V_{OUT}
M48Z512AV	M68Z512W	M40Z300W	V_{SS}

Note: 1. Connection of Threshold Select Pin (Pin 13) of SUPERVISOR (M40Z300/300W).

MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)		–40 to 85	°C
T_{BIAS}	Temperature Under Bias		–40 to 70	°C
T_{SLD}(1,2)	Lead Solder Temperature for 10 seconds		260	°C
V_{IO}	Input or Output Voltages		–0.3 to 7	V
V_{CC}	Supply Voltage	M48Z512A/512AY	–0.3 to 7.0	V
		M48Z512AV	–0.3 to 4.6	V
I_O	Output Current		20	mA
P_D	Power Dissipation		1	W

Note: 1. For DIP package: Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).
2. For SO package: Reflow at peak temperature of 215°C to 225°C for < 60 seconds (total thermal budget not to exceed 180°C for between 90 to 120 seconds).

CAUTION: *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*
CAUTION: *Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.*

DC AND AC PARAMETERS

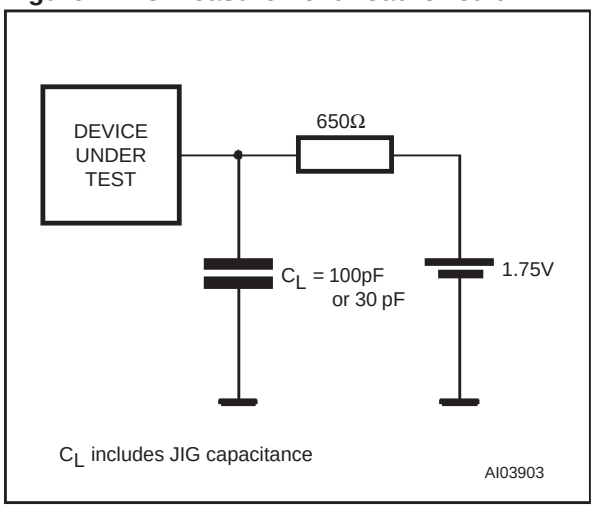
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 4. Operating and AC Measurement Conditions

Parameter	M48Z512A/512AY	M48Z512AV	Unit
Supply Voltage (V_{CC})	4.75 to 5.5V or 4.5 to 5.5	3.0 to 3.6	V
Ambient Operating Temperature (T_A)	0 to 70	0 to 70	°C
Load Capacitance (C_L)	100	50	pF
Input Rise and Fall Times	≤ 5	≤ 5	ns
Input Pulse Voltages	0 to 3	0 to 3	V
Input and Output Timing Ref. Voltages	1.5	1.5	V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 7. AC Measurement Load Circuit



Note: Excluding open drain output pins; 50pF for M48Z512AV.

Table 5. Capacitance

Symbol	Parameter(1,2)	Min	Max	Unit
C_{IN}	Input Capacitance		10	pF
C_{IO}(3)	Input / Output Capacitance		10	pF

Note: 1. Effective capacitance measured with power supply at 5V (M48Z512A/Y) or 3.3V (M48Z512AV); sampled only, not 100% tested.
2. Outputs deselected.
3. At 25°C.

Table 6. DC Characteristics

Sym	Parameter	Test Condition(1)	M48Z512A/Y		M48Z512AV		Unit
			–70		–85		
			Min	Max	Min	Max	
I_{LI}(2)	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1		±1	µA
I_{LO}(2)	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1		±1	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$ Outputs open		115		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		10		4	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} \ge V_{CC} - 0.2V$		5		3	mA
V_{IL}	Input Low Voltage		–0.3	0.8	–0.3	0.6	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		2.2		V

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5V, 4.5 to 5.5V, or 3.0 to 3.6V (except where noted).
2. Outputs deselected.

OPERATING MODES

The M48Z512A/Y/V also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single V_{CC} supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below the switchover voltage (V_{SO}), the control circuitry connects the battery which maintains data until valid power returns.

The ZEROPOWER® RAM replaces industry standard SRAMs. It provides the nonvolatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed.

Table 7. Operating Modes

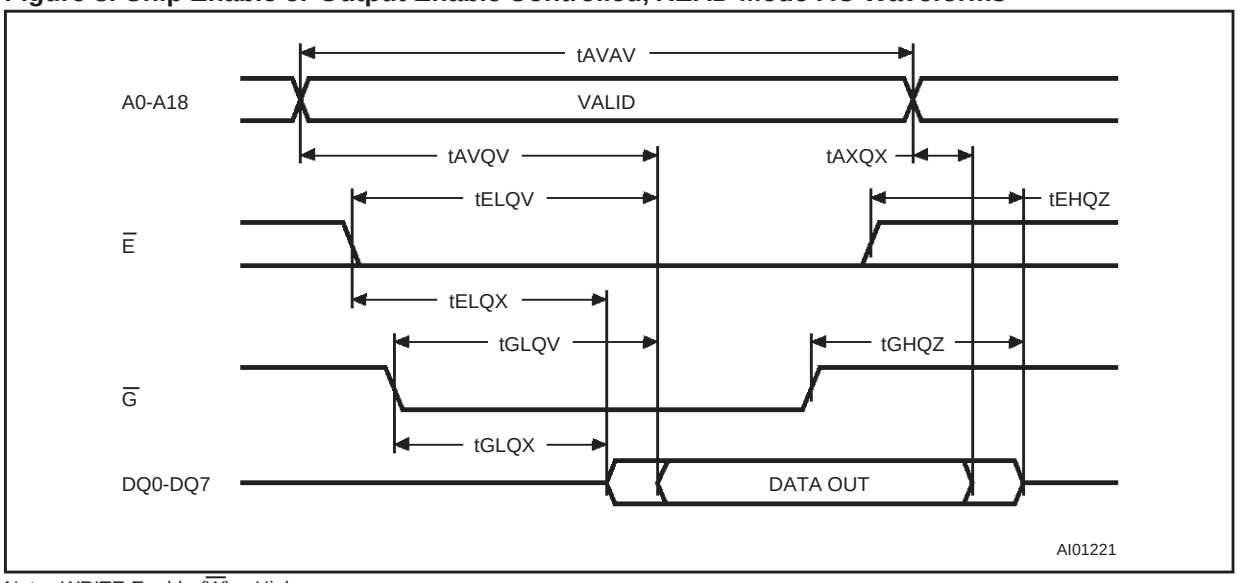
Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75 to 5.5V or 4.5 to 5.5V or 3.0 to 3.6V	V_{IH}	X	X	High Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)(1)	X	X	X	High Z	CMOS Standby
Deselect	$\le V_{SO}$(1)	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}; V_{SO} = Battery Back-up Switchover Voltage.
1. See Table 11, page 14 for details.

READ Mode

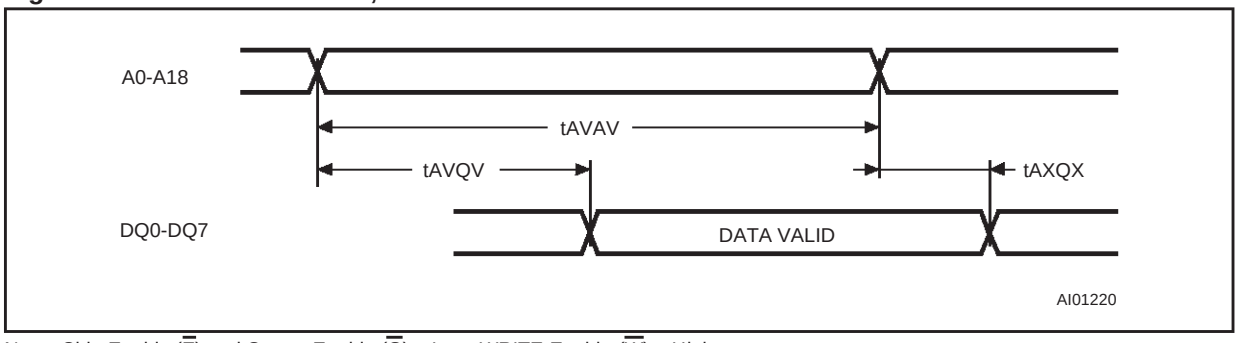
The M48Z512A/Y/V is in the READ Mode whenever $\overline{W}$ (WRITE Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 4,194,304 locations in the static storage array. Thus, the unique address specified by the 19 Address Inputs defines which one of the 524,288 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within Address Access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ (Chip Enable) and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of Chip Enable Access time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}). The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for Output Data Hold time (t_{AXQX}) but will go indeterminate until the next Address Access.

Figure 8. Chip Enable or Output Enable Controlled, READ Mode AC Waveforms



Note: WRITE Enable ($\overline{W}$) = High.

Figure 9. Address Controlled, READ Mode AC Waveforms



Note: Chip Enable ($\overline{E}$) and Output Enable ($\overline{G}$) = Low, WRITE Enable ($\overline{W}$) = High.

Table 8. READ Mode AC Characteristics

Symbol	Parameter[1]	M48Z512A/Y		M48Z512A/Y/V		Unit
		–70		–85		
		Min	Max	Min	Max	
t_{AVAV}	READ Cycle Time	70		85		ns
t_{AVQV}	Address Valid to Output Valid		70		85	ns
t_{ELQV}	Chip Enable Low to Output Valid		70		85	ns
t_{GLQV}	Output Enable Low to Output Valid		35		45	ns
t_{ELQX}[2]	Chip Enable Low to Output Transition	5		5		ns
t_{GLQX}[2]	Output Enable Low to Output Transition	5		5		ns
t_{EHQZ}[2]	Chip Enable High to Output Hi-Z		30		35	ns
t_{GHQZ}[2]	Output Enable High to Output Hi-Z		20		25	ns
t_{AXQX}	Address Transition to Output Transition	5		5		ns

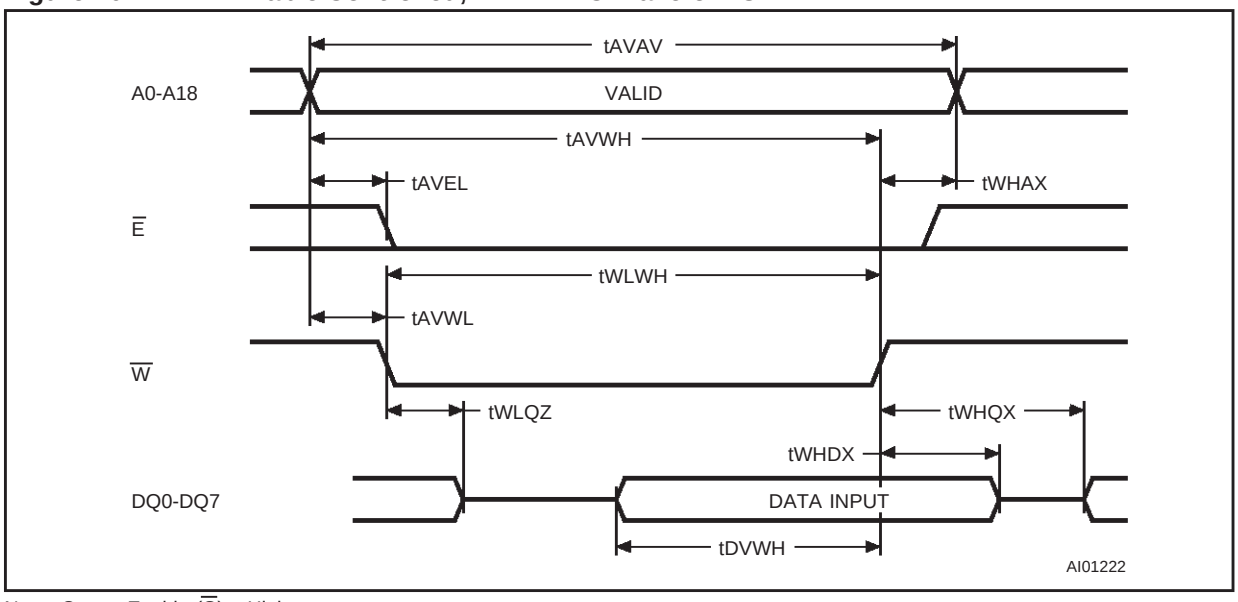
Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5V, 4.5 to 5.5V, or 3.0 to 3.6V (except where noted).
2. C_L = 5pF.

WRITE Mode

The M48Z512A/Y/V is in the WRITE Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$.

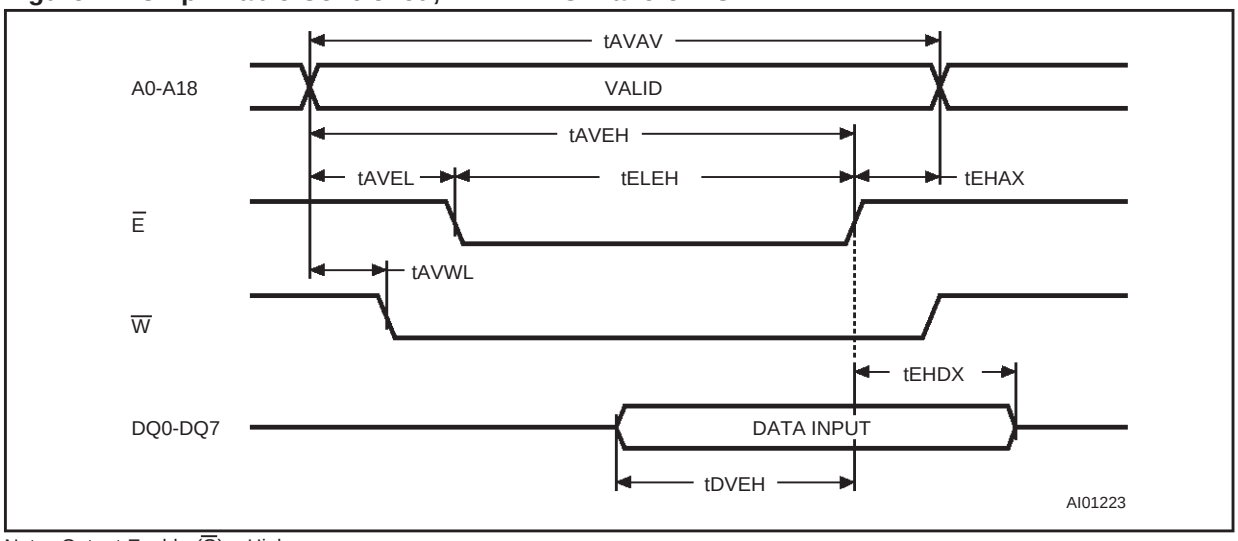
The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVEH} or t_{DVWH} prior to the end of WRITE and remain valid for t_{EHDX} or t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 10. WRITE Enable Controlled, WRITE AC Waveforms



Note: Output Enable ($\overline{G}$) = High.

Figure 11. Chip Enable Controlled, WRITE AC Waveforms



Note: Output Enable ($\overline{G}$) = High.

Table 9. WRITE Mode AC Characteristics

Symbol	Parameter(1)	M48Z512A/Y		M48Z512A/Y/V		Unit
		–70		–85		
		Min	Max	Min	Max	
t_{AVAV}	WRITE Cycle Time	70		85		ns
t_{AVWL}	Address Valid to WRITE Enable Low	0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{WLWH}	WRITE Enable Pulse Width	55		65		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	55		75		ns
t_{WHAX}	WRITE Enable High to Address Transition	5		5		ns
t_{EHAX}	Chip Enable High to Address Transition	15		15		ns
t_{DVWH}	Input Valid to WRITE Enable High	30		35		ns
t_{DVEH}	Input Valid to Chip Enable High	30		35		ns
t_{WHDX}	WRITE Enable High to Input Transition	0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	10		10		ns
t_{WLQZ}(2,3)	WRITE Enable Low to Output Hi-Z		25		30	ns
t_{AVWH}	Address Valid to WRITE Enable High	65		75		ns
t_{AVEH}	Address Valid to Chip Enable High	65		75		ns
t_{WHQX}(2,3)	WRITE Enable High to Output Transition	5		5		ns

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5V, 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. C_L = 5pF.
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

Data Retention Mode

With valid V_{CC} applied, the M48Z512A/Y/V operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When V_{CC} drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data.

The internal coin cell will maintain data in the M48Z512A/Y/V after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

For more information on Battery Storage Life refer to the Application Note AN1012.

Figure 12. Power Down/Up Mode AC Waveforms

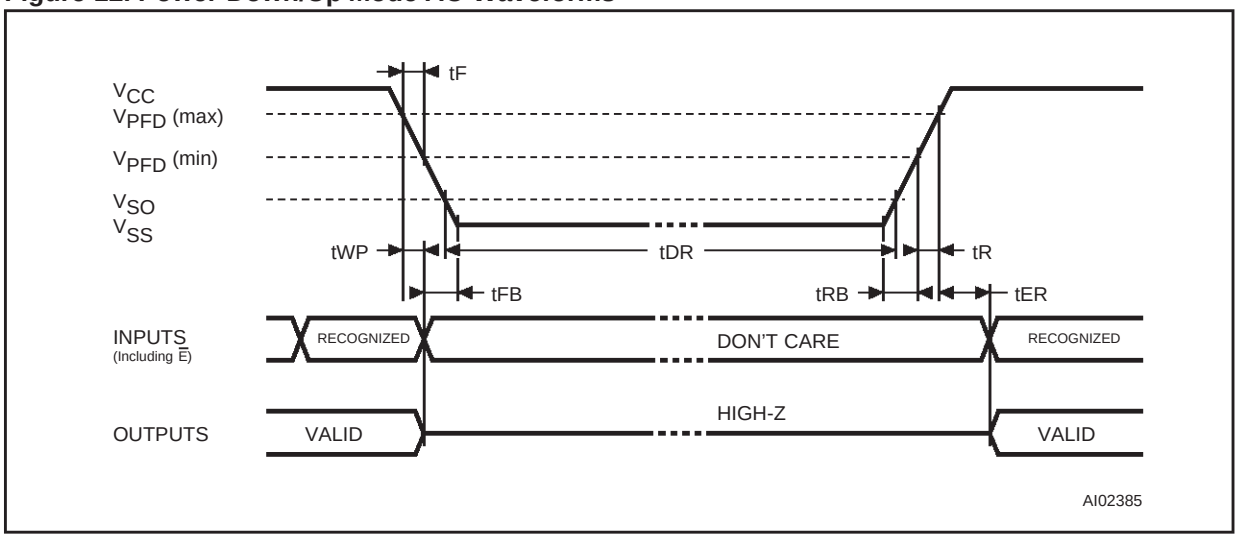


Table 10. Power Down/Up AC Characteristics

Symbol	Parameter(1)		Min	Max	Unit
t_F(2)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time		300		µs
t_{FB}(3)	V_{PFD} (min) to V_{SS} V_{CC} Fall Time	M48Z512A/Y	10		µs
		M48Z512AV	150		
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time		10		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} Rise Time		1		µs
t_{WPT}	Write Protect Time	M48Z512A/Y	40	150	µs
		M48Z512AV	40	250	
t_{ER}	$\overline{E}$ Recovery Time		40	120	ms

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5V, 4.5 to 5.5V, or 3.0 to 3.6V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

Table 11. Power Down/Up Trip Points DC Characteristics

Symbol	Parameter(1,2)		Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage	M48Z512A	4.5	4.6	4.75	V
		M48Z512AY	4.2	4.3	4.5	V
		M48Z512AV	2.8	2.9	3.0	V
V_{SO}	Battery Back-up Switchover Voltage	M48Z512A/Y		3.0		V
		M48Z512AV		2.5		V
t_{DR}(3)	Expected Data Retention Time		10			YEARS

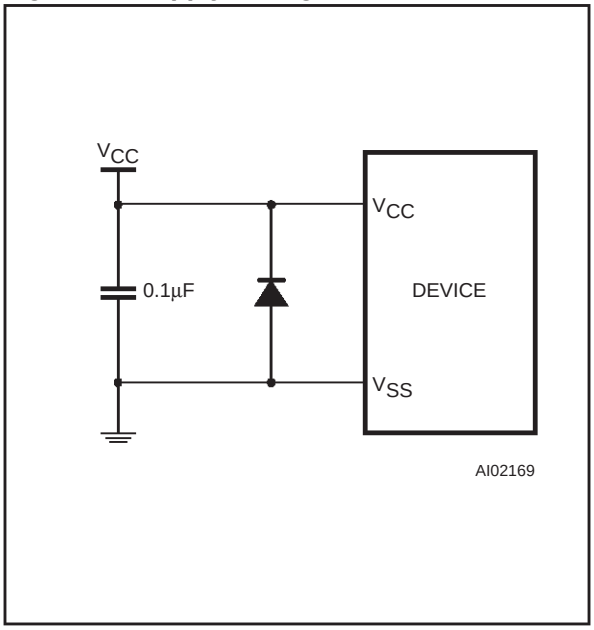
Note: 1. All voltages referenced to V_{SS}.
2. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5V, 4.5 to 5.5V, or 3.0 to 3.6V (except where noted).
3. At 25°C.

V_{CC} Noise And Negative Going Transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1µF (see Figure 13) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, ST recommends connecting a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). (Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface-mount).

Figure 13. Supply Voltage Protection



PART NUMBERING

Table 12. Ordering Information Scheme

Example: M48Z 512AY –70 PM 1

Device Type

M48Z

Supply Voltage and Write Protect Voltage

512A = V_{CC} = 4.75 to 5.5V; V_{PFD} = 4.5 to 4.75V

512AY = V_{CC} = 4.5 to 5.5V; V_{PFD} = 4.2 to 4.5V

512AV(1) = V_{CC} = 3.0 to 3.6V; V_{PFD} = 2.8 to 3.0V

Speed

–70 = 70ns (for M48Z512A/Y)

–85 = 85ns (for M48Z512A/Y/V)

Package(2)

PM = PMDIP32

Temperature Range

1 = 0 to 70°C

9 = Extended Temperature(3)

Note: 1. Contact Local Sales Office
2. The SOIC package (SOH28) requires the battery package (SNAPHAT®) which is ordered separately under the part number "M4Zxx-BR00SH" in plastic tube or "M4Zxx-BR00SHTR" in Tape & Reel form.
3. Contact Sales Offices for availability of Extended Temperature.

Caution: Do not place the SNAPHAT battery package "M4Zxx-BR00SH" in conductive foam as it will drain the lithium button-cell battery.

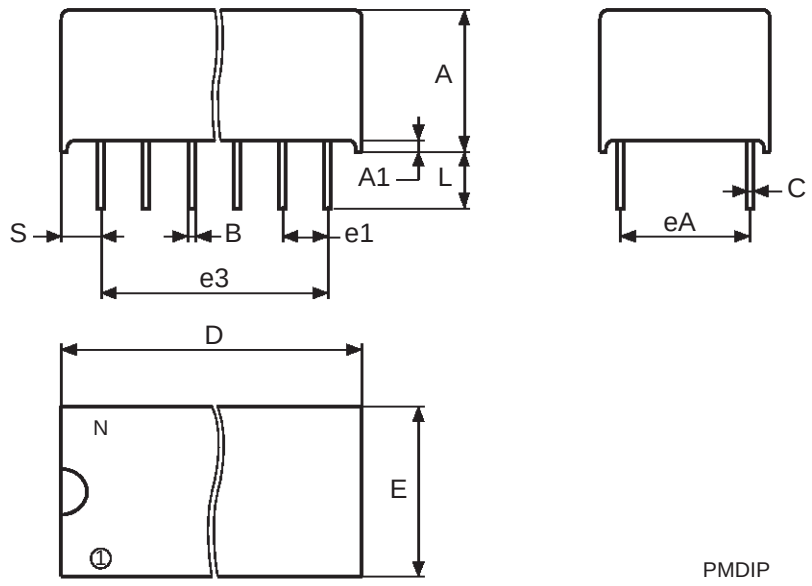
For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 13. SNAPHAT Battery Table

Part Number	Description	Package
M4Z28-BR00SH	Lithium Battery (48mAh) SNAPHAT	SH
M4Z32-BR00SH	Lithium Battery (120mAh) SNAPHAT	SH

PACKAGE MECHANICAL INFORMATION

Figure 14. PMDIP32 – 32-pin Plastic DIP Module, Package Outline

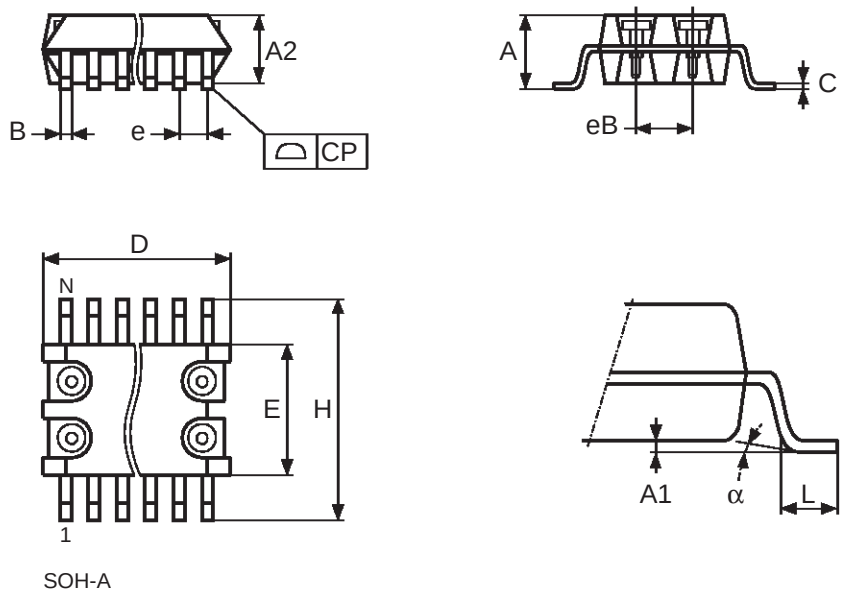


Note: Drawing is not to scale.

Table 14. PMDIP32 – 32-pin Plastic DIP Module, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		9.27	9.52		0.365	0.375
A1		0.38	–		0.015	–
B		0.43	0.59		0.017	0.023
C		0.20	0.33		0.008	0.013
D		42.42	43.18		1.670	1.700
E		18.03	18.80		0.710	0.740
e1		2.29	2.79		0.090	0.110
e3		34.29	41.91		1.350	1.650
eA		14.99	16.00		0.590	0.630
L		3.05	3.81		0.120	0.150
S		1.91	2.79		0.075	0.110
N	32			32		

Figure 15. SOH28 – 28-lead Plastic Small Outline, battery SNAPHAT, Package Outline

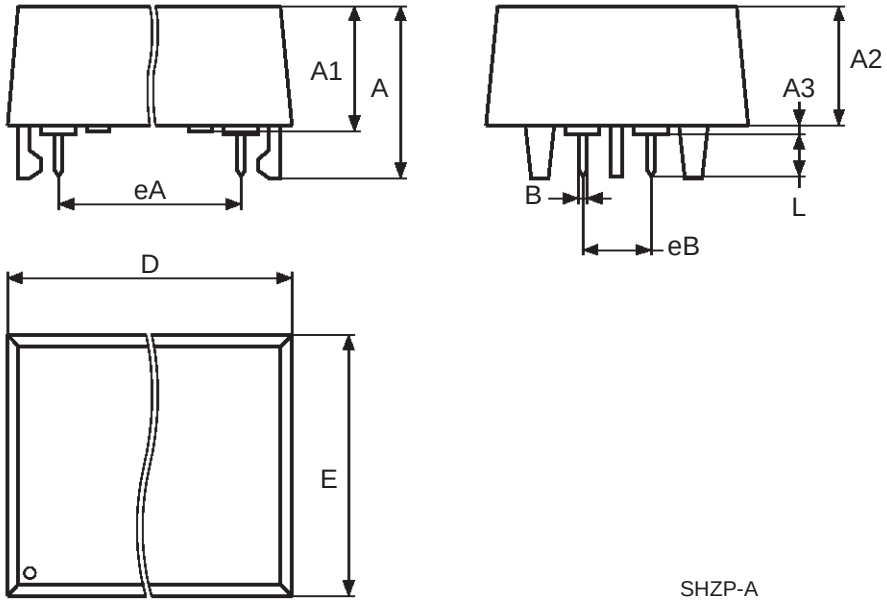


Note: Drawing is not to scale.

Table 15. SOH28 – 28-lead Plastic Small Outline, battery SNAPHAT, Package Mechanical Data

Symbol	mm			inch		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

Figure 16. SH – 4-pin SNAPHAT Housing for 48mAh Battery, Package Outline

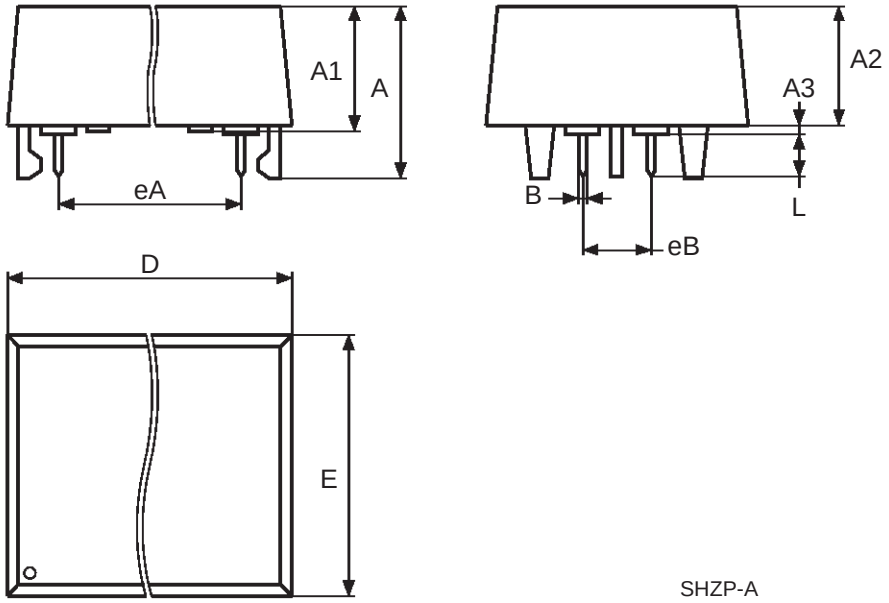


Note: Drawing is not to scale.

Table 16. SH – 4-pin SNAPHAT Housing for 48mAh Battery, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 17. SH – 4-pin SNAPHAT Housing for 120mAh Battery, Package Outline

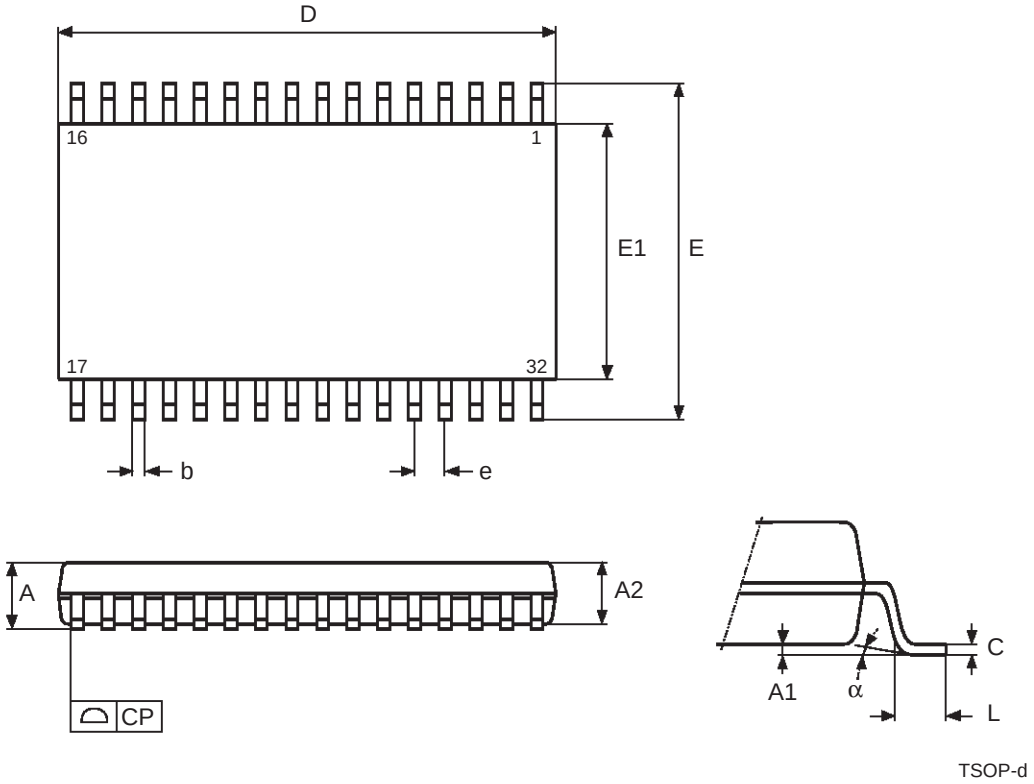


Note: Drawing is not to scale.

Table 17. SH - 4-pin SNAPHAT Housing for 120mAh Battery, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54			0.415
A1		8.00	8.51		0.315	0.335
A2		7.24	8.00		0.285	0.315
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	0.710
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 18. TSOP II 32 – 32-lead Plastic Thin Small Outline II, 10 x 20 mm, Package Outline



Note: Drawing is not to scale.

Table 18. TSOP II 32 – 32-lead Plastic Thin Small Outline II, 10 x 20 mm, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
b		0.30	0.52		0.012	0.020
C		0.12	0.21		0.005	0.008
D		20.82	21.08		0.820	0.830
e	1.27	–	–	0.050	–	–
E		11.56	11.96		0.455	0.471
E1		10.03	10.29		0.395	0.405
L		0.40	0.60		0.016	0.024
α		0°	5°		0°	5°
CP			0.10			0.004

REVISION HISTORY

Table 19. Revision History

Date	Revision Details
March 2000	First Issue
07/19/00	M48Z12AV added
01/15/01	Changed LPSRAM device (Table 2)
12/19/01	Reformatted; added temperature information (Table 5, 6, 8, 9, 10, 11); remove chipset option from Ordering Information (Table 12); remove reference to “clock”
02/08/02	Remove 85ns speed grade (Table 6, 8, and 9)
05/29/02	Modify reflow time and temperature footnotes (Table 3)

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