# 74VHC373

## OCTAL D-TYPE LATCH WITH 3 STATE OUTPUTS NON INVERTING

- HIGH SPEED: $t_{PD}$ = 5.0 ns (TYP.) at $V_{CC}$ = 5V
- LOW POWER DISSIPATION: $I_{CC}$ = 4 µA (MAX.) at $T_A$=25°C
- HIGH NOISE IMMUNITY: $V_{NIH} = V_{NIL}$ = 28% $V_{CC}$ (MIN.)
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE: $|I_{OH}| = I_{OL}$ = 8 mA (MIN)
- BALANCED PROPAGATION DELAYS: $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE: $V_{CC}$(OPR) = 2V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 373
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: $V_{OLP}$ = 0.9V (MAX.)

SOP TSSOP

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| SOP | 74VHC373M | 74VHC373MTR |
| TSSOP | | 74VHC373TTR |

### DESCRIPTION

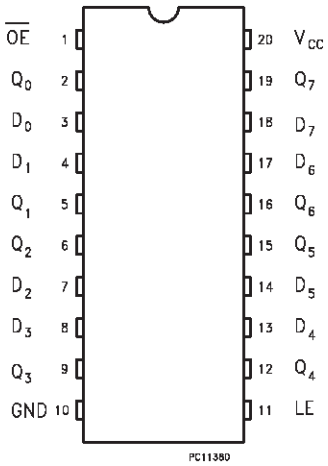
The 74VHC373 is an advanced high-speed CMOS OCTAL D-TYPE LATCH with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring $C^2$MOS technology.

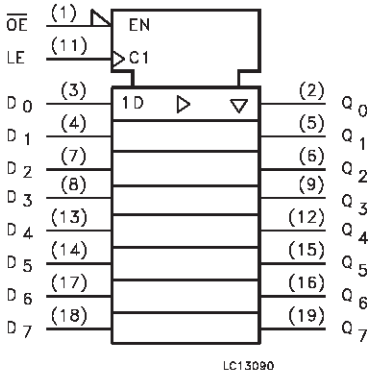
These 8 bit D-Type latch are controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$). While the LE inputs is held at a high level, the Q outputs will follow the data input precisely . When the LE is taken low, the Q outputs will be latched precisely at the logic level of D input data. While the ($\overline{OE}$) input is low, the 8 outputs will be in a normal logic state (high or low logic level) and while ($\overline{OE}$) is in high level, the outputs will be in a high impedance state.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

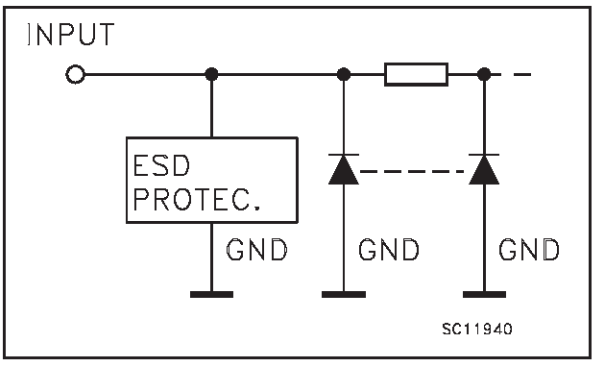
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



## INPUT EQUIVALENT CIRCUIT




## PIN DESCRIPTION

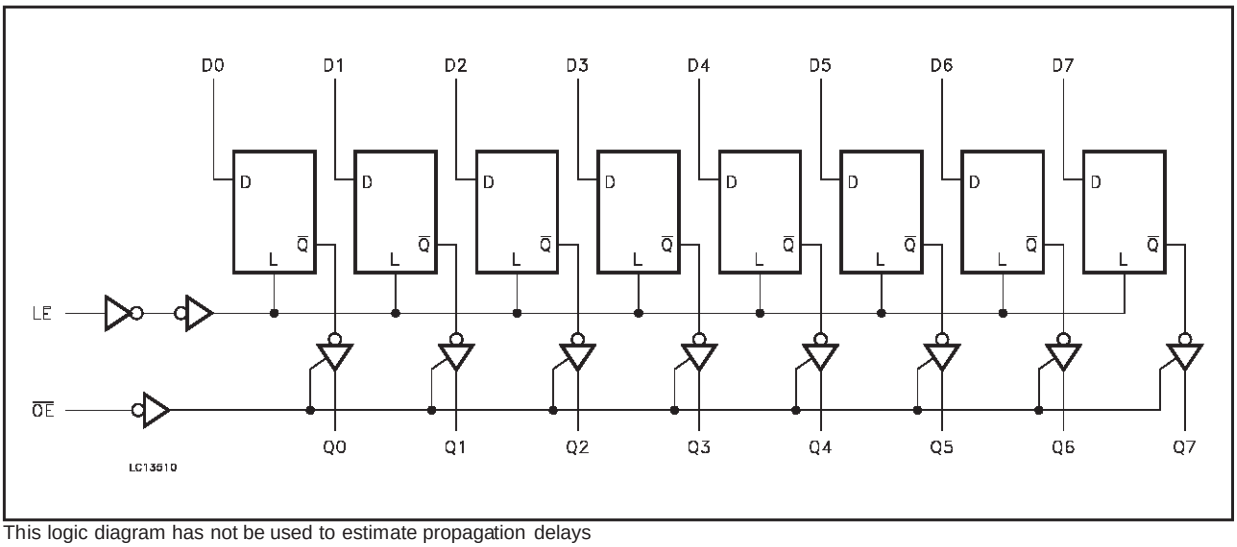
| PIN No | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1 | $\overline{OE}$ | 3 State Output Enable Input (Active LOW) |
| 2, 5, 6, 9, 12, 15, 16,19 | D0 to D7 | Data Inputs |
| 3, 4, 7, 8, 13, 14, 17, 18 | Q0 to Q7 | 3-State Outputs |
| 11 | LE | Latch Enable Input |
| 10 | GND | Ground (0V) |
| 20 | $V_{CC}$ | Positive Supply Voltage |

## TRUTH TABLE

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| H | X | X | Z |
| L | L | X | NO CHANGE* |
| L | H | L | L |
| L | H | H | H |

X : Don't Care
Z : High Impedance
* : Q Outputs are Latched at the time when the LE INPUT is taken low logic level

## LOGIC DIAGRAM




This logic diagram has not be used to estimate propagation delays

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.5 to +7.0 | V |
| $V_I$ | DC Input Voltage | -0.5 to +7.0 | V |
| $V_O$ | DC Output Voltage | -0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | DC Input Diode Current | - 20 | mA |
| $I_{OK}$ | DC Output Diode Current | ± 20 | mA |
| $I_O$ | DC Output Current | ± 25 | mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ or Ground Current | ± 75 | mA |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |
| $T_L$ | Lead Temperature (10 sec) | 300 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2 to 5.5 | V |
| $V_I$ | Input Voltage | 0 to 5.5 | V |
| $V_O$ | Output Voltage | 0 to $V_{CC}$ | V |
| $T_{op}$ | Operating Temperature | -55 to 125 | °C |
| dt/dv | Input Rise and Fall Time (note 1) ($V_{CC}$ = 3.3 ± 0.3V)<br>($V_{CC}$ = 5.0 ± 0.5V) | 0 to 100<br>0 to 20 | ns/V |

1) $V_{IN}$ from 30% to 70% of $V_{CC}$

## DC SPECIFICATIONS

| Symbol | Parameter | Test Condition | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | | $T_A$ = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $V_{IH}$ | High Level Input Voltage | 2.0 | | 1.5 | | | 1.5 | | 1.5 | | V |
| | | 3.0 to 5.5 | | $0.7V_{CC}$ | | | $0.7V_{CC}$ | | $0.7V_{CC}$ | | |
| $V_{IL}$ | Low Level Input Voltage | 2.0 | | | | 0.5 | | 0.5 | | 0.5 | V |
| | | 3.0 to 5.5 | | | | $0.3V_{CC}$ | | $0.3V_{CC}$ | | $0.3V_{CC}$ | |
| $V_{OH}$ | High Level Output Voltage | 2.0 | $I_O$=-50 µA | 1.9 | 2.0 | | 1.9 | | 1.9 | | V |
| | | 3.0 | $I_O$=-50 µA | 2.9 | 3.0 | | 2.9 | | 2.9 | | |
| | | 4.5 | $I_O$=-50 µA | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | 3.0 | $I_O$=-4 mA | 2.58 | | | 2.48 | | 2.4 | | |
| | | 4.5 | $I_O$=-8 mA | 3.94 | | | 3.8 | | 3.7 | | |
| $V_{OL}$ | Low Level Output Voltage | 2.0 | $I_O$=50 µA | | 0.0 | 0.1 | | 0.1 | | 0.1 | V |
| | | 3.0 | $I_O$=50 µA | | 0.0 | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 | $I_O$=50 µA | | 0.0 | 0.1 | | 0.1 | | 0.1 | |
| | | 3.0 | $I_O$=4 mA | | | 0.36 | | 0.44 | | 0.55 | |
| | | 4.5 | $I_O$=8 mA | | | 0.36 | | 0.44 | | 0.55 | |
| Ioz | High Impedance Output Leakage Current | 5.5 | $V_I = V_{IH}$ or $V_{IL}$<br>$V_O = V_{CC}$ or GND | | | ±0.25 | | ± 2.5 | | ± 2.5 | µA |
| $I_I$ | Input Leakage Current | 0 to 5.5 | $V_I$ = 5.5V or GND | | | ± 0.1 | | ± 1 | | ± 1 | µA |
| $I_{CC}$ | Quiescent Supply Current | 5.5 | $V_I = V_{CC}$ or GND | | | 4 | | 40 | | 40 | µA |

## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

| Symbol | Parameter | Test Condition | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | $C_L$ (pF) | | $T_A = 25°C$ | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time LE to Q | 3.3(*) | 15 | | | 7.0 | 11.0 | 1.0 | 13.0 | 1.0 | 13.0 | ns |
| | | 3.3(*) | 50 | | | 9.5 | 14.5 | 1.0 | 16.5 | 1.0 | 16.5 | |
| | | 5.0(**) | 15 | | | 4.9 | 7.2 | 1.0 | 8.5 | 1.0 | 8.5 | |
| | | 5.0(**) | 50 | | | 6.4 | 9.2 | 1.0 | 10.5 | 1.0 | 10.5 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time D to Q | 3.3(*) | 15 | | | 7.3 | 11.4 | 1.0 | 13.5 | 1.0 | 13.5 | ns |
| | | 3.3(*) | 50 | | | 9.8 | 14.9 | 1.0 | 17.0 | 1.0 | 17.0 | |
| | | 5.0(**) | 15 | | | 5.0 | 7.2 | 1.0 | 8.5 | 1.0 | 8.5 | |
| | | 5.0(**) | 50 | | | 6.5 | 9.2 | 1.0 | 10.5 | 1.0 | 10.5 | |
| $t_{PZL}$ $t_{PZH}$ | Output Enable Time | 3.3(*) | 15 | $R_L = 1K\Omega$ | | 7.3 | 11.4 | 1.0 | 13.5 | 1.0 | 13.5 | ns |
| | | 3.3(*) | 50 | $R_L = 1K\Omega$ | | 9.8 | 14.9 | 1.0 | 17.0 | 1.0 | 17.0 | |
| | | 5.0(**) | 15 | $R_L = 1K\Omega$ | | 5.5 | 8.1 | 1.0 | 9.5 | 1.0 | 9.5 | ns |
| | | 5.0(**) | 50 | $R_L = 1K\Omega$ | | 7.0 | 10.1 | 1.0 | 11.5 | 1.0 | 11.5 | |
| $t_{PLZ}$ $t_{PHZ}$ | Output Disable Time | 3.3(*) | 50 | $R_L = 1K\Omega$ | | 9.5 | 13.2 | 1.0 | 15.0 | 1.0 | 15.0 | ns |
| | | 5.0(**) | 50 | $R_L = 1K\Omega$ | | 6.5 | 9.2 | 1.0 | 10.5 | 1.0 | 10.5 | |
| $t_w$ | Pulse Width (LE) HIGH | 3.3(*) | | | | | 5.0 | | 5.0 | | 5.0 | ns |
| | | 5.0(**) | | | | | 5.0 | | 5.0 | | 5.0 | |
| $t_s$ | Setup Time D to LE HIGH or LOW | 3.3(*) | | | | | 4.0 | | 4.0 | | 4.0 | ns |
| | | 5.0(**) | | | | | 4.0 | | 4.0 | | 4.0 | |
| $t_h$ | Setup Time D to LE HIGH or LOW | 3.3(*) | | | | | 1.0 | | 1.0 | | 1.0 | ns |
| | | 5.0(**) | | | | | 1.0 | | 1.0 | | 1.0 | |
| $t_{OSLH}$ $t_{OSHL}$ | Output to Output Skew time (note 1) | 3.3(*) | 50 | | | | 1.5 | | 1.5 | | 1.5 | ns |
| | | 5.0(**) | 50 | | | | 1.0 | | 1.0 | | 1.0 | |

(*) Voltage range is 3.3V ± 0.3V
(**) Voltage range is 5.0V ± 0.5V
Note 1 : Parameter guaranteed by design. $t_{soLH} = |t_{pLHm} - t_{pLHn}|$, $t_{soHL} = |t_{pHLm} - t_{pHLn}|$

## CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Test Condition | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A = 25°C$ | | | -40 to 85°C | | -55 to 125°C | | |
| | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $C_{IN}$ | Input Capacitance | | | 7 | 10 | | 10 | | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | | 9 | | | | | | pF |
| $C_{PD}$ | Power Dissipation Capacitance (note 1) | | | 15 | | | | | | pF |

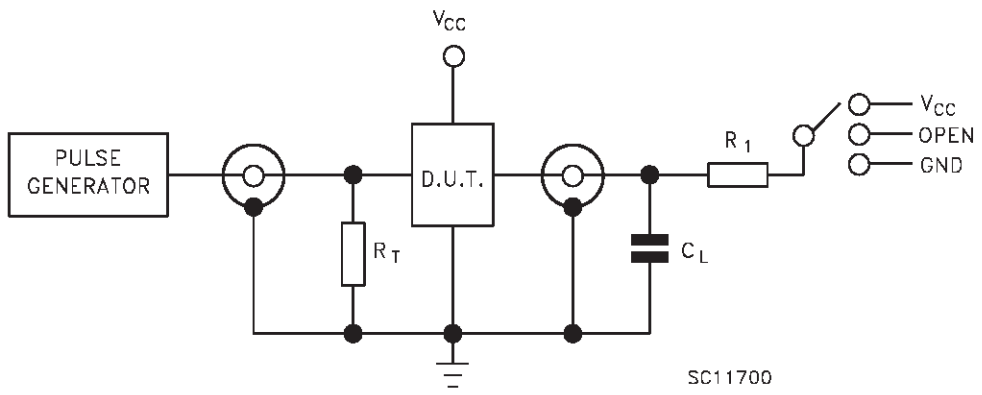
1) $C_{PD}$ is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per Latch)

## DYNAMIC SWITCHING CHARACTERISTICS

| Symbol | Parameter | Test Condition | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | | $T_A$ = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $V_{OLP}$ | Dynamic Low Voltage Quiet Output (note 1, 2) | 5.0 | $C_L$ = 50 pF | | 0.6 | 0.9 | | | | | V |
| $V_{OLV}$ | | | | -0.9 | -0.6 | | | | | | |
| $V_{IHD}$ | Dynamic High Voltage Input (note 1, 3) | 5.0 | | 3.5 | | | | | | | V |
| $V_{ILD}$ | Dynamic Low Voltage Input (note 1, 3) | 5.0 | | | | 1.5 | | | | | V |

1) Worst case package.
2) Max number of outputs defined as (n). Data inputs are driven 0V to 5.0V, (n-1) outputs switching and one output at GND.
3) Max number of data inputs (n) switching. (n-1) switching 0V to 5.0V. Inputs under test switching: 5.0V to threshold ($V_{ILD}$), 0V to threshold ($V_{IHD}$), f=1MHz.

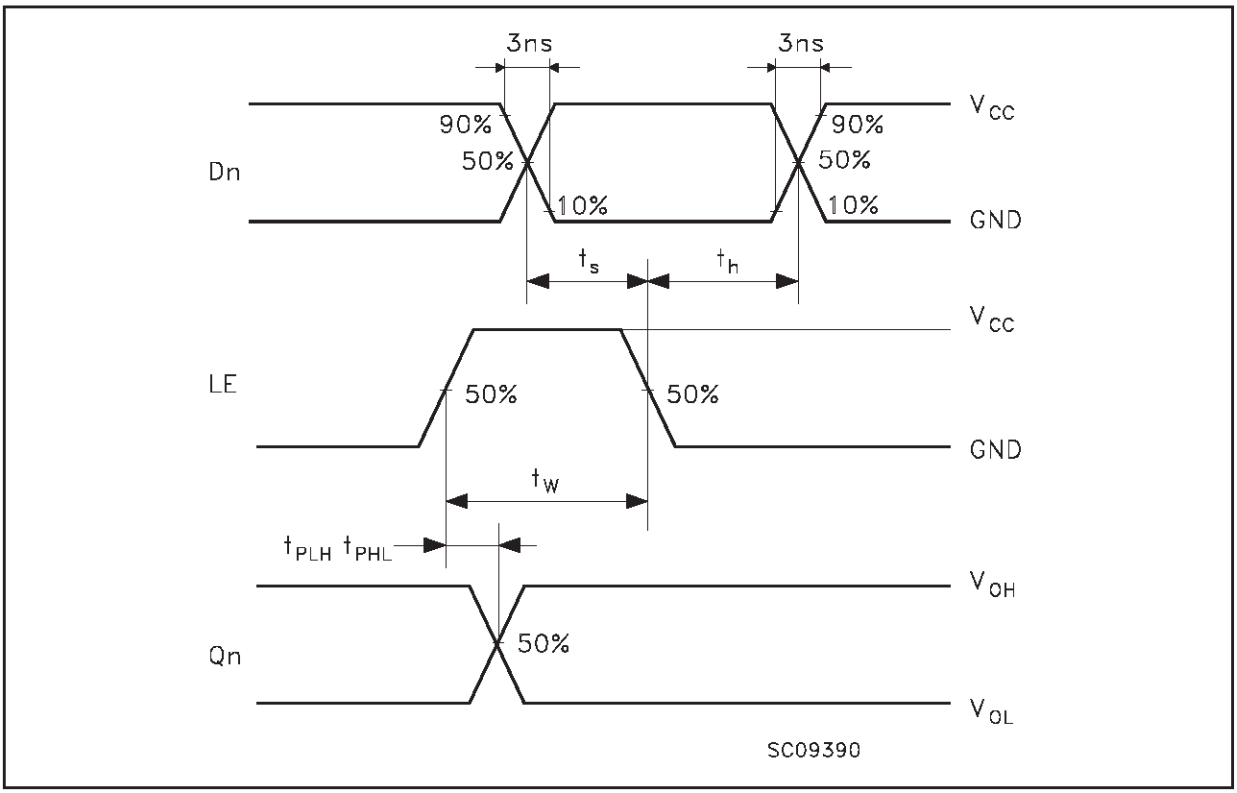
## TEST CIRCUIT



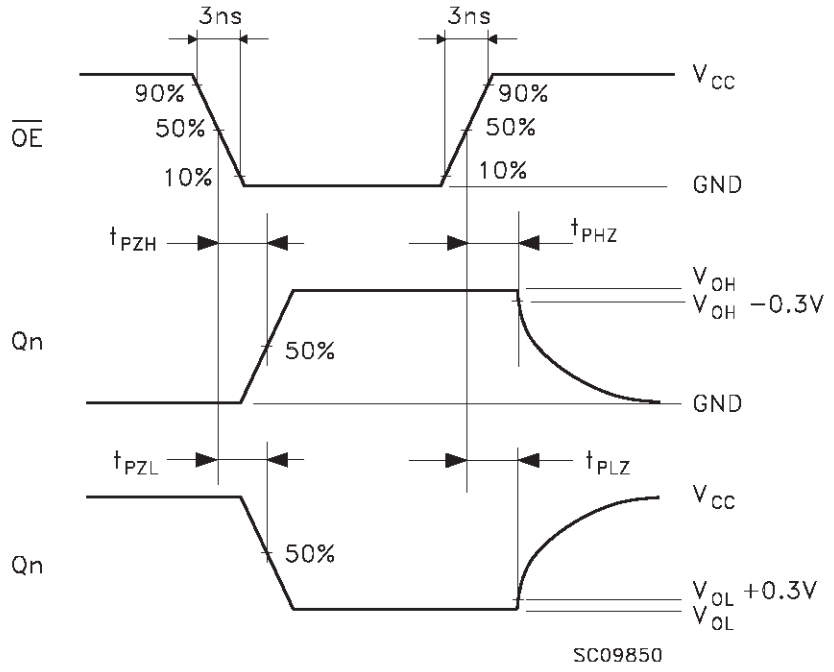

| TEST | SWITCH |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | $V_{CC}$ |
| $t_{PZH}$, $t_{PHZ}$ | GND |

$C_L$ =15/50pF or equivalent (includes jig and probe capacitance)
$R_L$ = R1 = 1KΩ or equivalent
$R_T$ = $Z_{OUT}$ of pulse generator (typically 50Ω)

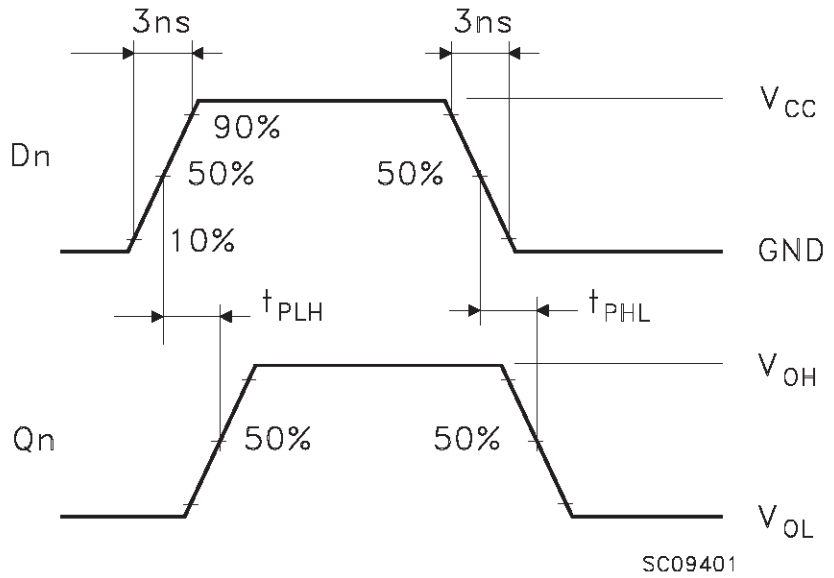
**WAVEFORM 1: LE TO Qn PROPAGATION DELAYS, LE MINIMUN PULSE WIDTH, Dn TO LE SETUP AND HOLD TIMES** (f=1MHz; 50% duty cycle)



**WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES** (f=1MHz; 50% duty cycle)

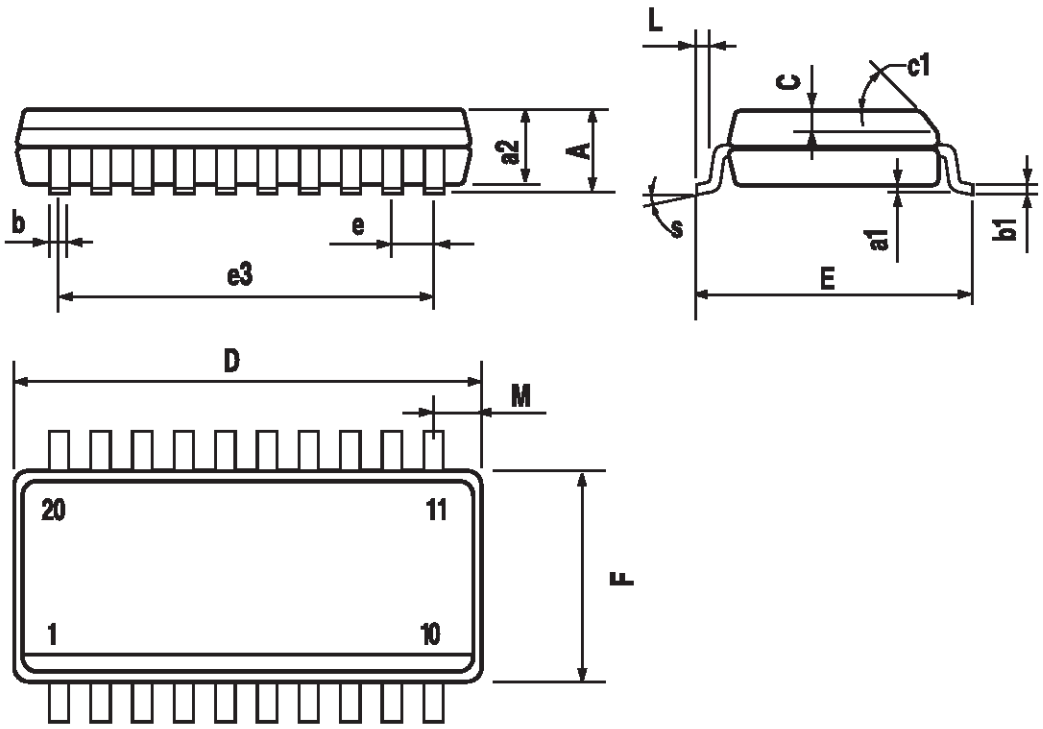



**WAVEFORM 3: PROPAGATION DELAY TIME** (f=1MHz; 50% duty cycle)



## SO-20 MECHANICAL DATA

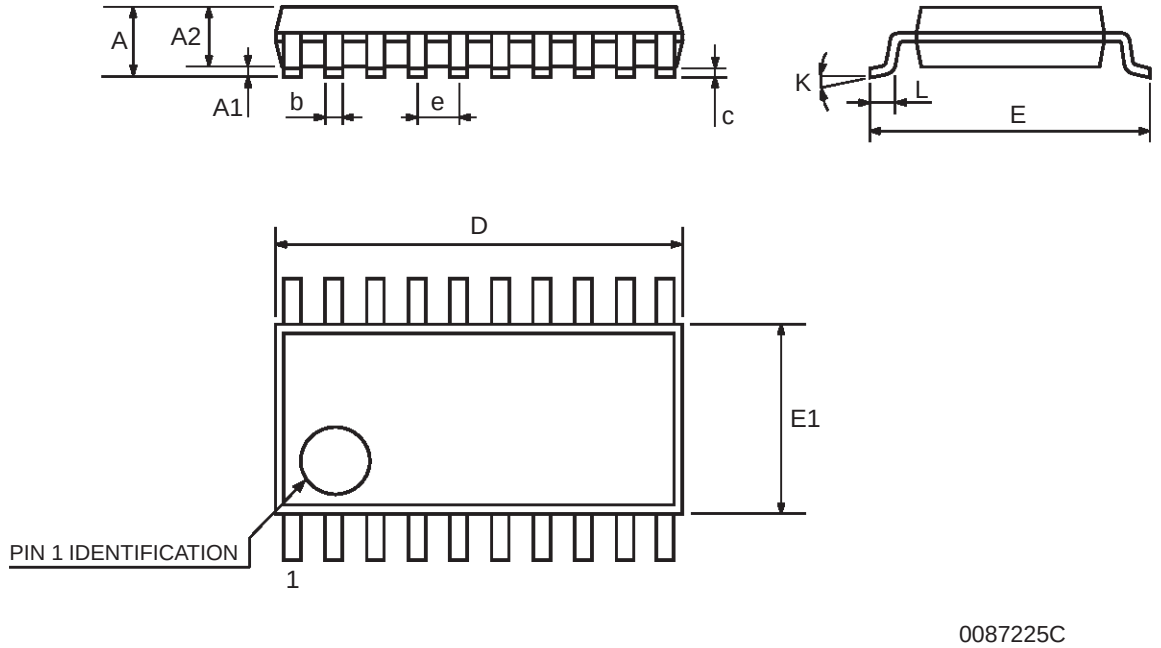
| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.1 | | 0.2 | 0.004 | | 0.008 |
| a2 | | | 2.45 | | | 0.096 |
| b | 0.35 | | 0.49 | 0.014 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.012 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 12.60 | | 13.00 | 0.496 | | 0.512 |
| E | 10.00 | | 10.65 | 0.393 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 11.43 | | | 0.450 | |
| F | 7.40 | | 7.60 | 0.291 | | 0.300 |
| L | 0.50 | | 1.27 | 0.020 | | 0.050 |
| M | | | 0.75 | | | 0.029 |
| S | 8° (max.) | | | | | |




PO13L

## TSSOP20 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.2 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.8 | 1 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.0089 |
| D | 6.4 | 6.5 | 6.6 | 0.252 | 0.256 | 0.260 |
| E | 6.2 | 6.4 | 6.6 | 0.244 | 0.252 | 0.260 |
| E1 | 4.3 | 4.4 | 4.48 | 0.169 | 0.173 | 0.176 |
| e | | 0.65 BSC | | | 0.0256 BSC | |
| K | 0° | | 8° | 0° | | 8° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |



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