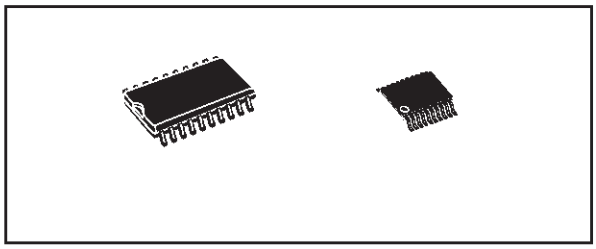
- HIGH SPEED: t_{PD} = 5.0 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION:
  I_{CC} = 4 µA (MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 8 mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC}(OPR) = 2V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH
  74 SERIES 573
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: V_{OLP} = 0.9V (MAX.)



DESCRIPTION

The 74VHC573 is an advanced high-speed CMOS OCTAL D-TYPE LATCH with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.

These 8 bit D-Type latch are controlled by a latch enable input (LE) and an output enable input (OE). While the LE inputs is held at a high level, the Q outputs will follow the data input precisely . When the LE is taken low, the Q outputs will be latched precisely at the logic level of D input data. While the (OE) input is low, the 8 outputs will be in