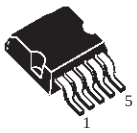
ST1534A

500mA SMART LDO

FEAURES

- GLITCH FREE TRANSITION BETWEEN INPUT SOURCES
- INTERNAL LOGIC SELECTS INPUT SOURCE
- GATE DRIVE FOR EXTERNAL PMOS BYPASS SWITCH
- 5V DETECTOR WITH HYSTERESIS
- 1% 3.3V REGULATED OUTPUT VOLTAGE
- 500mA GUARANTEED OUTPUT CURRENT
- OPERATING TEMPERATURE RANGE FROM 0°C TO 85°C
- AVAILABLE IN P^2PAK AND THE SMALLER PPAK PACKAGES



P^2PAK

PPAK

APPLICATIONS

- NETWORK INTERFACE CARDS
- PCMCIA/PCI INTERFACE CARDS
- DESKTOP COMPUTERS
- POWER SUPPLY WITH MULTIPLE INPUT SOURCES

DESCRIPTION

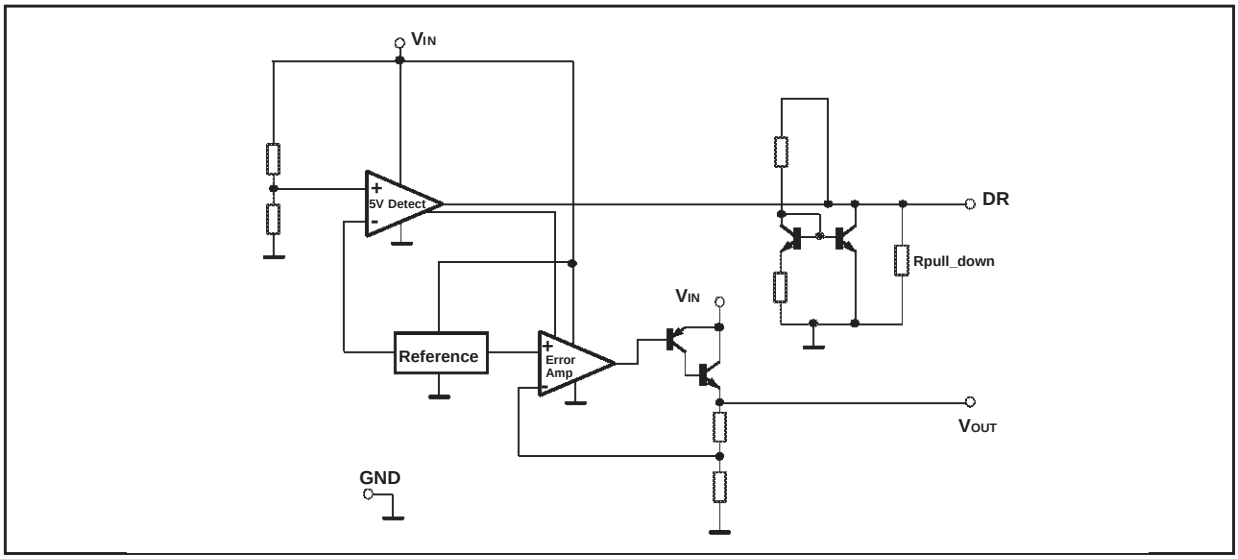
The ST1534A is lintended for application such as power managed PCI and network interface cards (NICs), where operations from 3.3V VAUX supply may be required when the 5V supply has been shut down.

During regular operation, 3.3V power for the PCI card is provided by the internal LDO regulator, generated from 5V supply. When the 5V V_{AUX} is available, theIC connects this supply directly to its output using an external P-Channel FET. This ensures an uninterrupted 3.3V out even if VIN falls out of specification.

When both supplies are available simultaneously, the drive pin DR will be pulled high, turning off the PMOS switch.

The device is available in the popular 5 leads P^2PAK and PPAK

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

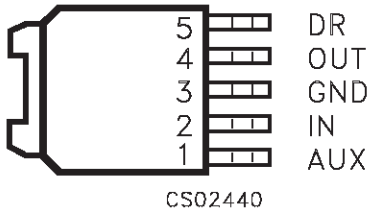
Symbol	Parameter	Value	Unit
V_I	DC Input Voltage	-0.3 to 7	V
V_{SHDN}	Shutdown Input Voltage	-0.3 to 7	V
I_O	Output Current	Internally limited	mA
T_{stg}	Storage Temperature Range	-40 to +125	°C
T_{op}	Operating Junction Temperature Range	0 to +85	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

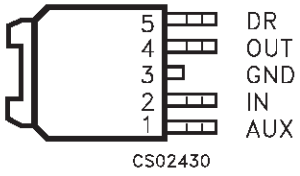
THERMAL DATA

Symbol	Parameter	PPAK	P^2PAK	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	8	3	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	100	50	°C/W

CONNECTION DIAGRAM (top view)



P^2PAK



PPAK

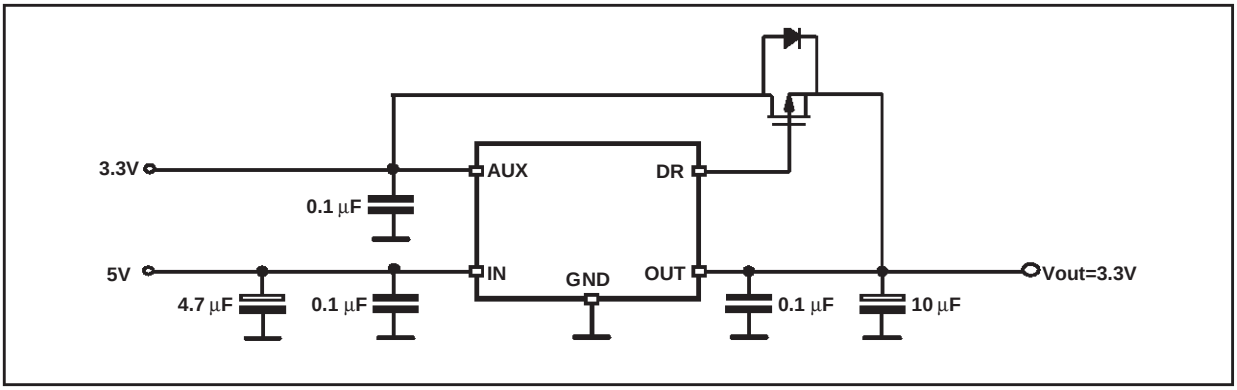
PIN DESCRIPTION

Pin N°	Symbol	Name and Function
1	AUX	Auxliary Input port typically 3.3V
2	IN	Input port typically 5V
3	GND	Ground
4	OUT	LDO 3.3V Output Port
5	DR	Drive Output for external P-Channel MOSFET pass element

ORDERING INFORMATION

TYPE	PPAK	P^2PAK
ST1534A	ST1534APT	ST1534AP2T

TYPICAL APPLICATION CIRCUIT

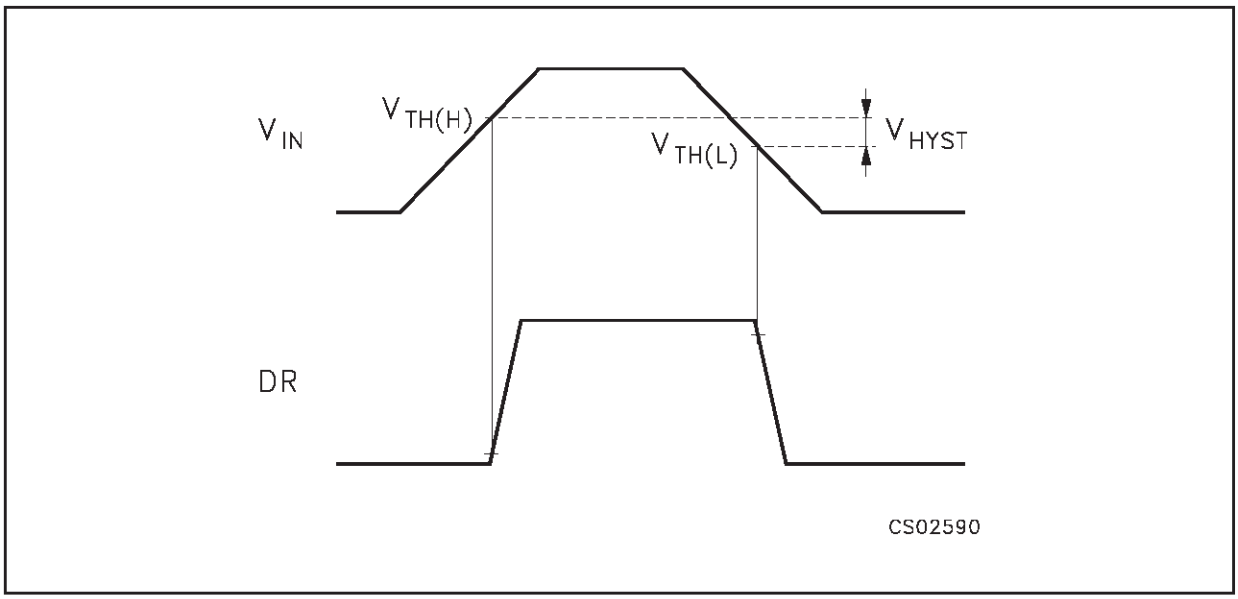


ELECTRICAL CHARACTERISTICS (T_j = 25°C, V_I=5V, V_{AUX}=3.3V, I_O=10mA, C_O = 2.2µF, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_I	Input Voltage Range		4.5	5	5.5	V
I_{IN}	Input Supply Current	$V_I \geq 4.5V$ I_O = 0mA V_{AUX} = 0V		11		mA
		$V_I \geq 4.5V$ I_O = 0mA V_{AUX} = 3.3V		11		mA
		$V_I < 4.1V$ I_O = 0mA V_{AUX} = 0V		2		mA
		$V_I < 4.1V$ I_O = 0mA V_{AUX} = 3.3V		2		mA
I_{AUX}	Auxliary Supply Current	V_I = 0 V		2.2		mA
		V_I = 5V		200		µA
3.3V VOLTAGE REGULATOR BLOCK						
V_O	Output Voltage	T_j = 0 to 85 °C	3.18	3.3	3.42	V
ΔV_O	Line Regulation	V_I = 4.5 to 5.5V		0.04	0.5	%
ΔV_O	Load Regulation	I_O = 0 to 500mA		0.1	1	%
V_d	Dropout Voltage	I_O = 500 mA T_j = 0 to 85 °C			1.15	V
I_O	Output Current Limit	T_j = 0 to 85 °C	550			mA
5V DETECT BLOCK						
V_{THL}	Low Threshold Voltage	V_I falling, I_O = 500 mA T_j = 0 to 85 °C	4.15		4.3	V
V_{HYST}	Hysteresis		70		200	mV
DRIVE OUTPUT BLOCK						
V_{DR}	Drive Output Voltage	V_I = 4.5 to 5.5V I_{DR} = 200 µA	3.6	V_{IN}-0.8		V
		V_I < 4.15V I_{DR} = 200 µA		100	200	mV
I_{DR}	Drive Current	Sinking: V_I = 4.15V V_{DR} = 1V	7	20		mA
		Sourcing: V_I = 4.5V $V_I - V_{DR}$ = 2V	7	25		mA
t_{DH}	Drive High Delay (Note 1 and 2)	C_{DR} = 1.2nF, V_{IN} ramping up, measured from $V_I = V_{TH(H)}$ to V_{DR} = 3.3V T_j = 0 to 85 °C		2	5	µs
t_{DL}	Drive Low Delay (Note 1 and 2)	C_{DR} = 1.2nF, V_{IN} ramping down, measured from $V_I = V_{TH(L)}$ to V_{DR} = 200mV T_j = 0 to 85 °C		3	6	µs

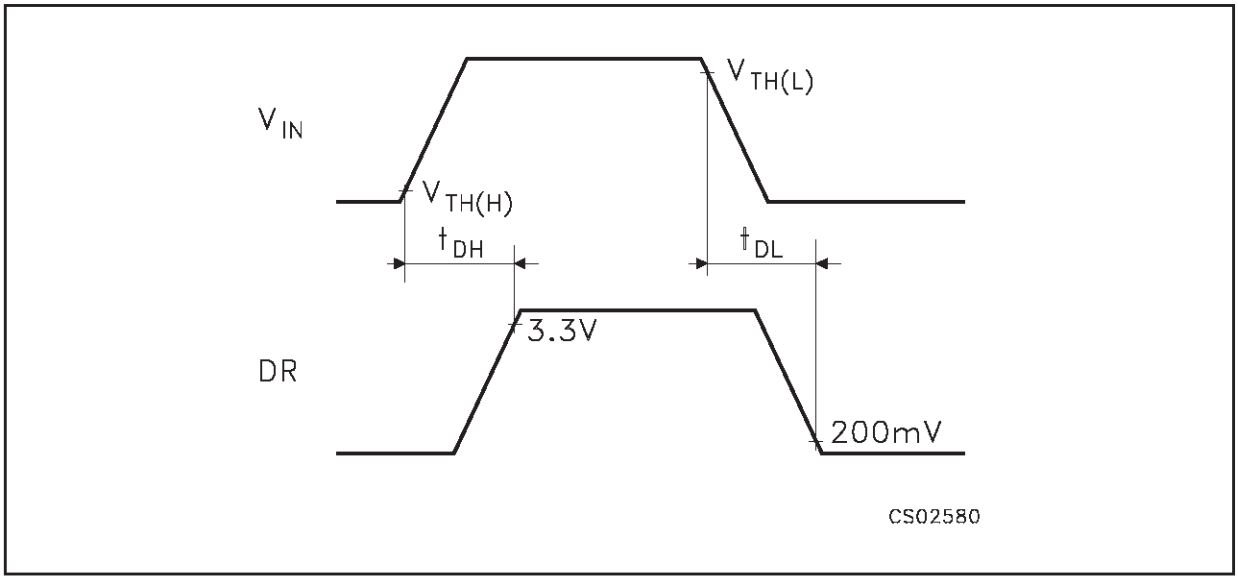
Note 1: Guaranteed by design
Note 2: See timing diagram

5V DETECT THRESHOLDS



V_{IN} rise and fall times (10% to 90%) to be > 100µs

TIMING DIAGRAM



V_{IN} rise and fall times (10% to 90%) to be > 100µs

TYPICAL CHARACTERISTICS (unless otherwise specified T_j = 25°C)

Figure 1 : Supply Current vs Temperature

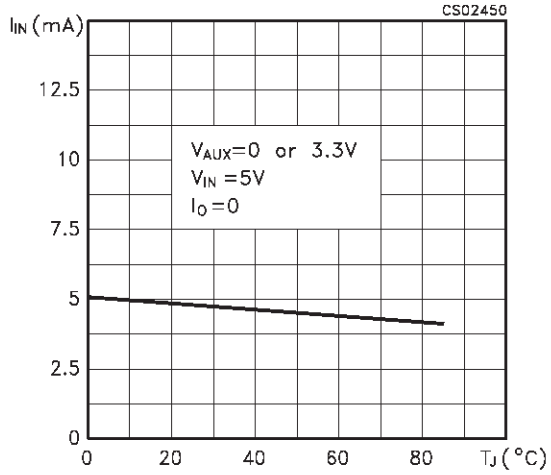


Figure 2 : Aux Current vs Temperature

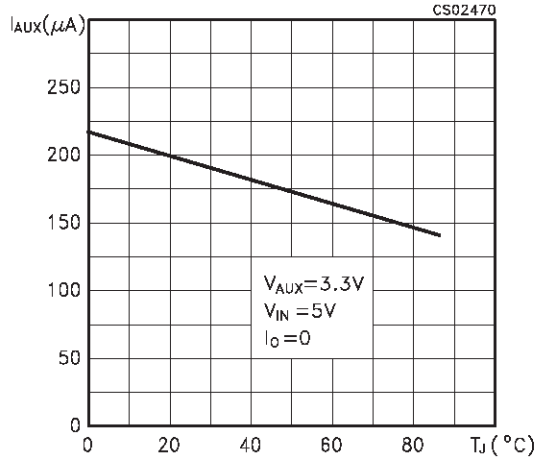


Figure 3 : Drive Current vs Temperature

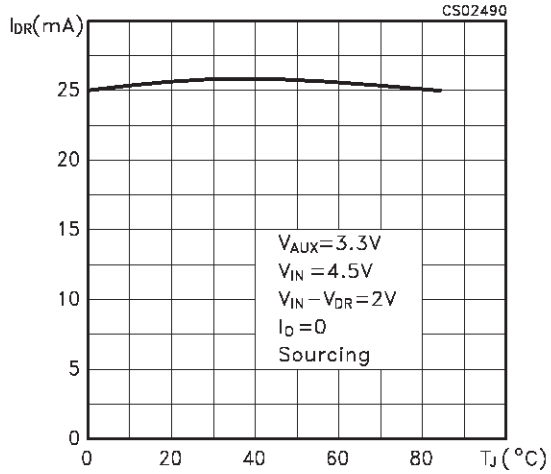


Figure 4 : Aux Current vs Temperature

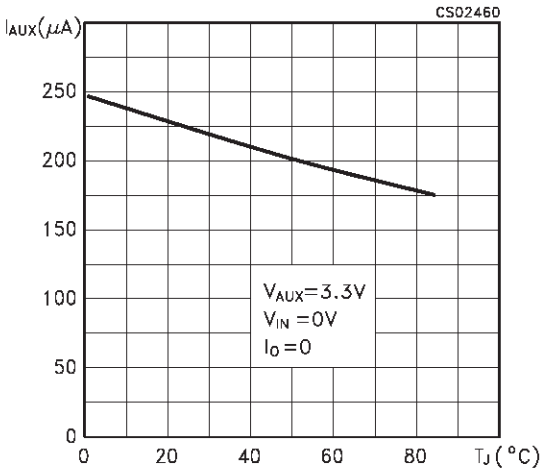


Figure 5 : Drive Output Voltage vs Temperature

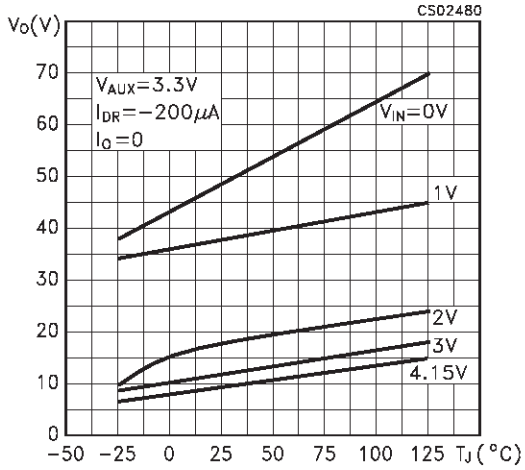


Figure 6 : Drive Current vs V_{IN}-V_{DR}

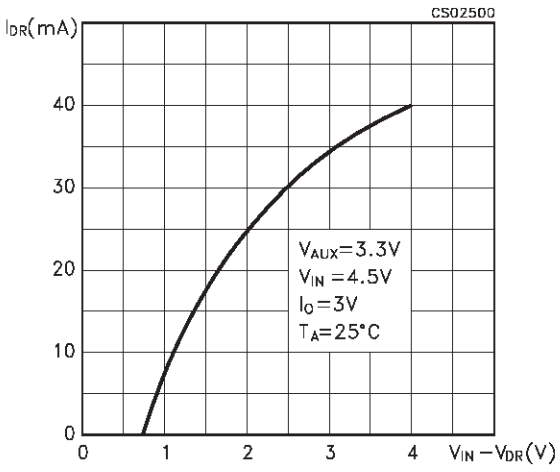


Figure 7 : Drive Current vs Temperature

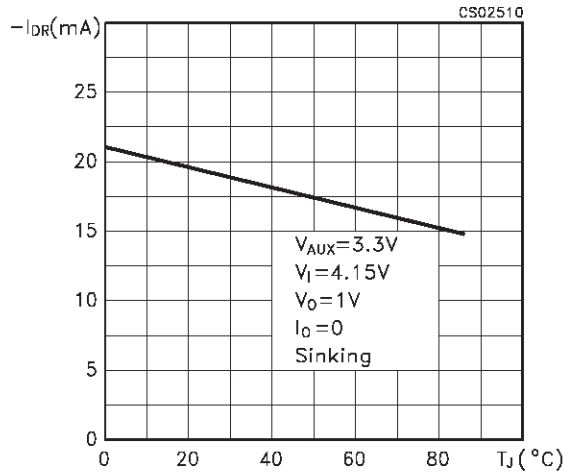


Figure 8 : Line Regulation vs Temperature

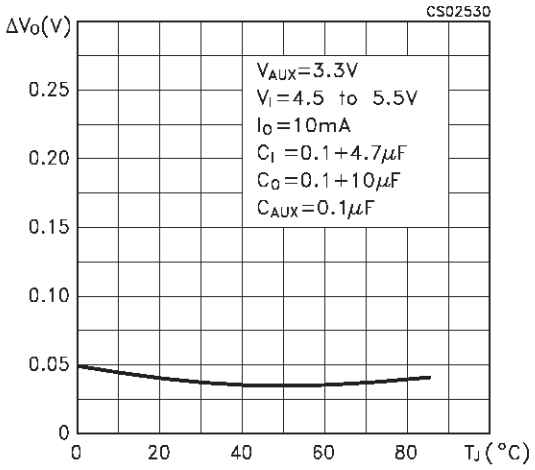


Figure 9 : Output Voltage vs Input Voltage

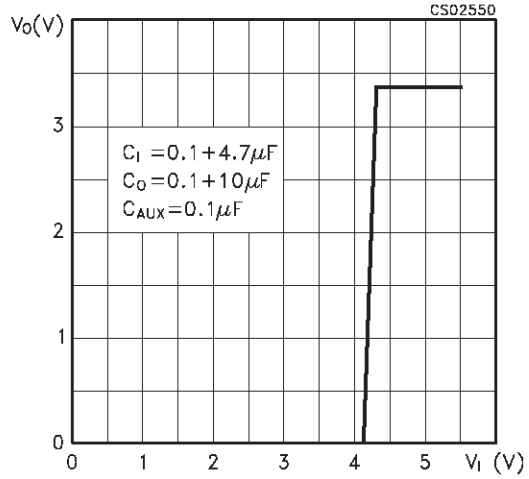


Figure 10 : Output Voltage vs Temperature

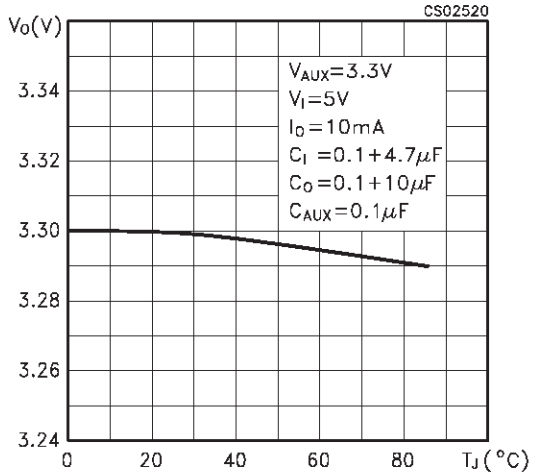


Figure 11 : Load Regulation vs Temperature

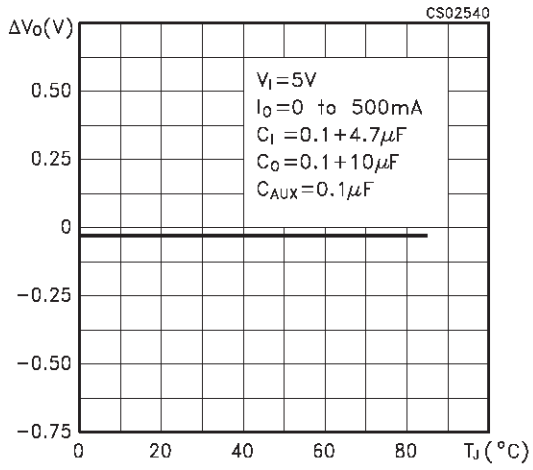


Figure 12 : Threshold Voltage vs Temperature

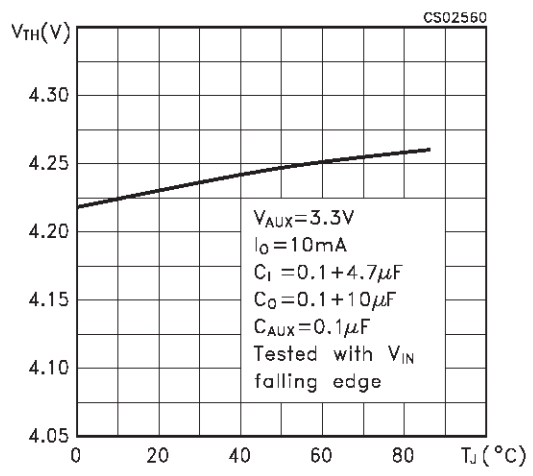


Figure 13 : Hysteresis vs Temperature

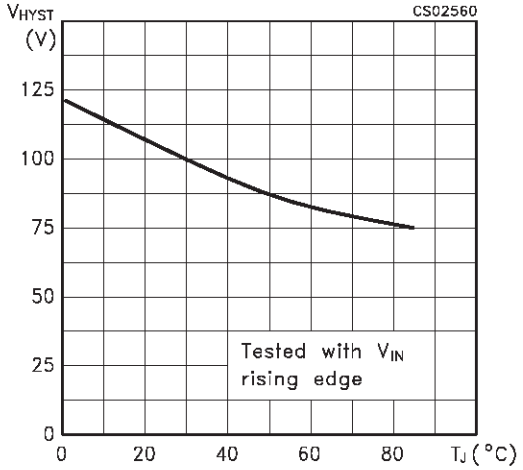
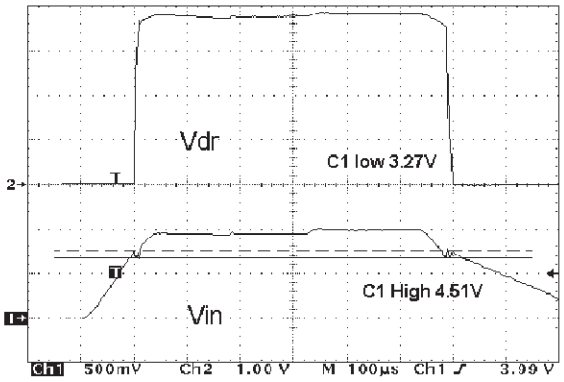
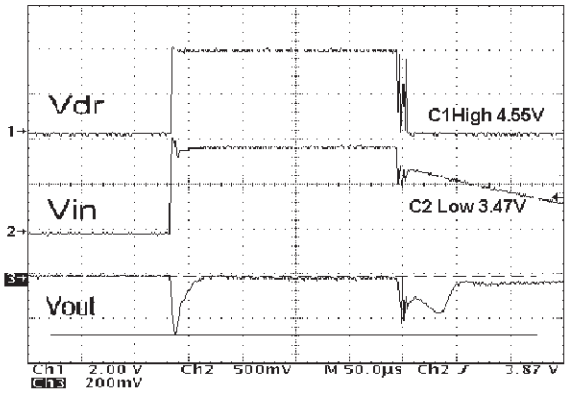


Figure 14 : Threshold



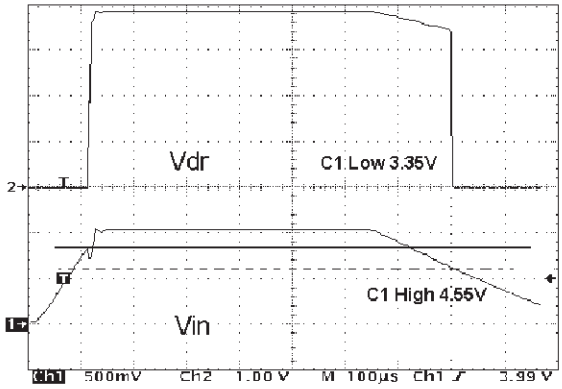
V_I=3.5 to 4.5V, t_s=t_f>100µs, I_O=500mA, C_I=0.1+4.7µF, C_O=33+0.1µF

Figure 15 : Glitch



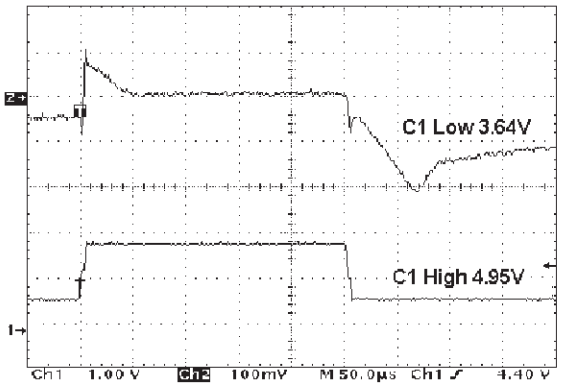
V_I=3.5 to 5V, I_O=500mA, C_O=33+0.1µF, with P-Channel

Figure 16 : Threshold



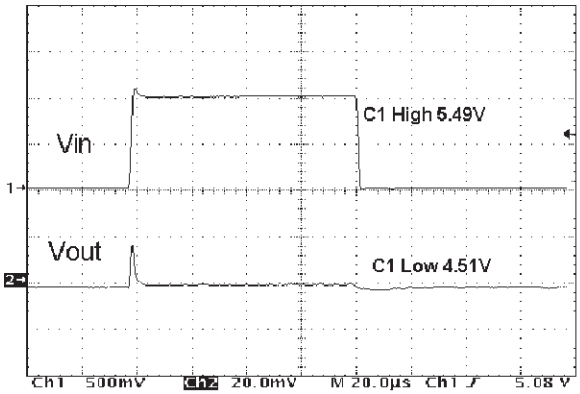
V_I=3.5 to 4.5V, t_s=t_f>100µs, No Load C_I=0.1+4.7µF, C_O=33+0.1µF

Figure 17 : Glitch



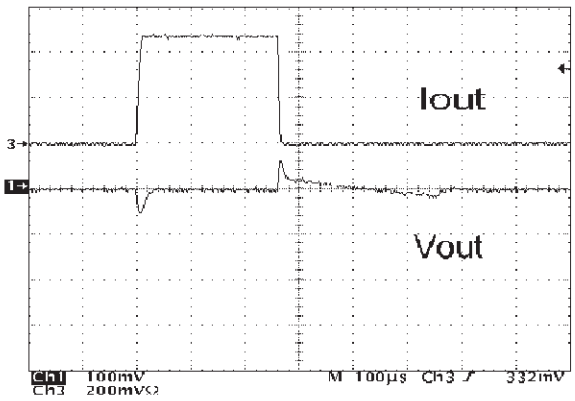
V_I=3.5 to 5V, I_O=500mA, C_O=33+0.1µF, with P-Channel

Figure 18 : Line Transient



V_I=4.5 to 5.5V, I_O=10mA, C_I=0.1+4.7µF, C_O=33+0.1µF, C_{AUX}=0.1µF,

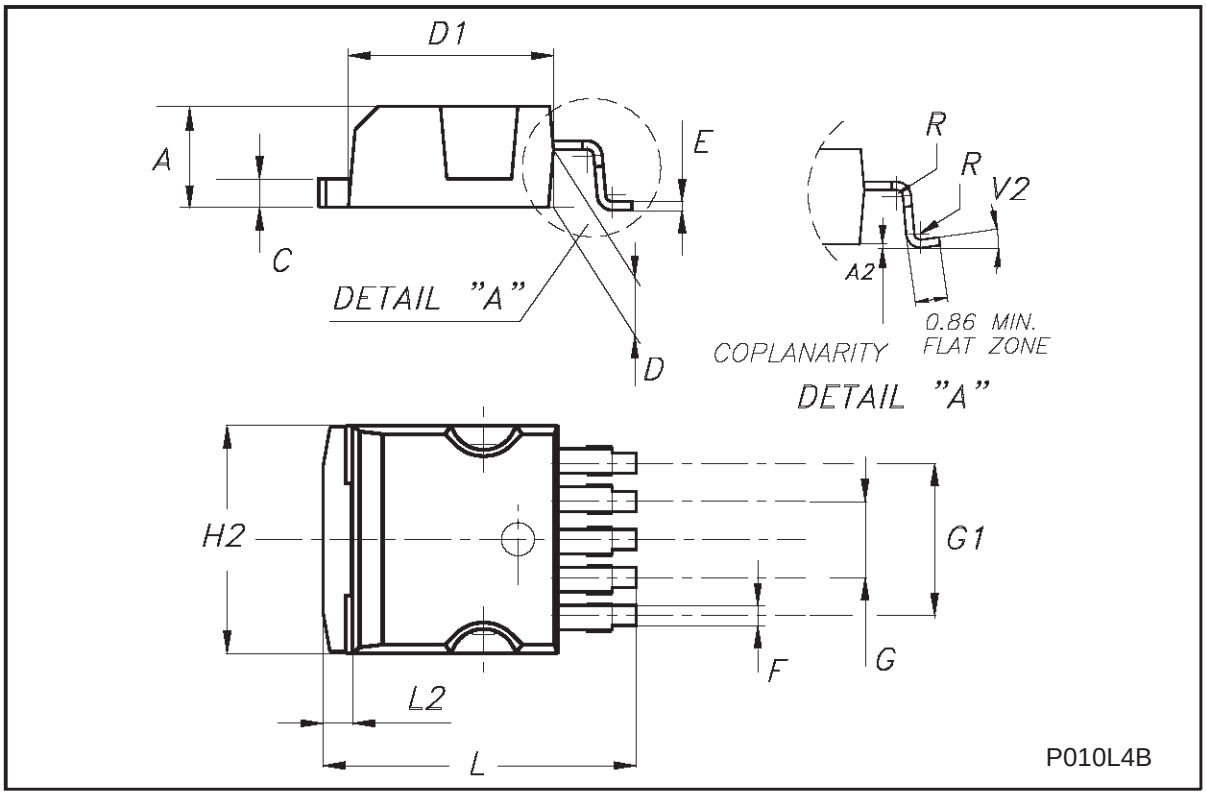
Figure 19 : Load Transient



V_I=5 V, I_O=0 to 500mA, C_I=4.7+0.1µF, C_O=0.1+33µF, C_{AUX}=0.1µF

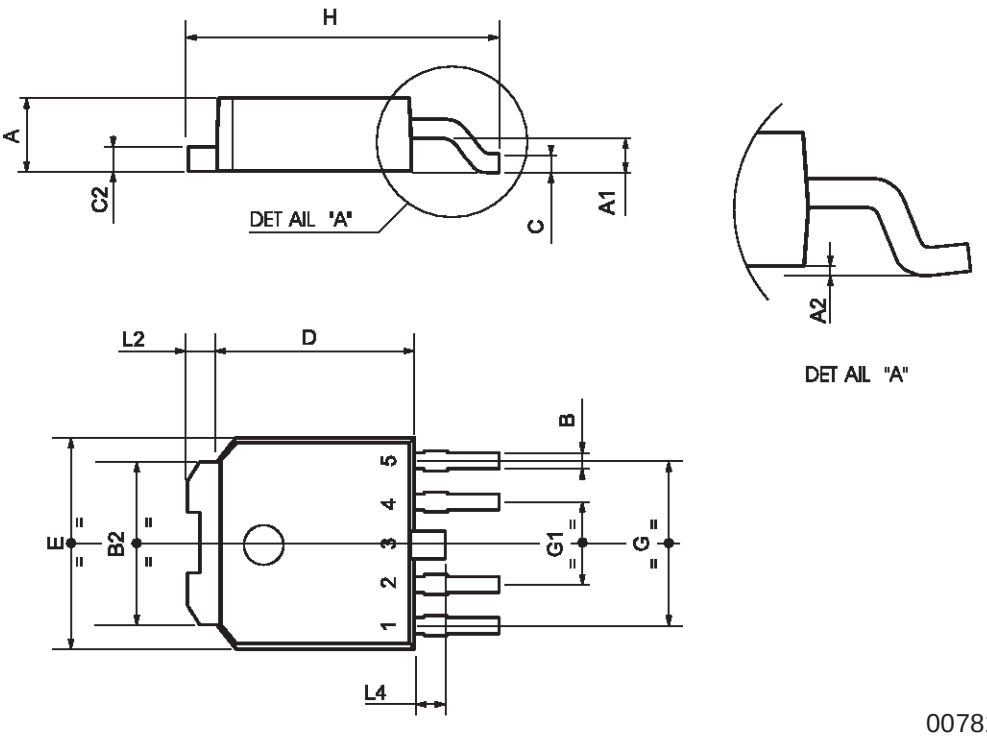
PENTAWATT SMD (P2PAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.30		4.80	0.169		0.188
A2	0.03		0.23	0.001		0.009
C	1.17		1.37	0.046		0.053
D	2.40		2.80	0.094		0.110
D1	8.95		9.35	0.352		0.368
E	0.35		0.55	0.013		0.021
F	0.80		1.05	0.031		0.041
G	3.20		3.60	0.126		0.142
G1	6.60		7.00	0.260		0.275
H2			10.40			0.409
L	13.59		14.39	0.535		0.566
L2	1.27		1.40	0.05		0.055
R		0.30				
V2	0 °		8 °			



PPAK MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.4		0.6	0.015		0.023
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.9		5.25	0.193		0.206
G1	2.38		2.7	0.093		0.106
H	9.35		10.1	0.368		0.397
L2		0.8	1		0.031	0.039
L4	0.6		1	0.023		0.039



0078180/B