



STD35NF06L

N-CHANNEL 60V - 0.014Ω - 35A DPAK

STripFET™ II MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STD35NF06L	60 V	< 0.017 Ω	35 A

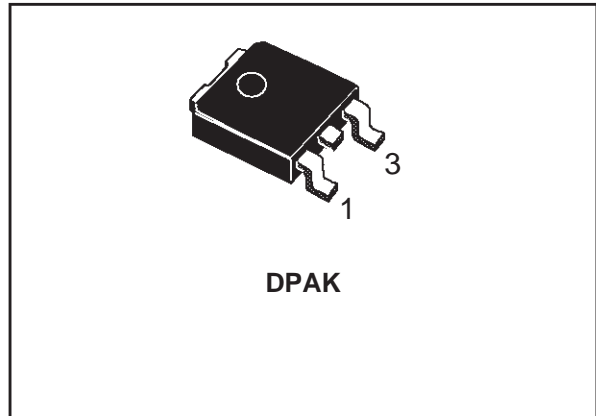
- TYPICAL R_{DS(on)} = 0.014 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED

DESCRIPTION

This Power Mosfet is the latest development of ST-Microelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

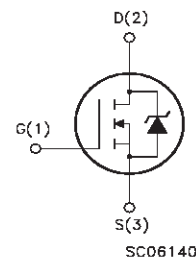
APPLICATIONS

- SOLENOID AND RELAY DRIVERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-AC CONVERTERS
- AUTOMOTIVE ENVIRONMENT



DPAK

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	60	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	60	V
V _{GS}	Gate- source Voltage	± 15	V
I _D	Drain Current (continuous) at T _C = 25°C	35	A
I _D	Drain Current (continuous) at T _C = 100°C	24.5	A
I _{DM} (●)	Drain Current (pulsed)	140	A
P _{TOT}	Total Dissipation at T _C = 25°C	60	W
	Derating Factor	0.4	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	5	V/ns
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(●)Pulse width limited by safe operating area

(1)I_{SD} ≤ 35A, di/dt ≤ 100A/μs, V_{DD} ≤ V(BR)DSS, T_j ≤ T_{JMAX}.

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THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	2.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	100	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	275	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	17.5	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	175	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	60			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 15V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1		2.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 17.5 A V _{GS} = 4.5V, I _D = 17.5 A		0.014 0.016	0.017 0.020	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 17.5 A		18		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		1700		pF
C _{oss}	Output Capacitance			305		pF
C _{rss}	Reverse Transfer Capacitance			105		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 30\text{ V}, I_D = 27.5\text{ A}$ $R_G = 4.7\Omega, V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 3)		20		ns
t_r	Rise Time			100		ns
Q_g	Total Gate Charge	$V_{DD} = 48\text{V}, I_D = 55\text{ A},$ $V_{GS} = 4.5\text{V}$		25	33	nC
Q_{gs}	Gate-Source Charge			5		nC
Q_{gd}	Gate-Drain Charge			10		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 30\text{V}, I_D = 27.5\text{A},$ $R_G = 4.7\Omega, V_{GS} = 4.5\text{V}$ (see test circuit, Figure 3)		40		ns
t_f	Fall Time			20		ns
$t_{d(off)}$	Off-voltage Rise Time	$V_{clamp} = 48\text{V}, I_D = 55\text{A}$ $R_G = 4.7\Omega, V_{GS} = 4.5\text{V}$ (see test circuit, Figure 5)		40		ns
t_f	Fall Time			35		ns
t_c	Cross-over Time			50		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				35	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				140	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 35\text{ A}, V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 35\text{ A}, di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 30\text{V}, T_J = 150^\circ\text{C}$ (see test circuit, Figure 5)		80		ns
Q_{rr}	Reverse Recovery Charge			200		nC
I_{RRM}	Reverse Recovery Current			5		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

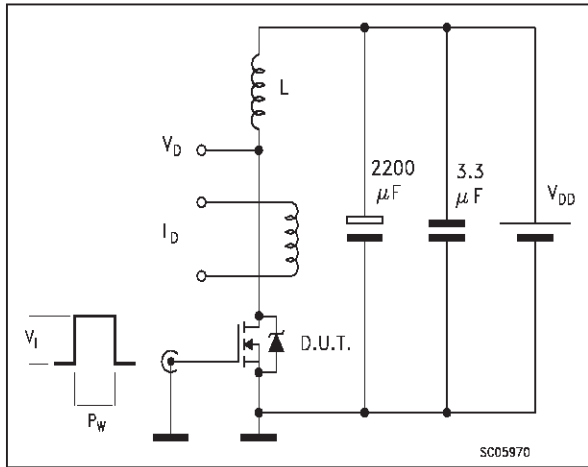


Fig. 2: Unclamped Inductive Waveform

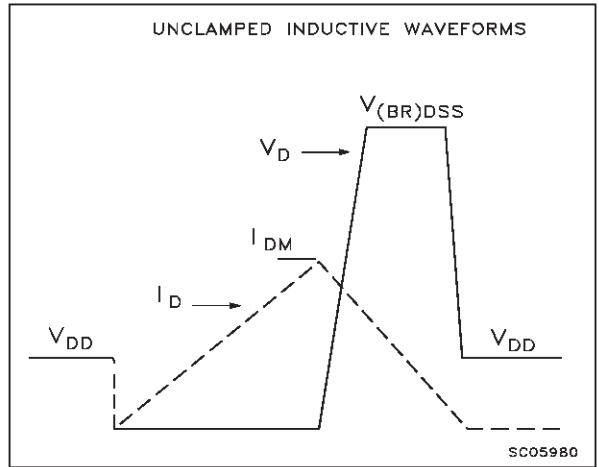


Fig. 3: Switching Times Test Circuit For Resistive Load

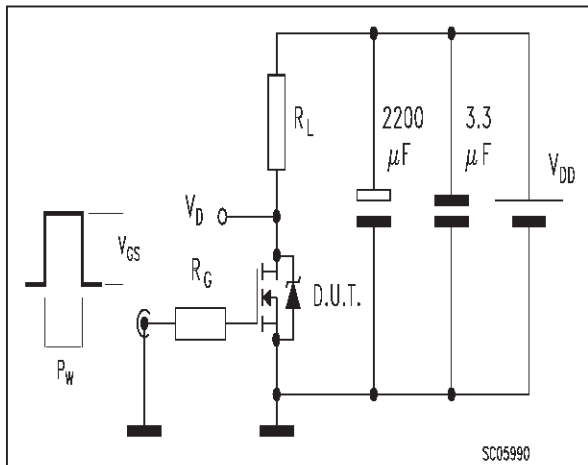


Fig. 4: Gate Charge test Circuit

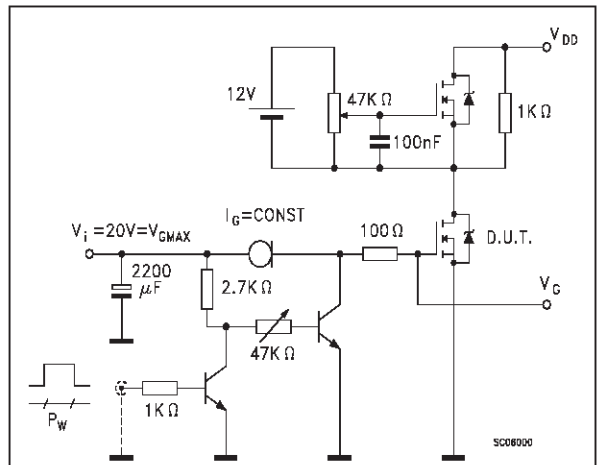
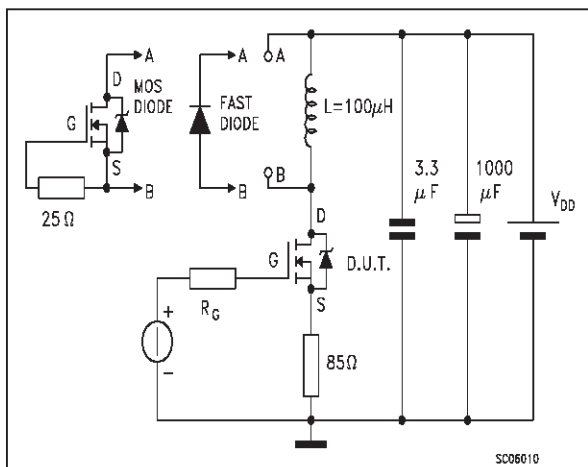
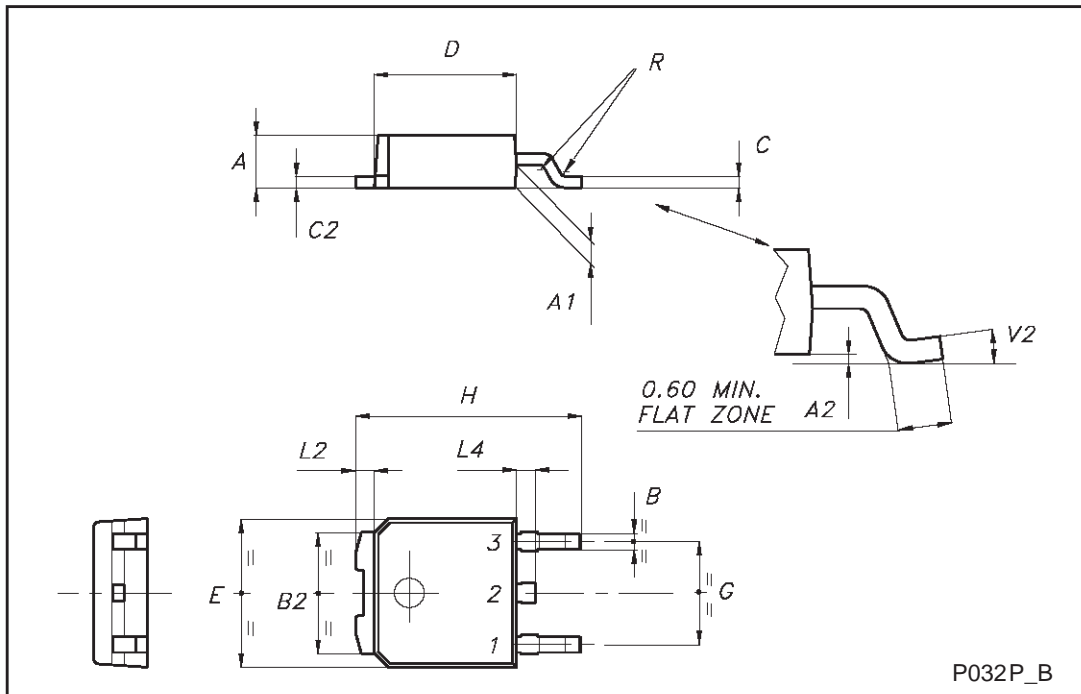


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



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