



STP85NF3LL STB85NF3LL-1

N-CHANNEL 30V - 0.006Ω - 85A TO-220/I²PAK
LOW GATE CHARGE STripFET™ POWER MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP85NF3LL	30 V	< 0.008 Ω	85 A
STB85NF3LL-1	30 V	< 0.008 Ω	85 A

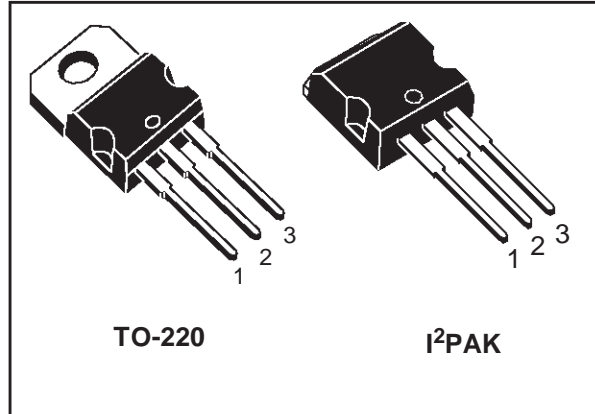
- TYPICAL R_{DS(on)} = 0.0075 Ω (@4.5V)
- OPTIMAL R_{DS(on)} x Q_g TRADE-OFF @4.5V
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED

DESCRIPTION

This application specific Power MOSFET is the third generation of STMicroelectronics unique "Single Feature Size" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

APPLICATIONS

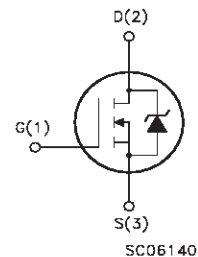
- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS



TO-220

I²PAK

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	30	V
V _{GS}	Gate- source Voltage	± 15	V
I _D	Drain Current (continuous) at T _C = 25°C	85	A
I _D	Drain Current (continuous) at T _C = 100°C	60	A
I _{DM} (●)	Drain Current (pulsed)	340	A
P _{TOT}	Total Dissipation at T _C = 25°C	110	W
	Derating Factor	0.73	W/°C
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(●) Pulse width limited by safe operating area

STP85NF3LL/STB85NF3LL-1

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1.36	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300	°C

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 15V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 40 A V _{GS} = 4.5V, I _D = 40 A		0.006 0.0075	0.008 0.0095	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 40 A		30		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		2210		pF
C _{oss}	Output Capacitance			635		pF
C _{rss}	Reverse Transfer Capacitance			138		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15V, I_D = 30A$		22		ns
t_r	Rise Time	$R_G = 4.7\Omega, V_{GS} = 4.5V$ (see test circuit, Figure 3)		130		ns
Q_g	Total Gate Charge	$V_{DD} = 24V, I_D = 60A,$		30	40	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 4.5V$		9		nC
Q_{gd}	Gate-Drain Charge			12.5		nC

SWITCHING OFF

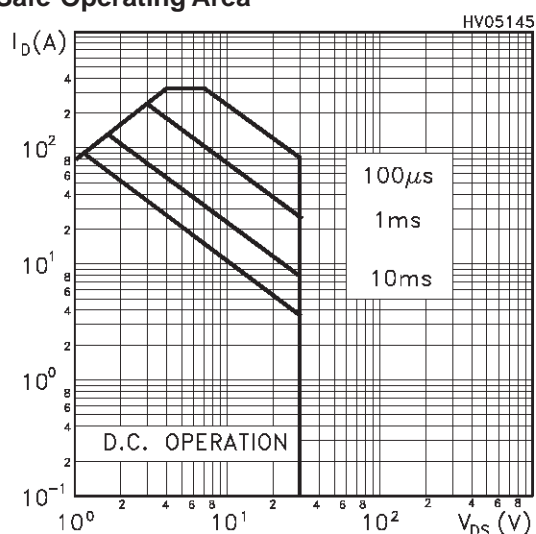
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 15V, I_D = 30A,$		36.5		ns
t_f	Fall Time	$R_G = 4.7\Omega, V_{GS} = 4.5V$ (see test circuit, Figure 3)		36.5		ns
$t_{d(off)}$	Off-voltage Rise Time	$V_{clamp} = 24V, I_D = 30A$		32		ns
t_f	Fall Time	$R_G = 4.7\Omega, V_{GS} = 4.5V$		23		ns
t_c	Cross-over Time	(see test circuit, Figure 5)		40		ns

SOURCE DRAIN DIODE

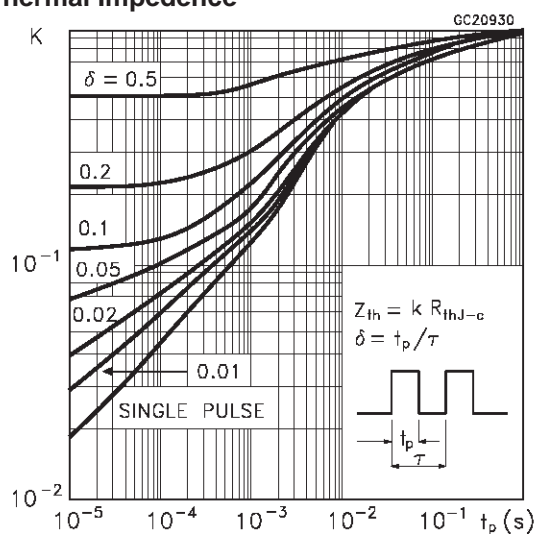
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				85	A
$I_{SDM(1)}$	Source-drain Current (pulsed)				340	A
$V_{SD(2)}$	Forward On Voltage	$I_{SD} = 85A, V_{GS} = 0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 85A, di/dt = 100A/\mu s,$		65		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 15V, T_j = 150^\circ C$		105		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		3.4		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

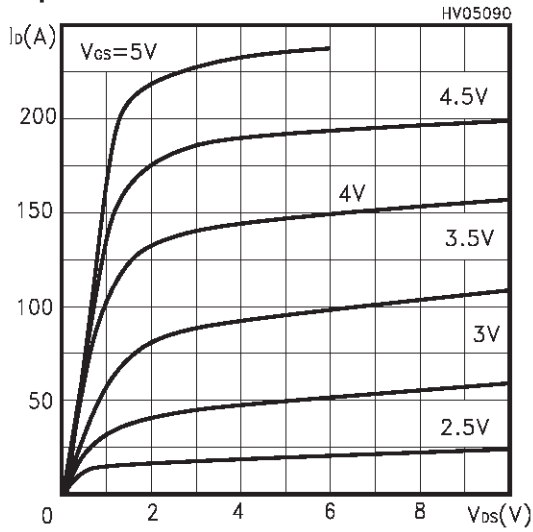
Safe Operating Area



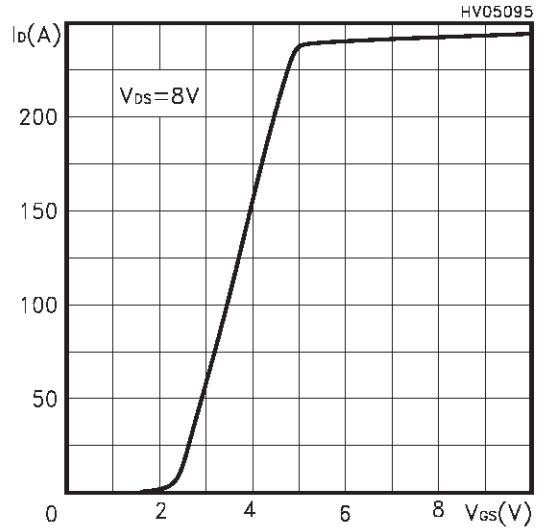
Thermal Impedence



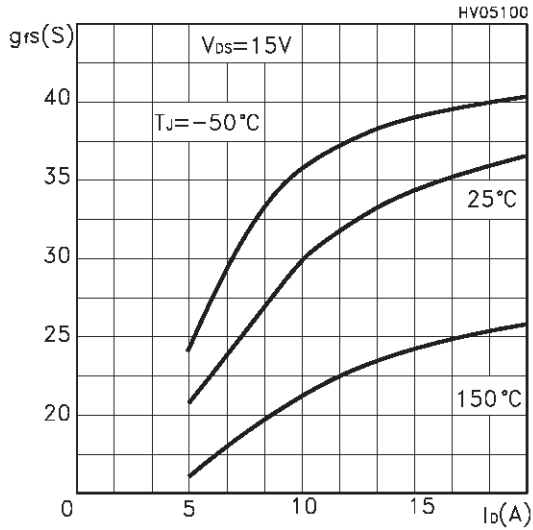
Output Characteristics



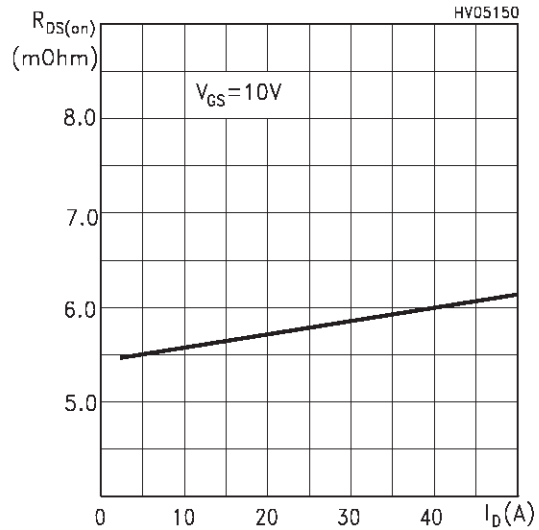
Transfer Characteristics



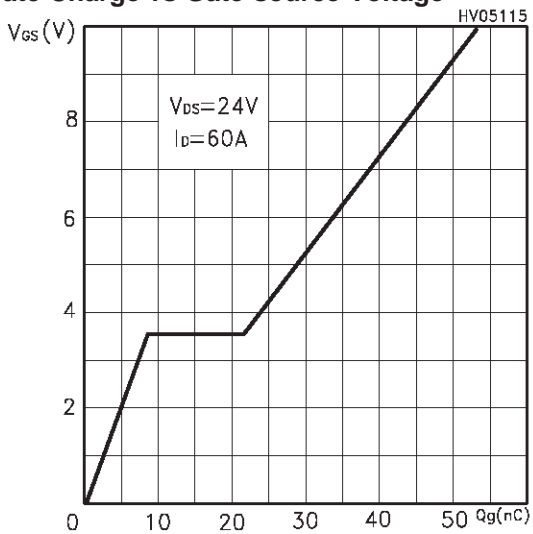
Transconductance



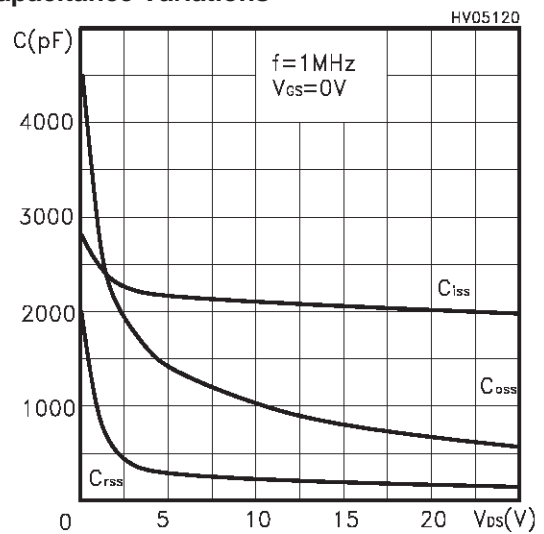
Static Drain-source On Resistance



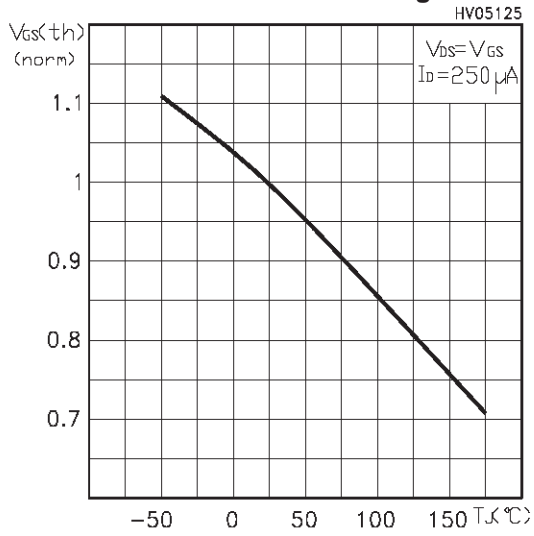
Gate Charge vs Gate-source Voltage



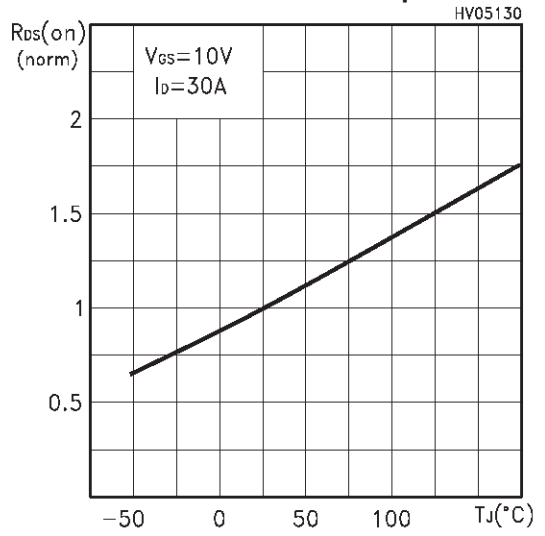
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

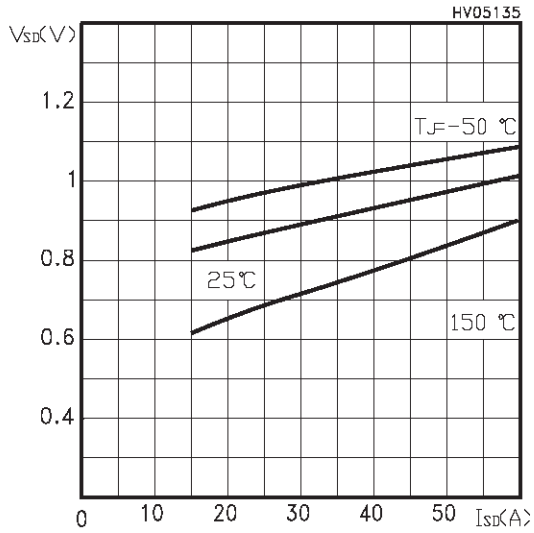


Fig. 1: Unclamped Inductive Load Test Circuit

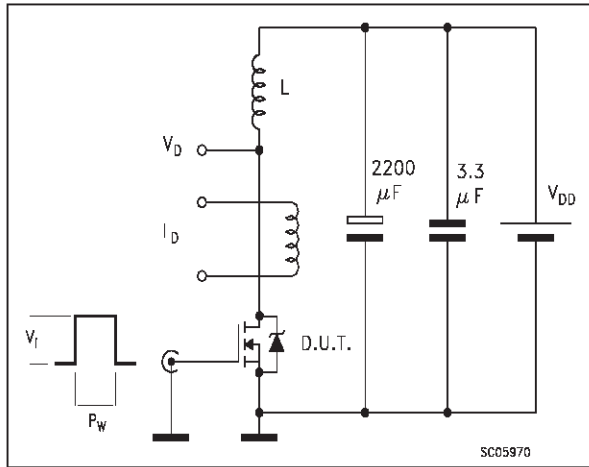


Fig. 2: Unclamped Inductive Waveform

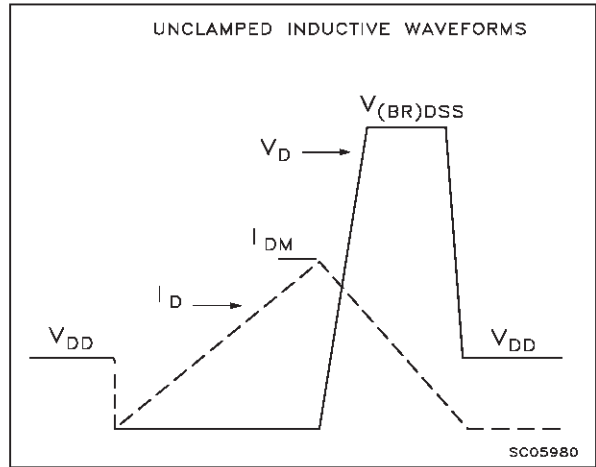


Fig. 3: Switching Times Test Circuit For Resistive Load

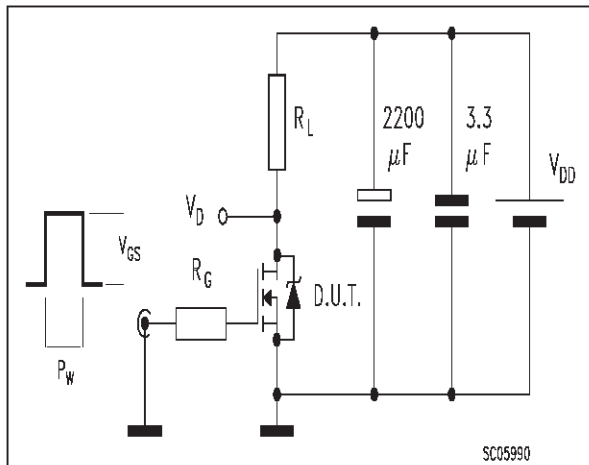


Fig. 4: Gate Charge test Circuit

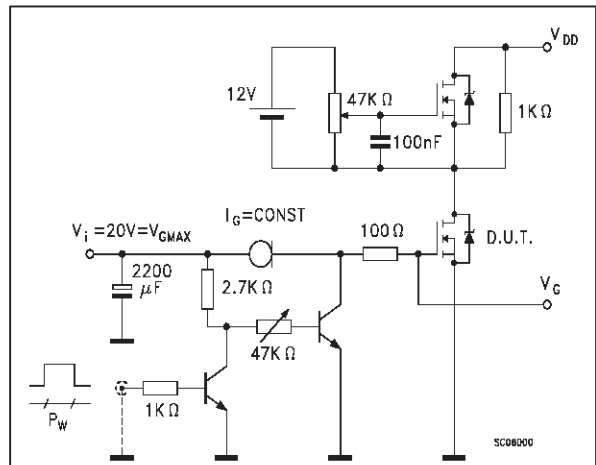
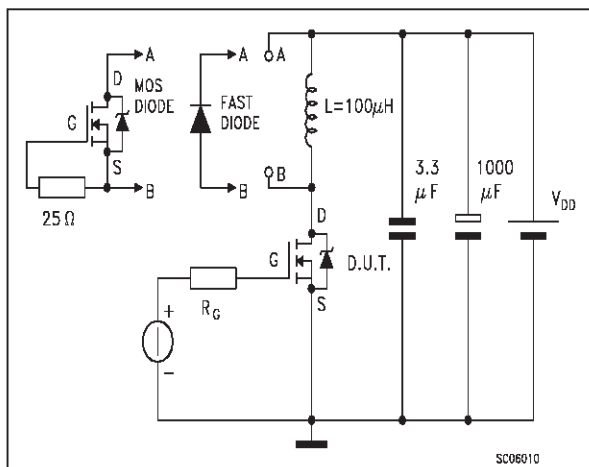
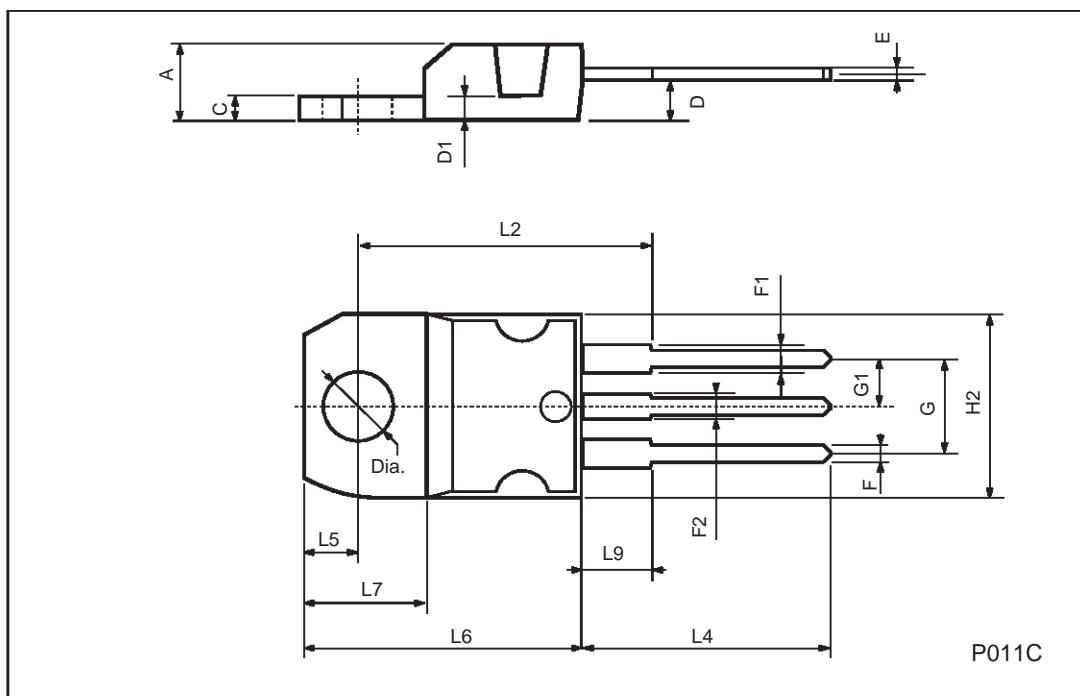


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



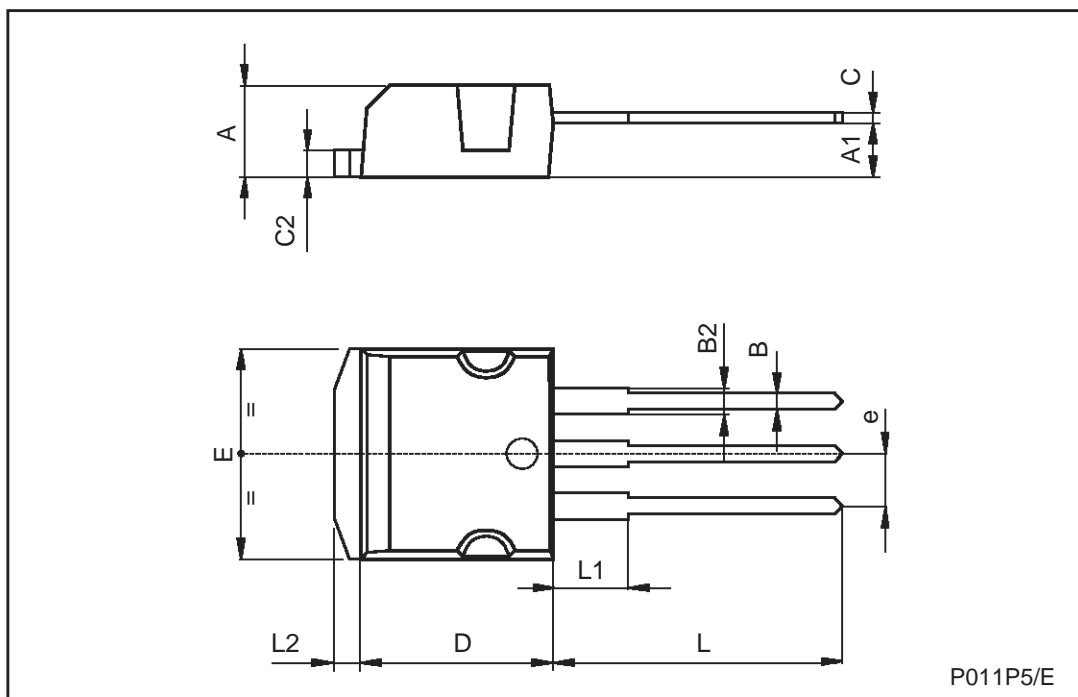
TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



TO-262 (I²PAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
e	2.4		2.7	0.094		0.106
E	10		10.4	0.393		0.409
L	13.1		13.6	0.515		0.531
L1	3.48		3.78	0.137		0.149
L2	1.27		1.4	0.050		0.055



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