



## 10/100 BASE-TX/FX 8 PORT TRANSCEIVER

PRODUCT PREVIEW

### 1.0 DESCRIPTION

The STE800P is a high performance Octal Fast Ethernet physical layer interface for 10BASE-T and 100BASE-TX/ FX applications.

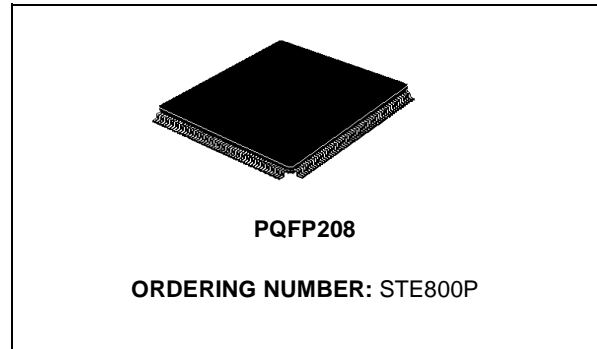
It was designed with advanced CMOS technology to provide a RMII/SMII for easy attachment to 10/100 Media Access Controllers (MAC) and a physical media interface for 100BASE-TX / FX of IEEE802.3u and 10BASE-T of IEEE802.3.

The STE800P supports both half-duplex and full-duplex operation, at 10 and 100 Mbps operation. Its operating mode can be set using auto-negotiation, parallel detection or manual control. It also allows for the support of auto-negotiation functions for speed and duplex detection.

### 2.0 FEATURE

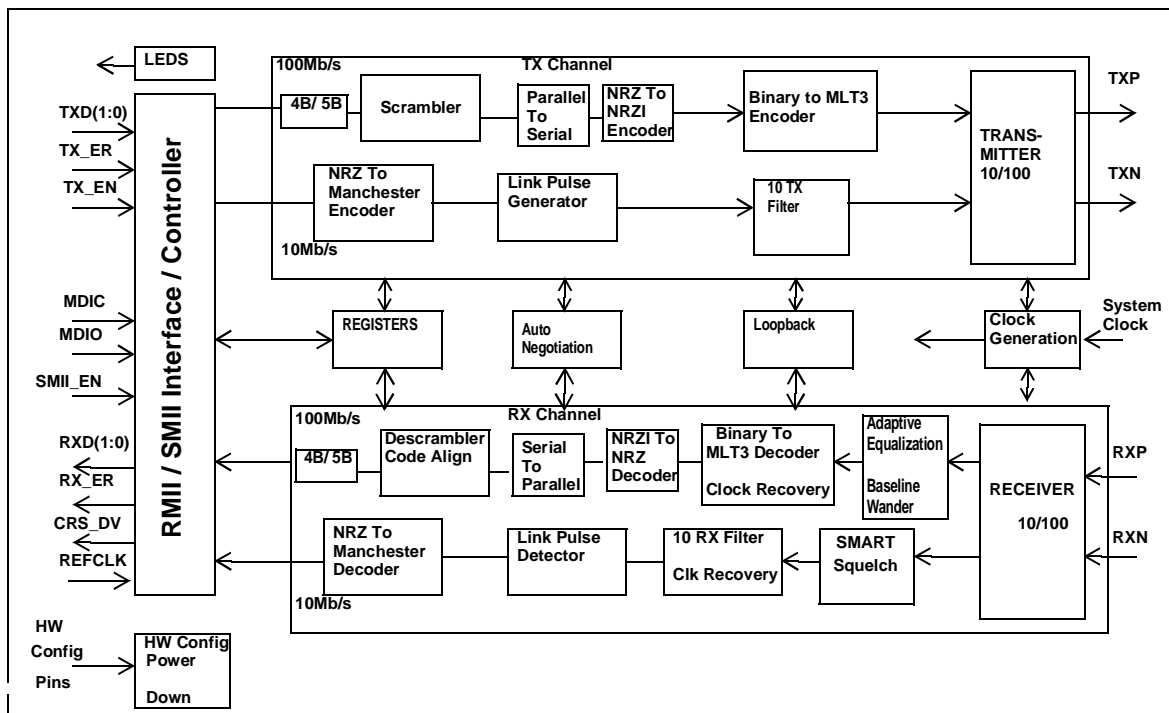
#### 2.1 Industry standard

- IEEE802.3u 100BASE-TX/FX and IEEE802.3 10BASE-T compliant



- Support for IEEE802.3x flow control
- IEEE802.3u Auto-Negotiation support
- RMII/SMII interface
- Low power, single supply 3.3V CMOS
- Shared MII management interface up to 25 Mbps

Figure 1. BLOCK DIAGRAM FOR 1 PORT



**2.2 Physical Layer**

- Integrates the whole Physical layer functions for
  - 100BASE-TX full or half duplex Ethernet on CAT 5 twisted pair cable
  - 100BASE-FX full or half duplex transmission over fiber optic cabling
  - 10BASE-T full or half duplex Ethernet on CAT 3, 4 or 5 cable.
- Auto-negotiation(NWAY) function of full/half duplex operation for both 10 and 100 Mbps
- MLT-3 transceiver with DC restoration for Base-line wander compensation
- Transmit wave-shaper, receive filters, and adaptive equalizer
- Loop-back modes for diagnostic
- In Stream Cipher Scrambler/ De-scrambler
- 4B/5B, MLT3, NRZI and Manchester encoding/decoding
- 125 MHz clock generator and timing recovery
- Supports external transmit transformer with turn ratio 1.41 : 1
- Supports external receive transformer with turn ratio 1:1

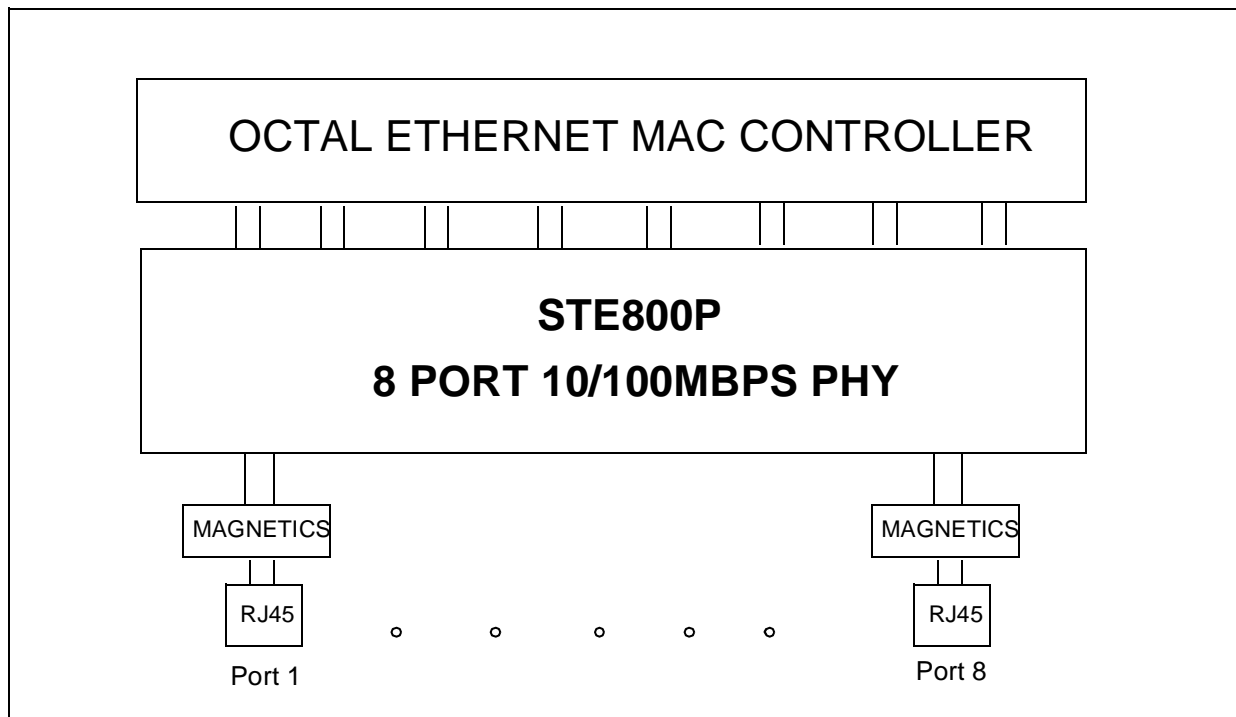
**2.3 LED Display**

- Serial LED status pins
- Programmable parallel LED pins

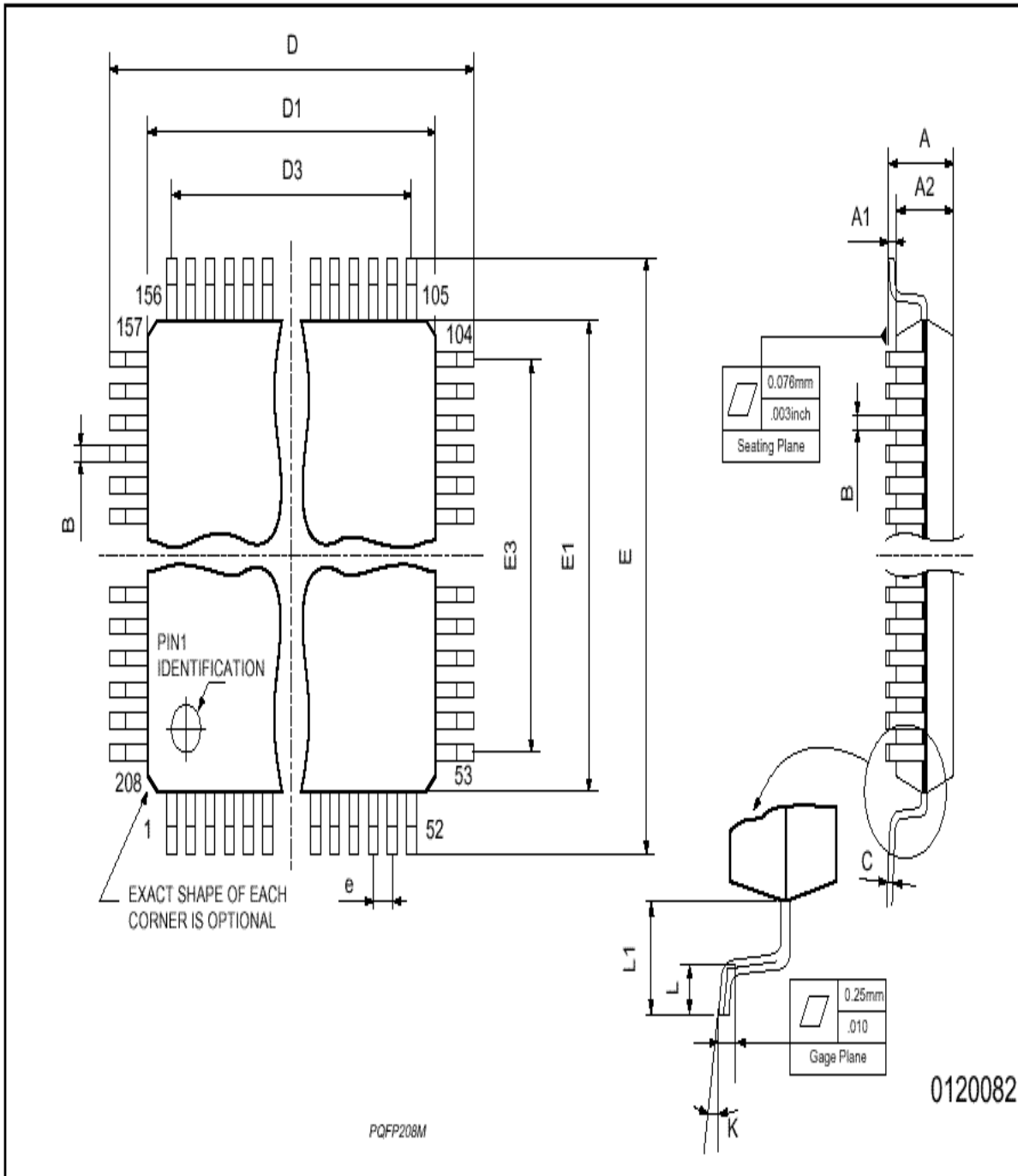
**2.4 Miscellaneous**

- Standard 208-pin PQFP package pinout

**Figure 2. System Diagram of the STE800P Application**



3.0 PACKAGE



**PACKAGE TYPE: PQFP 208 / BODY 28X28X3.49mm**

REF	Dimensions mm			Dimensions inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX
A			4.10			0.161
A1	0.25			0.010		
A2	3.40	3.20	3.60	0.134	0.126	0.142
B	0.17		0.27	0.007		0.011
C	0.09		0.20	0.003		0.008
D		30.60			1.205	
D1		28.00			1.102	
D3		25.50			1.004	
e		0.50			0.020	
E		30.60			1.205	
E1		28.00			1.102	
E3		25.50			1.004	
L	0.45	0.60	0.75	0.018	0.024	0.029
L1		1.30			0.51	
K	0 deg. (min), 3.5 deg. (typ.), 7 deg.(max)					

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics  
© 2001 STMicroelectronics - All Rights Reserved

STMicroelectronics GROUP OF COMPANIES  
Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain  
- Sweden - Switzerland - United Kingdom - U.S.A.  
<http://www.st.com>