

## 5V or 3V NVRAM SUPERVISOR FOR LPSRAM

### FEATURES SUMMARY

- CONVERT LOW POWER SRAMs INTO NVRAMs
- 5V OR 3V OPERATING VOLTAGE
- PRECISION POWER MONITORING and POWER SWITCHING CIRCUITRY
- AUTOMATIC WRITE-PROTECTION WHEN  $V_{CC}$  IS OUT-OF-TOLERANCE
- CHOICE OF SUPPLY VOLTAGES and POWER-FAIL DESELECT VOLTAGES:
  - M40SZ100Y:  $V_{CC} = 4.5$  to  $5.5V$ ;  
 $4.20V \leq V_{PFD} \leq 4.50V$
  - M40SZ100W:  $V_{CC} = 2.7$  to  $3.6V$ ;  
 $2.55V \leq V_{PFD} \leq 2.70V$
- RESET OUTPUT ( $\overline{RST}$ ) FOR POWER ON RESET
- 1.25V REFERENCE (for  $PFI/\overline{PFO}$ )
- LESS THAN 10ns CHIP ENABLE ACCESS PROPAGATION DELAY (at 5V)
- OPTIONAL PACKAGING INCLUDES A 28-LEAD SOIC and SNAPHAT® TOP (to be ordered separately)
- 28-LEAD SOIC PACKAGE PROVIDES DIRECT CONNECTION FOR A SNAPHAT TOP WHICH CONTAINS THE BATTERY
- BATTERY LOW PIN ( $\overline{BL}$ )

Figure 1. 16-pin SOIC Package

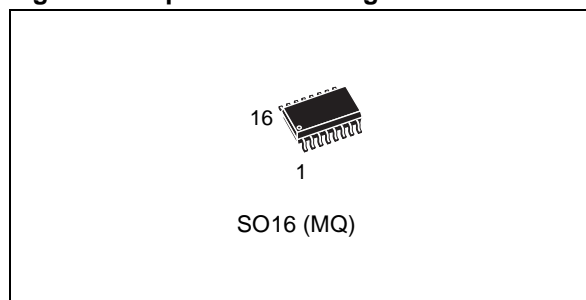
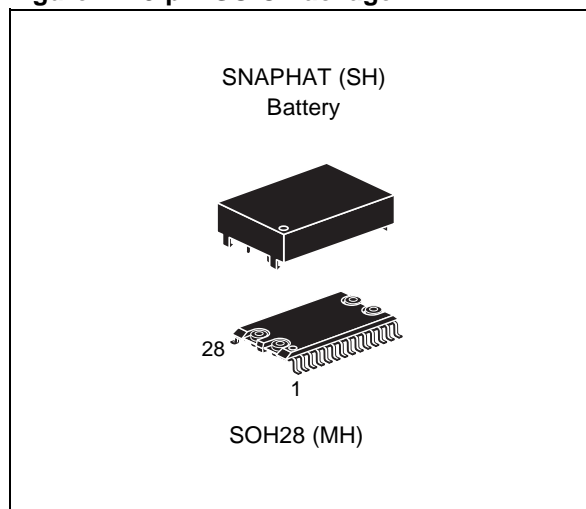


Figure 2. 28-pin SOIC Package\*



\* Contact Local Sales Office

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## SUMMARY DESCRIPTION

The M40SZ100Y/W NVRAM Controller is a self-contained device which converts a standard low-power SRAM into a non-volatile memory. A precision voltage reference and comparator monitors the  $V_{CC}$  input for an out-of-tolerance condition.

When an invalid  $V_{CC}$  condition occurs, the conditioned chip enable output ( $\overline{E}_{CON}$ ) is forced inactive to write protect the stored data in the SRAM. During a power failure, the SRAM is switched from the  $V_{CC}$  pin to the lithium cell within the SNAPHAT (or external battery for the 16-lead SOIC) to provide the energy required for data retention. On a subsequent power-up, the SRAM remains write protected until a valid power condition returns.

The 28-pin, 330 mil SOIC provides sockets with gold plated contacts for direct connection to a separate SNAPHAT<sup>®</sup> housing containing the battery. The SNAPHAT housing has gold plated pins which mate with the sockets, ensuring reliable connection. The housing is keyed to prevent improper insertion. This unique design allows the SNAPHAT battery package to be mounted on top

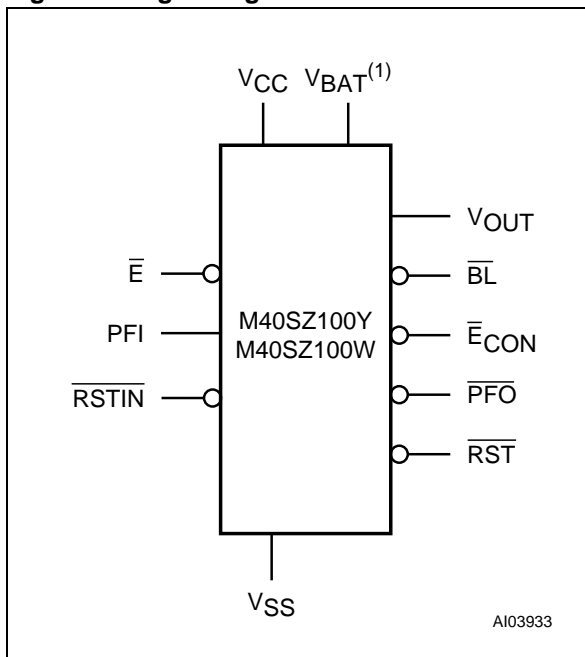
of the SOIC package after the completion of the surface mount process which greatly reduces the board manufacturing process complexity of either directly soldering or inserting a battery into a soldered holder. Providing non-volatility becomes a "SNAP." This feature is also available in the "top-less" 16-pin SOIC package (MQ).

Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is also keyed to prevent reverse insertion.

The 28-pin SOIC and battery packages are shipped separately in plastic anti-static tubes or in Tape & Reel form. For the 28-lead SOIC, the battery/crystal package (e.g., SNAPHAT) part number is "M4ZXX-BR00SH" (see Table 13, page 17).

**Caution:** Do not place the SNAPHAT battery top in conductive foam, as this will drain the lithium button-cell battery.

Figure 3. Logic Diagram



Note: 1. For 16-pin SOIC package only.

Table 1. Signal Names

$\overline{E}$	Chip Enable Input
$\overline{E}_{CON}$	Conditioned Chip Enable Output
$\overline{RST}$	Reset Output (Open Drain)
$\overline{RSTIN}$	Reset Input
$\overline{BL}$	Battery Low Output (Open Drain)
$V_{OUT}$	Supply Voltage Output
$V_{CC}$	Supply Voltage
$V_{BAT}^{(1)}$	Back-up Supply Voltage
PFI	Power Fail Input
$\overline{PFO}$	Power Fail Output
$V_{SS}$	Ground
NC	Not Connected Internally

Note: 1. For SO16 only.

Figure 4. SOIC16 Connections

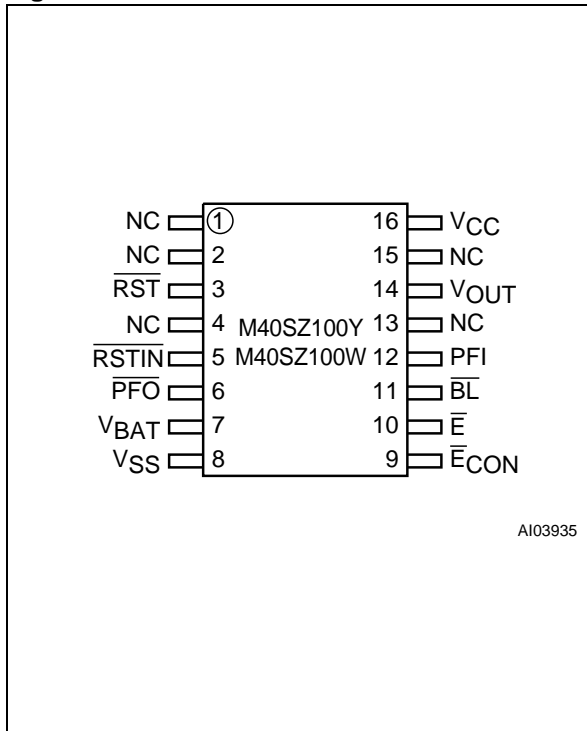
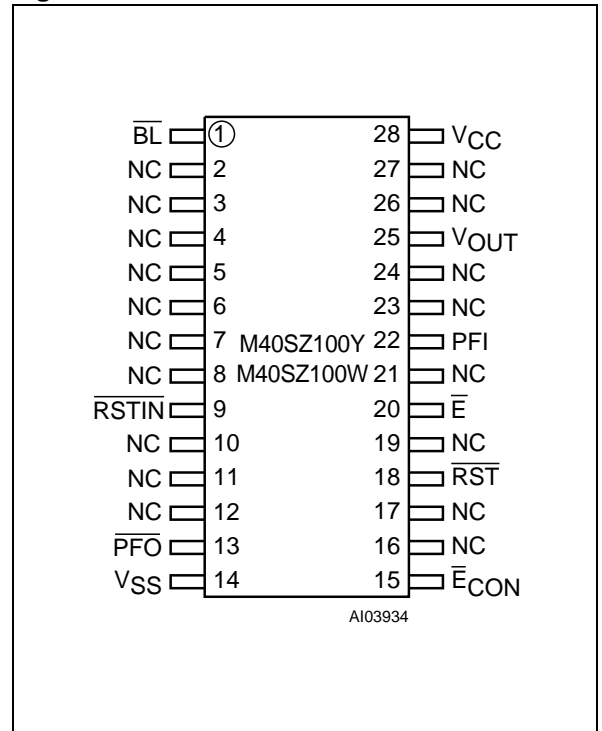
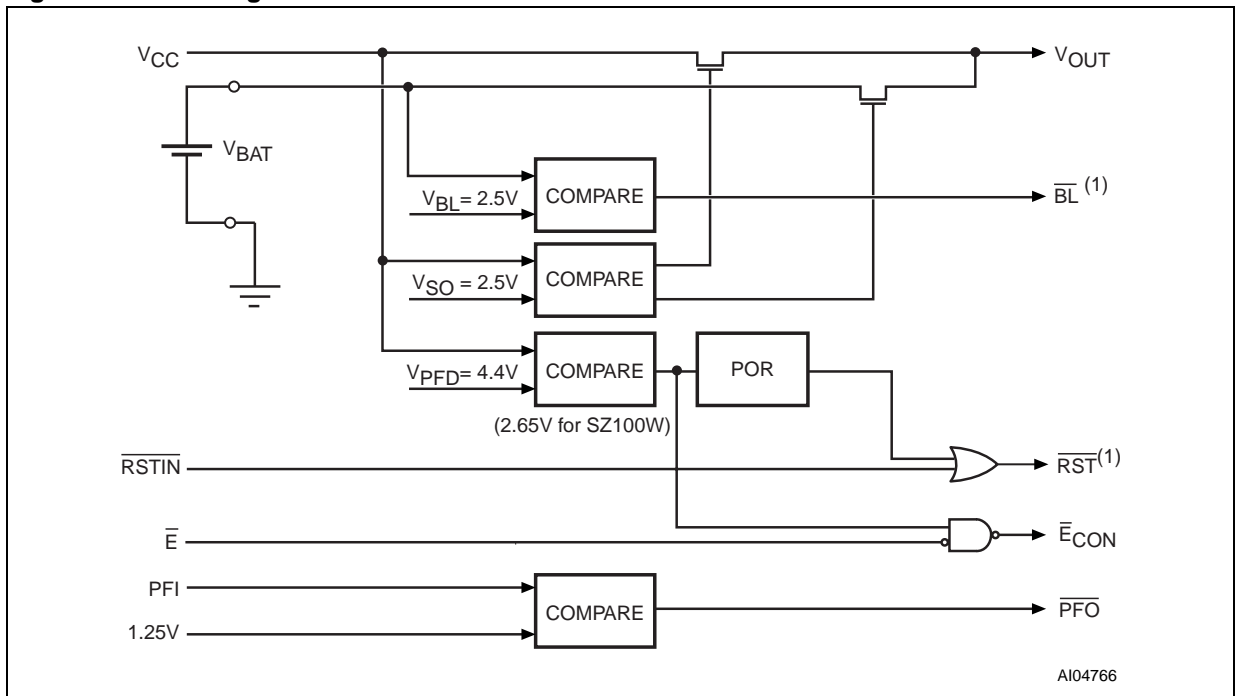


Figure 5. SOIC28 Connections



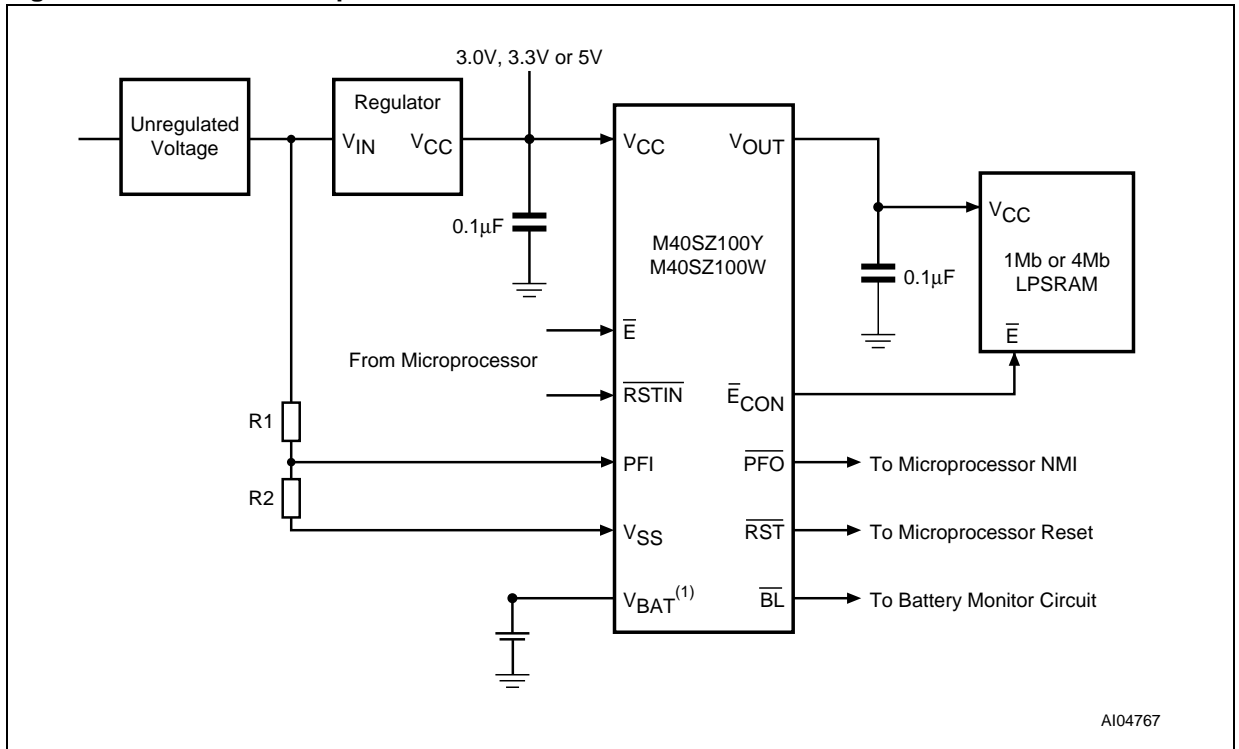
Note: 1. DU = Do Not Use

Figure 6. Block Diagram



Note: Open drain output

Figure 7. Hardware Hookup



Note: 1. User supplied for the 16-pin package

**MAXIMUM RATING**

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is

not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T <sub>STG</sub>	Storage Temperature (V <sub>CC</sub> Off)	SNAPHAT	-40 to 85	°C
		SOIC	-55 to 125	°C
T <sub>S<sub>LD</sub></sub> <sup>(1)</sup>	Lead Solder Temperature for 10 seconds		260	°C
V <sub>IO</sub>	Input or Output Voltages		-0.3 to V <sub>CC</sub> +0.3	V
V <sub>CC</sub>	Supply Voltage	M40SZ100Y	-0.3 to 7	V
		M40SZ100W	-0.3 to 4.6	V
I <sub>O</sub>	Output Current		20	mA
P <sub>D</sub>	Power Dissipation		1	W

Note: 1. Reflow at peak temperature of 215°C to 225°C for < 60 seconds (total thermal budget not to exceed 180°C for between 90 to 120 seconds).

**CAUTION:** Negative undershoots below -0.3V are not allowed on any pin while in the Battery Back-up mode.  
**CAUTION:** Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.

**DC AND AC PARAMETERS**

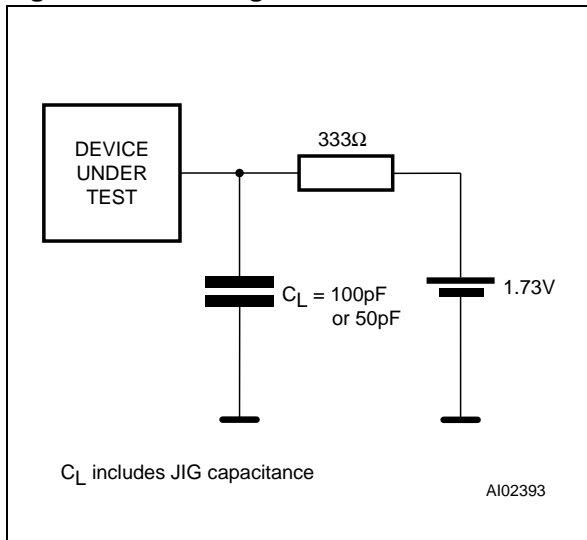
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measure-

ment Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

**Table 3. DC and AC Measurement Conditions**

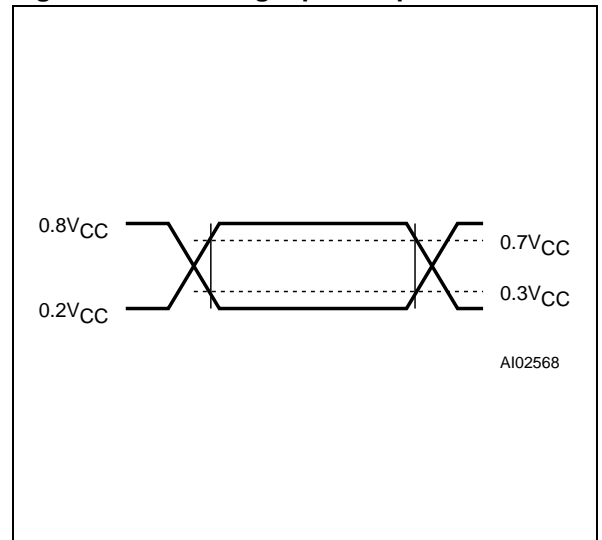
Parameter	M40SZ100Y	M40SZ100W
V <sub>CC</sub> Supply Voltage	4.5 to 5.5V	2.7 to 3.6V
Ambient Operating Temperature	-40 to 85°C	-40 to 85°C
Load Capacitance (C <sub>L</sub> )	100pF	50pF
Input Rise and Fall Times	≤ 5ns	≤ 5ns
Input Pulse Voltages	0.2 to 0.8V <sub>CC</sub>	0.2 to 0.8V <sub>CC</sub>
Input and Output Timing Ref. Voltages	0.3 to 0.7V <sub>CC</sub>	0.3 to 0.7V <sub>CC</sub>

**Figure 8. AC Testing Load Circuit**



Note: 1. CL = 100pF for M40SZ100Y and 50pF for M40SZ100W.

**Figure 9. AC Testing Input/Output Waveforms**



**Table 4. Capacitance**

Symbol	Parameter <sup>(1,2)</sup>	Min	Max	Unit
C <sub>IN</sub>	Input Capacitance		7	pF
C <sub>OUT</sub> <sup>(3)</sup>	Output Capacitance		10	pF

Note: 1. Sampled only, not 100% tested.  
 2. At 25°C, f = 1MHz.  
 3. Outputs deselected

Table 5. DC Characteristics

Sym	Parameter	Test Condition <sup>(1)</sup>	M40SZ100Y			M40SZ100W			Unit
			Min	Typ	Max	Min	Typ	Max	
I <sub>CC</sub>	Supply Current	Outputs open			1			0.5	mA
I <sub>CCDR</sub>	Data Retention Mode Current <sup>(2)</sup>			50	200		50	200	nA
I <sub>LI</sub> <sup>(3)</sup>	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$			±1			±1	µA
	Input Leakage Current (PFI)		-25	2	25	-25	2	25	nA
I <sub>LO</sub> <sup>(4)</sup>	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$			±1			±1	µA
I <sub>OUT1</sub> <sup>(5)</sup>	V <sub>OUT</sub> Current (Active)	$V_{OUT} > V_{CC} - 0.3$			175			100	mA
I <sub>OUT2</sub>	V <sub>OUT</sub> Current (Battery Back-up)	$V_{OUT} > V_{BAT} - 0.3$			100			100	µA
V <sub>BAT</sub>	Battery Voltage		2.5	3.0	3.5 <sup>(6)</sup>	2.5	3.0	3.5 <sup>(6)</sup>	V
V <sub>IH</sub>	Input High Voltage		0.7V <sub>CC</sub>		V <sub>CC</sub> + 0.3	0.7V <sub>CC</sub>		V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage		-0.3		0.3V <sub>CC</sub>	-0.3		0.3V <sub>CC</sub>	V
V <sub>OH</sub>	Output High Voltage <sup>(7)</sup>	I <sub>OH</sub> = -1.0mA	2.4			2.4			V
V <sub>OHB</sub>	V <sub>OH</sub> Battery Back-up <sup>(8)</sup>	I <sub>OUT2</sub> = -1.0µA	2.5	2.9	3.5	2.5	2.9	3.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 3.0mA			0.4			0.4	V
	Output Low Voltage (open drain) <sup>(9)</sup>	I <sub>OL</sub> = 10mA			0.4			0.4	V
V <sub>PFD</sub>	Power-fail Deselect Voltage		4.20	4.40	4.50	2.55	2.60	2.70	V
V <sub>PFI</sub>	PFI Input Threshold	V <sub>CC</sub> = 5V(Y) V <sub>CC</sub> = 3V(V)	1.225	1.250	1.275	1.225	1.250	1.275	V
	PFI Hysteresis	PFI Rising		20	70		20	70	mV
V <sub>SO</sub>	Battery Back-up Switchover Voltage			2.5			2.5		V

Note: 1. Valid for Ambient Operating Temperature: T<sub>A</sub> = -40 to 85°C; V<sub>CC</sub> = 2.7 to 3.6V or 4.5 to 5.5V(except where noted).

2. Measured with V<sub>OUT</sub> and E<sub>CON</sub> open.

3. RSTIN internally pulled-up to V<sub>CC</sub> through 100kΩ resistor.

4. Outputs deselected.

5. External SRAM must match SUPERVISOR chip V<sub>CC</sub> specification (3V or 5V).

6. For rechargeable back-up, V<sub>BAT</sub> (max) may be considered V<sub>CC</sub> - 0.5V.

7. For PFO pin (CMOS).

8. Chip Enable output (E<sub>CON</sub>) can only sustain CMOS leakage currents in the battery back-up mode. Higher leakage currents will reduce battery life.

9. For RST & BL pins (Open Drain).

**OPERATION**

The M40SZ100Y/W, as shown in Figure 7, page 5, can control one (two, if placed in parallel) standard low-power SRAM. This SRAM must be configured to have the chip enable input disable all other input signals. Most slow, low-power SRAMs are configured like this, however many fast SRAMs are not. During normal operating conditions, the conditioned chip enable ( $\overline{E}_{CON}$ ) output pin follows the chip enable ( $\overline{E}$ ) input pin with timing shown in Table 6, page 10. An internal switch connects  $V_{CC}$  to  $V_{OUT}$ . This switch has a voltage drop of less than 0.3V ( $I_{OUT1}$ ).

When  $V_{CC}$  degrades during a power failure,  $\overline{E}_{CON}$  is forced inactive independent of  $\overline{E}$ . In this situation, the SRAM is unconditionally write protected as  $V_{CC}$  falls below an out-of-tolerance threshold ( $V_{PFD}$ ). For the M40SZ100Y/W the power fail detection value associated with  $V_{PFD}$  is shown in Table 5, page 7.

If chip enable access is in progress during a power fail detection, that memory cycle continues to completion before the memory is write protected. If the memory cycle is not terminated within time  $t_{WPT}$ ,  $\overline{E}_{CON}$  is unconditionally driven high, write protecting the SRAM. A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the SRAM's contents. At voltages below  $V_{PFD}$  (min), the user can be assured the memory will be write protected within the Write Protect Time ( $t_{WPT}$ ) provided the  $V_{CC}$  fall time does not exceed  $t_F$  (see Table 6, page 10).

As  $V_{CC}$  continues to degrade, the internal switch disconnects  $V_{CC}$  and connects the internal battery to  $V_{OUT}$ . This occurs at the switchover voltage ( $V_{SO}$ ). Below the  $V_{SO}$ , the battery provides a voltage  $V_{OHB}$  to the SRAM and can supply current  $I_{OUT2}$  (see Table 5, page 7).

When  $V_{CC}$  rises above  $V_{SO}$ ,  $V_{OUT}$  is switched back to the supply voltage. Output  $\overline{E}_{CON}$  is held inactive for  $t_{CER}$  (120ms maximum) after the power

supply has reached  $V_{PFD}$ , independent of the  $\overline{E}$  input, to allow for processor stabilization (see Figure 11, page 10).

**Data Retention Lifetime Calculation**

Most low power SRAMs on the market today can be used with the M40SZ100Y/W NVRAM Controller. There are, however some criteria which should be used in making the final choice of which SRAM to use. The SRAM must be designed in a way where the chip enable input disables all other inputs to the SRAM. This allows inputs to the M40SZ100Y/W and SRAMs to be "Don't care" once  $V_{CC}$  falls below  $V_{PFD}(\text{min})$  (see Figure 10, page 9). The SRAM should also guarantee data retention down to  $V_{CC} = 2.0V$ . The chip enable access time must be sufficient to meet the system needs with the chip enable propagation delays included.

If data retention lifetime is a critical parameter for the system, it is important to review the data retention current specifications for the particular SRAMs being evaluated. Most SRAMs specify a data retention current at 3.0V. Manufacturers generally specify a typical condition for room temperature along with a worst case condition (generally at elevated temperatures). The system level requirements will determine the choice of which value to use. The data retention current value of the SRAMs can then be added to the  $I_{CCDR}$  value of the M40SZ100Y/W to determine the total current requirements for data retention. The available battery capacity for the SNAPHAT<sup>®</sup> of your choice (see Table 13, page 17) can then be divided by this current to determine the amount of data retention available.

**CAUTION:** Take care to avoid inadvertent discharge through  $V_{OUT}$  and  $\overline{E}_{CON}$  after battery has been attached.

For a further more detailed review of lifetime calculations, please see Application Note AN1012.



Figure 10. Power Down Timing

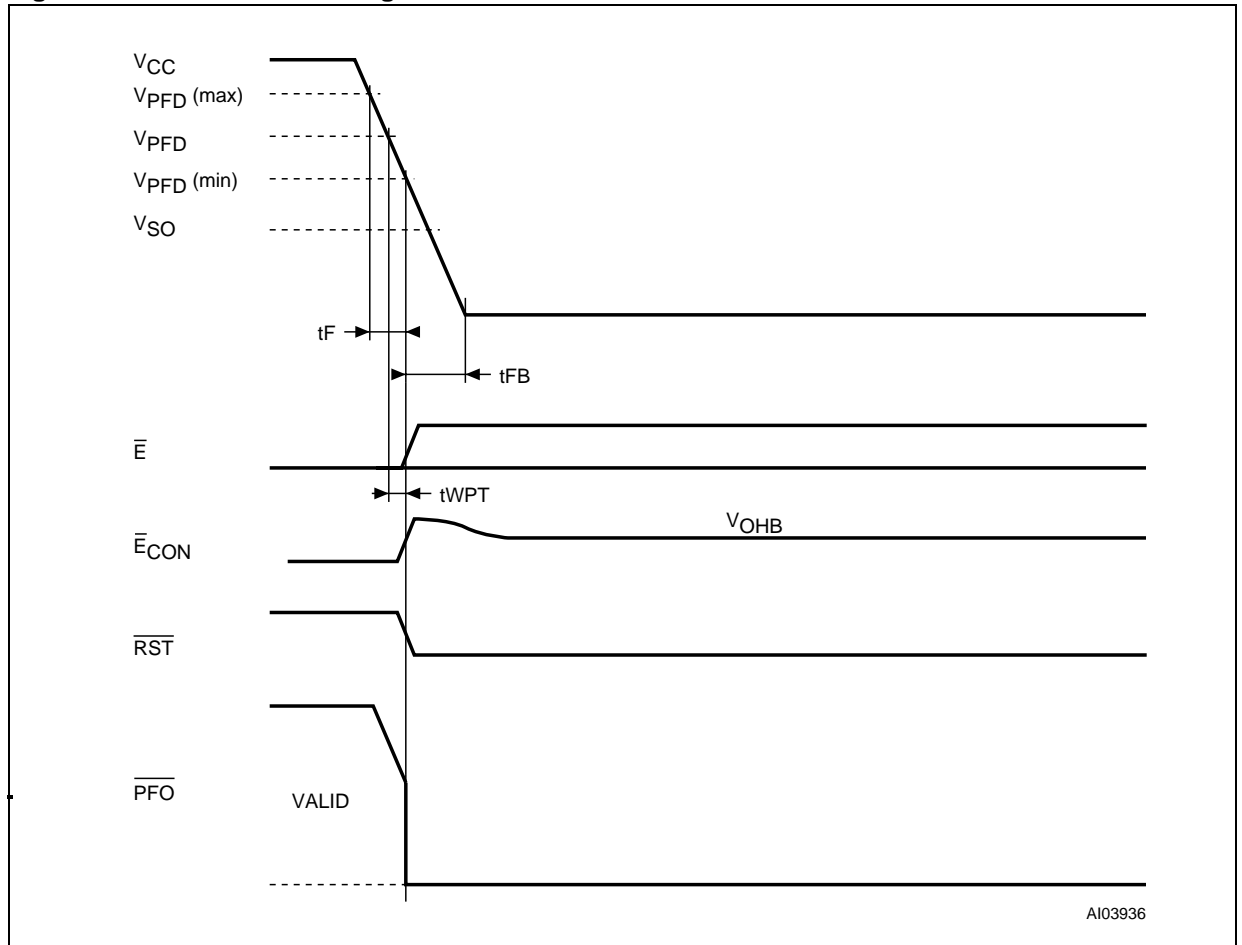
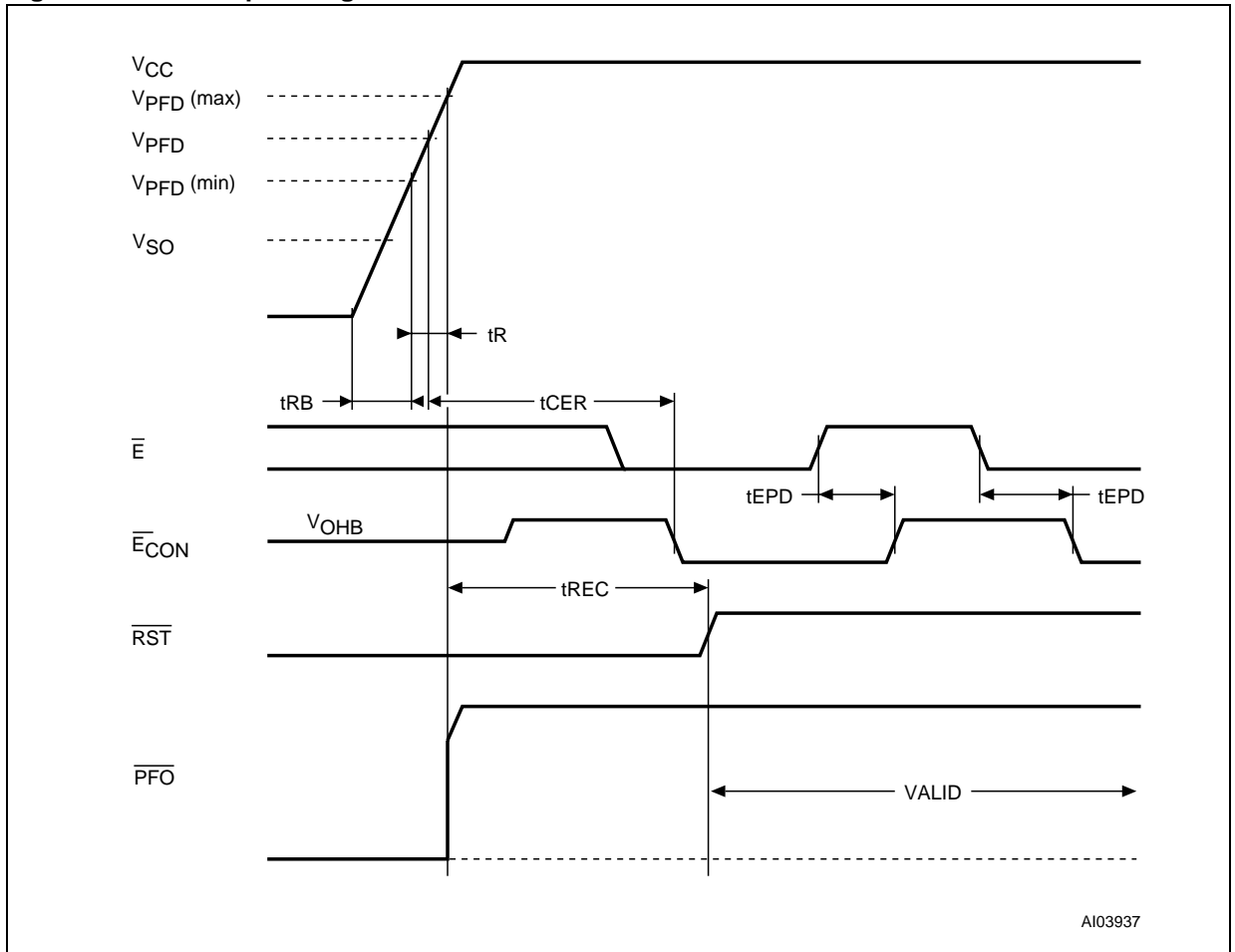


Figure 11. Power Up Timing



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Table 6. Power Down/Up AC Characteristics

Symbol	Parameter <sup>(1)</sup>	Min	Max	Unit
$t_F^{(2)}$	$V_{PF D (max)}$ to $V_{PF D (min)}$ $V_{CC}$ Fall Time	300		$\mu s$
$t_{FB}^{(3)}$	$V_{PF D (min)}$ to $V_{SS}$ $V_{CC}$ Fall Time	10		$\mu s$
$t_{PFD}$	PFI to $\overline{PFO}$ Propagation Delay	15	25	$\mu s$
$t_R$	$V_{PF D (min)}$ to $V_{PF D (max)}$ $V_{CC}$ Rise Time	10		$\mu s$
$t_{EPD}$	Chip Enable Propagation Delay (Low or High)	M40SZ100Y	10	ns
		M40SZ100W	15	ns
$t_{RB}$	$V_{SS}$ to $V_{PF D (min)}$ $V_{CC}$ Rise Time	1		$\mu s$
$t_{CER}$	Chip Enable Recovery	40	120	ms
$t_{REC}$	$V_{PF D (max)}$ to $\overline{RST}$ High	40	200	ms
$t_{WPT}$	Write Protect Time	40	200	$\mu s$

Note: 1. Valid for Ambient Operating Temperature:  $T_A = -40$  to  $85^\circ C$ ;  $V_{CC} = 2.7$  to  $3.6V$  or  $4.5$  to  $5.5V$  (except where noted).

2.  $V_{PF D (max)}$  to  $V_{PF D (min)}$  fall time of less than  $t_F$  may result in deselection/write protection not occurring until  $200 \mu s$  after  $V_{CC}$  passes  $V_{PF D (min)}$ .

3.  $V_{PF D (min)}$  to  $V_{SS}$  fall time of less than  $t_{FB}$  may cause corruption of RAM data.

### Power-on Reset Output

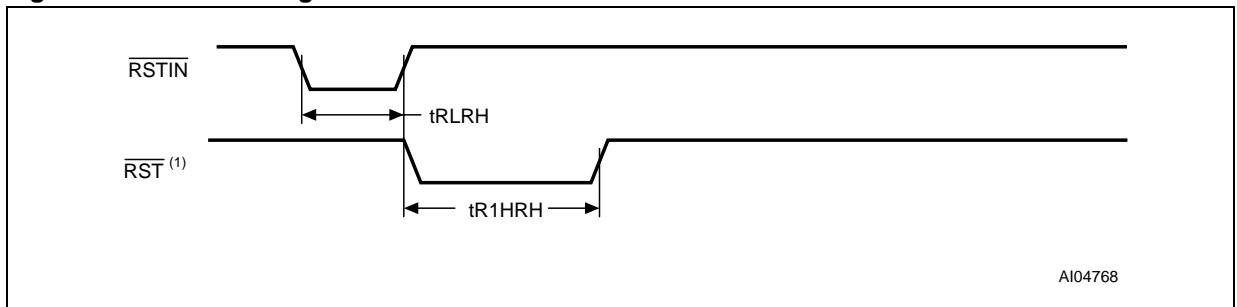
All microprocessors have a reset input which forces them to a known state when starting. The M40SZ100Y/W has a reset output ( $\overline{\text{RST}}$ ) pin which is guaranteed to be low by  $V_{\text{PFD}}$  (see Table 5, page 7). This signal is an open drain configuration. An appropriate pull-up resistor to  $V_{\text{CC}}$  should be chosen to control the rise time. This signal will be valid for all voltage conditions, even when  $V_{\text{CC}}$  equals  $V_{\text{SS}}$  (with valid battery voltage).

Once  $V_{\text{CC}}$  exceeds the power failure detect voltage  $V_{\text{PFD}}$ , an internal timer keeps  $\overline{\text{RST}}$  low for  $t_{\text{REC}}$  to allow the power supply to stabilize.

### Reset Input ( $\overline{\text{RSTIN}}$ )

The M40SZ100Y/W provides one independent input which can generate an output reset. The duration and function of this reset is identical to a reset generated by a power cycle. Table 7 and Figure 12 illustrate the AC reset characteristics of this function. Pulses shorter than  $t_{\text{RLRH}}$  will not generate a reset condition.  $\overline{\text{RSTIN}}$  is internally pulled up to  $V_{\text{CC}}$  through a 100k $\Omega$  resistor.

Figure 12.  $\overline{\text{RSTIN}}$  Timing Waveform



Note: With pull-up resistor

Table 7. Reset AC Characteristics

Symbol	Parameter <sup>(1)</sup>	Min	Max	Unit
$t_{\text{RLRH}}^{(2)}$	$\overline{\text{RSTIN}}$ Low to $\overline{\text{RSTIN}}$ High	200		ns
$t_{\text{R1HRH}}^{(3)}$	$\overline{\text{RSTIN}}$ High to $\overline{\text{RST}}$ High	40	200	ms

Note: 1. Valid for Ambient Operating Temperature:  $T_{\text{A}} = -40$  to  $85^{\circ}\text{C}$ ;  $V_{\text{CC}} = 2.7$  to  $3.6\text{V}$  or  $4.5$  to  $5.5\text{V}$  (except where noted).

2. Pulse width less than 50ns will result in no RESET (for noise immunity).

3.  $C_{\text{L}} = 5\text{pF}$  (see Figure 8, page 6).

**Battery Low Pin**

The M40SZ100Y/W automatically performs battery voltage monitoring upon power-up, and at factory-programmed time intervals of at least 24 hours. The Battery Low (BL) pin will be asserted if the battery voltage is found to be less than approximately 2.5V. The BL pin will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that the battery is below 2.5V and may not be able to maintain data integrity in the SRAM. Data should be considered suspect, and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal  $V_{CC}$  is supplied. In order to insure data integrity during subsequent periods of battery back-up mode, the battery should be replaced.

The M40SZ100Y/W only monitors the battery when a nominal  $V_{CC}$  is applied to the device. Thus applications which require extensive durations in the battery back-up mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique. The BL pin is an open drain output and an appropriate pull-up resistor to  $V_{CC}$  should be chosen to control the rise time.

**Power-fail Input/Output**

The Power-Fail Input (PFI) is compared to an internal reference voltage (independent from the  $V_{PFD}$  comparator). If PFI is less than the power-fail threshold ( $V_{PFI}$ ), the Power-Fail Output (PFO) will go low. This function is intended for use as an under-voltage detector to signal a failing power supply. Typically PFI is connected through an external voltage divider (see Figure 7, page 5) to either the unregulated DC input (if it is available) or the regulated output of the  $V_{CC}$  regulator. The voltage divider can be set up such that the voltage at PFI falls below  $V_{PFI}$  several milliseconds before the regulated  $V_{CC}$  input to the M40SZ100Y/W or the microprocessor drops below the minimum operating voltage.

During battery back-up, the power-fail comparator turns off and PFO goes (or remains) low. This oc-

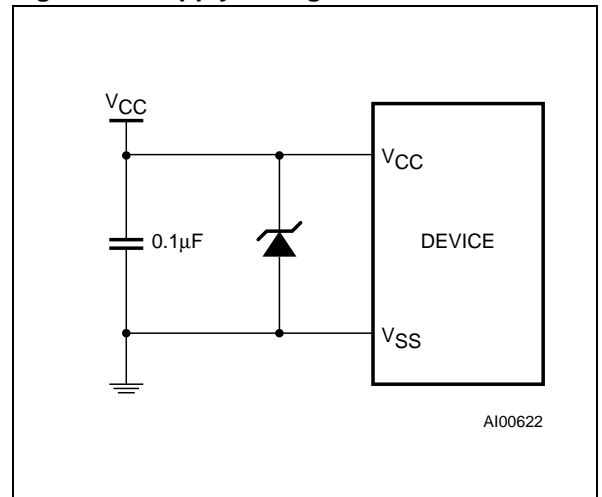
curs after  $V_{CC}$  drops below  $V_{PFD}(min)$ . When power returns, PFO is forced high, irrespective of  $V_{PFI}$  for the write protect time ( $t_{REC}$ ), which is the time from  $V_{PFD}(max)$  until the inputs are recognized. At the end of this time, the power-fail comparator is enabled and PFO follows PFI. If the comparator is unused, PFI should be connected to  $V_{SS}$  and PFO left unconnected.

**$V_{CC}$  Noise And Negative Going Transients**

$I_{CC}$  transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the  $V_{CC}$  bus. These transients can be reduced if capacitors are used to store energy which stabilizes the  $V_{CC}$  bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1 $\mu$ F (as shown in Figure 13) is recommended in order to provide the needed filtering.

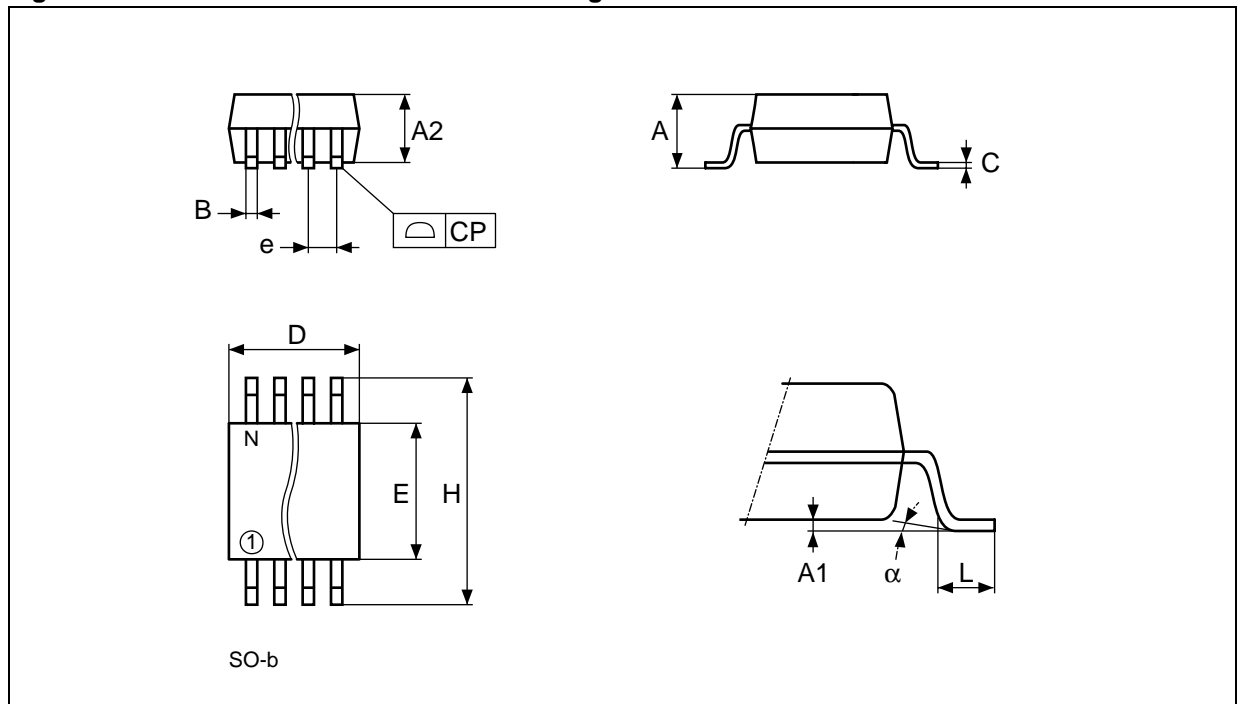
In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on  $V_{CC}$  that drive it to values below  $V_{SS}$  by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, STMicroelectronics recommends connecting a schottky diode from  $V_{CC}$  to  $V_{SS}$  (cathode connected to  $V_{CC}$ , anode to  $V_{SS}$ ). Schottky diode 1N5817 is recommended for through hole and MBR5120T3 is recommended for surface mount.

**Figure 13. Supply Voltage Protection**



## PACKAGE MECHANICAL INFORMATION

Figure 14. SO16 – 16-lead Plastic Small Package Outline

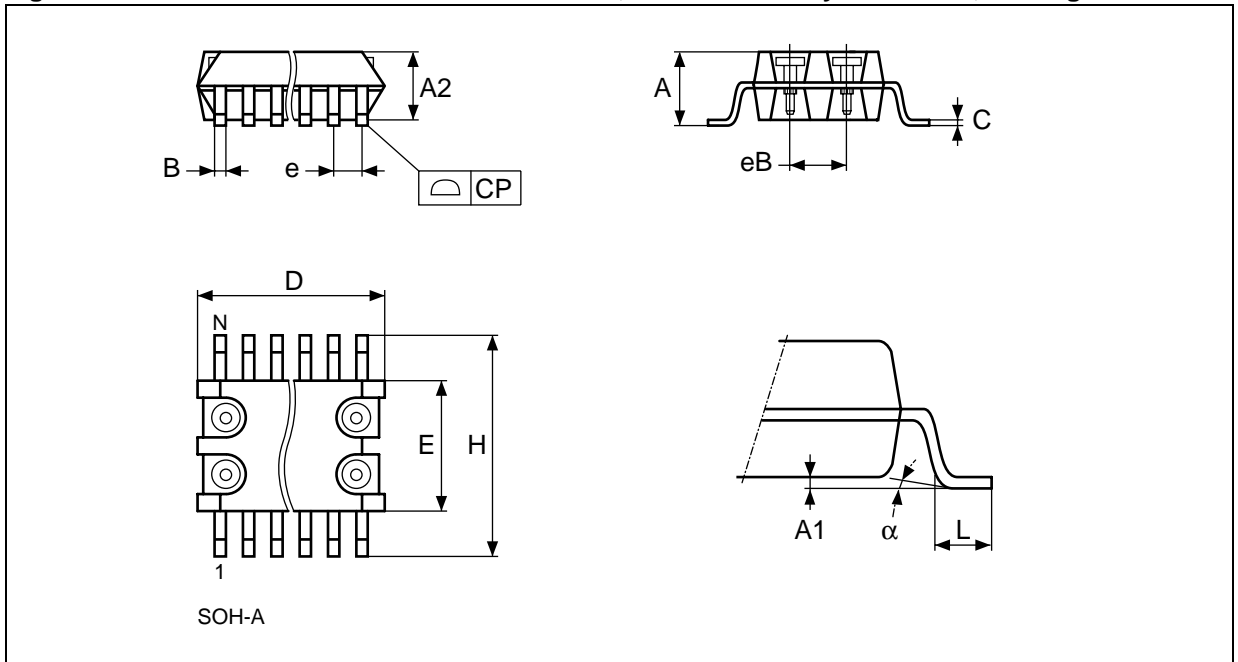


Note: Drawing is not to scale.

Table 8. SO16 – 16-lead Plastic Small Plastic Package Mechanical Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2			1.60			0.063
B		0.35	0.46		0.014	0.018
C		0.19	0.25		0.007	0.010
D		9.80	10.00		0.386	0.394
E		3.80	4.00		0.150	0.158
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
L		0.40	1.27		0.016	0.050
a		0°	8°		0°	8°
N	16			16		
CP			0.10			0.004

Figure 15. SOH28 – 28-lead Plastic Small Outline, 4-socket battery SNAPHAT, Package Outline

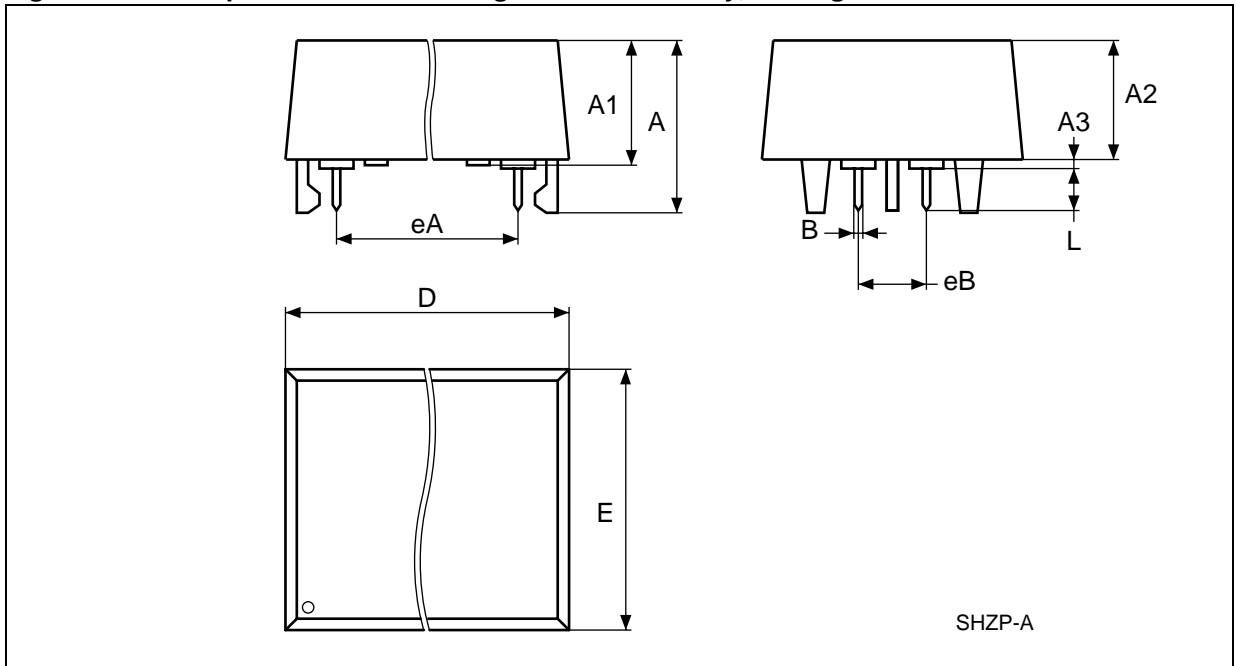


Note: Drawing is not to scale.

Table 9. SOH28 – 28-lead Plastic Small Outline, battery SNAPHAT, Package Mechanical Data

Symbol	mm			inches			
	Typ	Min	Max	Typ	Min	Max	
A			3.05			0.120	
A1		0.05	0.36		0.002	0.014	
A2		2.34	2.69		0.092	0.106	
B		0.36	0.51		0.014	0.020	
C		0.15	0.32		0.006	0.012	
D		17.71	18.49		0.697	0.728	
E		8.23	8.89		0.324	0.350	
e	1.27	–	–	0.050	–	–	
eB		3.20	3.61		0.126	0.142	
H		11.51	12.70		0.453	0.500	
L		0.41	1.27		0.016	0.050	
$\alpha$		0°	8°		0°	8°	
N		28			28		
CP			0.10			0.004	

Figure 16. SH – 4-pin SNAPHAT Housing for 48mAh Battery, Package Outline

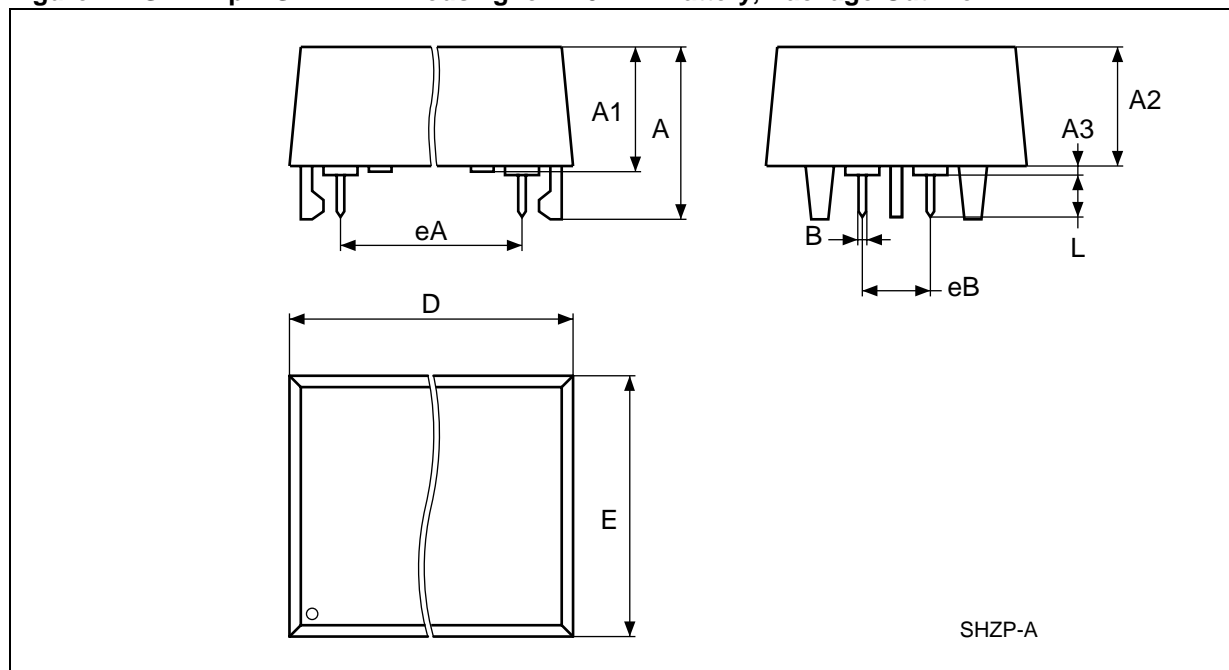


Note: Drawing is not to scale.

Table 10. SH – 4-pin SNAPHAT Housing for 48mAh Battery, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 17. SH – 4-pin SNAPHAT Housing for 120mAh Battery, Package Outline



Note: Drawing is not to scale.

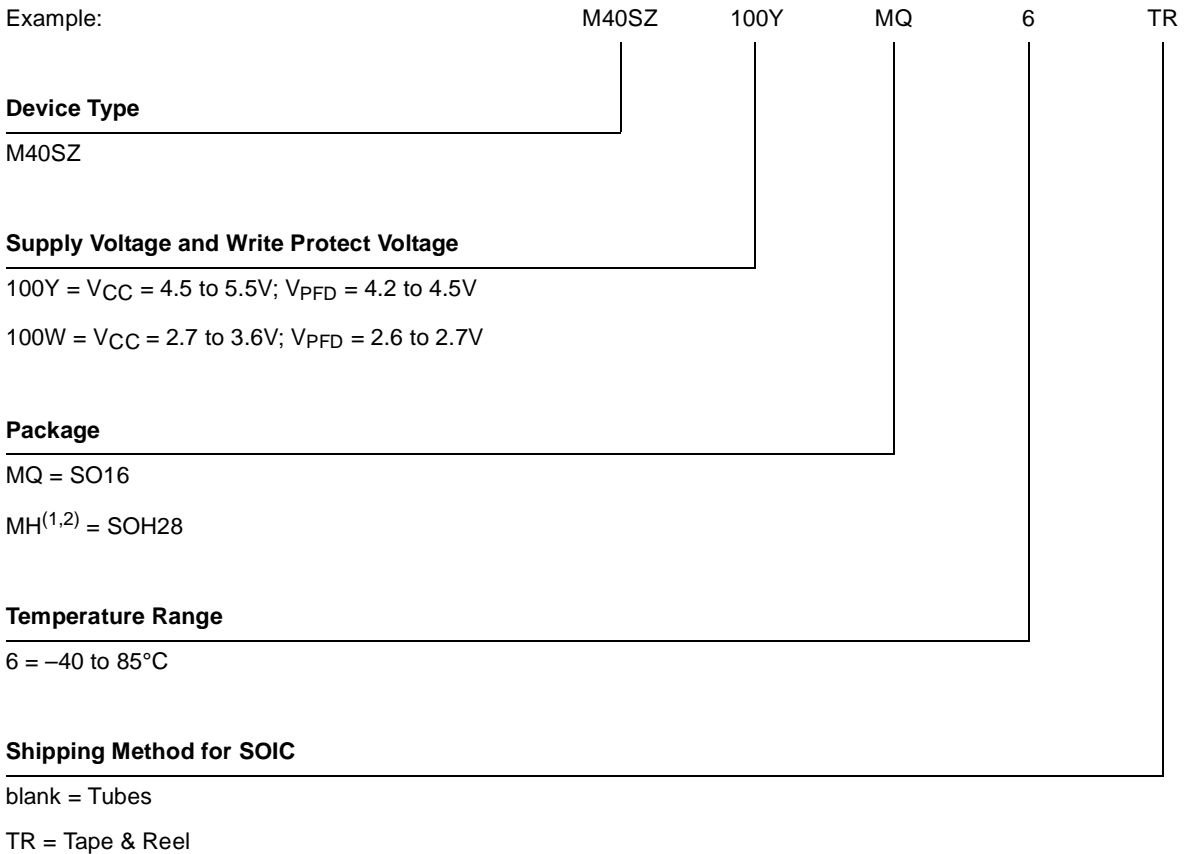
Table 11. SH – 4-pin SNAPHAT Housing for 120mAh Battery, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54			0.415
A1		8.00	8.51		0.315	0.335
A2		7.24	8.00		0.285	0.315
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	0.710
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090



**PART NUMBERING**

**Table 12. Ordering Information Scheme**



Note: 1. The SOIC package (SOH28) requires the battery package (SNAPHAT<sup>®</sup>) which is ordered separately under the part number "M4ZXX-BR00SHX" in plastic tube or "M4ZXX-BR00SHXTR" in Tape & Reel form.  
 2. Contact Local Sales Office

**Caution:** Do not place the SNAPHAT battery package "M4Zxx-BR00SH" in conductive foam as it will drain the lithium button-cell battery.

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

**Table 13. SNAPHAT<sup>®</sup> Battery Table**

Part Number	Description	Package
M4Z28-BR00SH	SNAPHAT Housing for 48mAh Battery	SH
M4Z32-BR00SH	SNAPHAT Housing for 120mAh Battery	SH

**REVISION HISTORY****Table 14. Document Revision History**

<b>Date</b>	<b>Rev. #</b>	<b>Revision Details</b>
December 2001	1.0	First Issue
13-May-02	1.1	Modify reflow time and temperature footnote (Table 2)
01-Aug-02	1.2	Add marketing status (Figure 2; Table 12)
15-Sep-03	1.3	Remove reference to M68xxx (obsolete) part (Figure 7); update disclaimer

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