



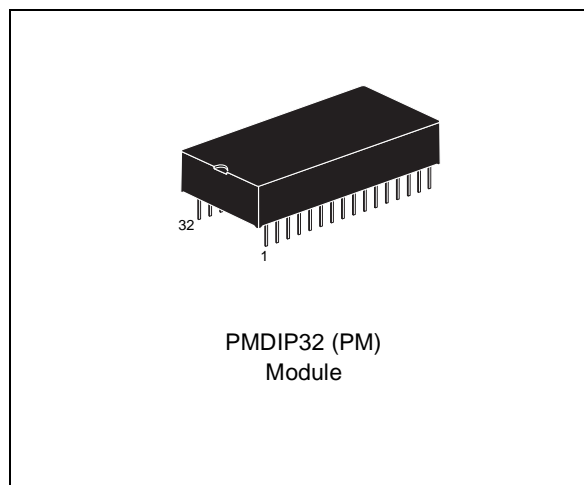
# M48Z129Y M48Z129V

## 3.3V/5V 1 Mbit (128Kb x8) ZEROPOWER® SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT, and BATTERY
- AUTOMATIC POWER-FAIL CHIP DESELECT AND WRITE PROTECTION
- MICROPROCESSOR POWER-ON RESET (RESET VALID EVEN DURING BATTERY BACK-UP MODE)
- BATTERY LOW PIN - PROVIDES WARNING OF BATTERY END-OF-LIFE
- WRITE PROTECT VOLTAGES ( $V_{PFD}$  = Power-fail Deselect Voltage):
  - M48Z129Y:  $4.2V \leq V_{PFD} \leq 4.5V$
  - M48Z129V:  $2.7V \leq V_{PFD} \leq 3.0V$
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS OF DATA RETENTION IN THE ABSENCE OF POWER
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 128Kb x 8 SRAMS
- SELF CONTAINED BATTERY IN DIP PACKAGE

**Table 1. Signal Names**

A0-A16	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
$\bar{W}$	Write Enable
$\overline{RST}$	Reset Output (Open Drain)
$\overline{BL}$	Battery Low Output (Open Drain)
V <sub>CC</sub>	Supply Voltage
V <sub>SS</sub>	Ground



**Figure 1. Logic Diagram**

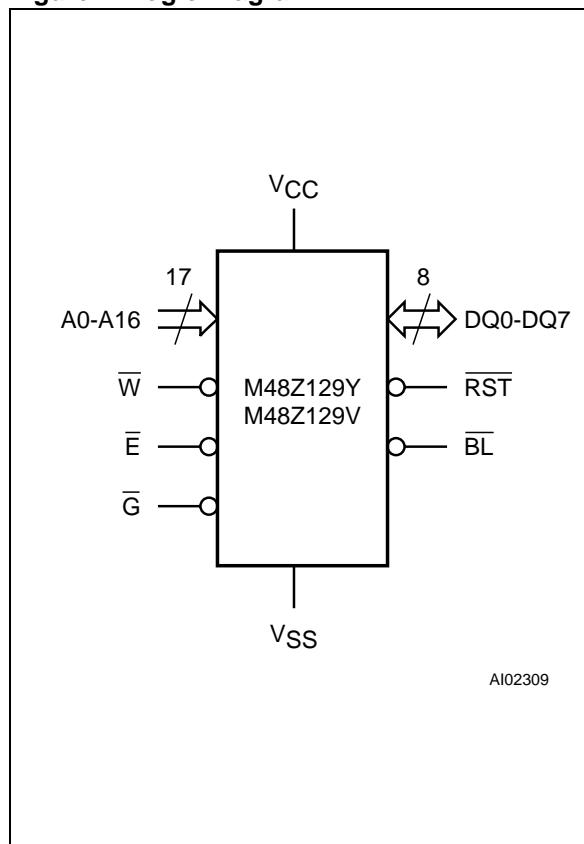


Table 2. Absolute Maximum Ratings <sup>(1)</sup>

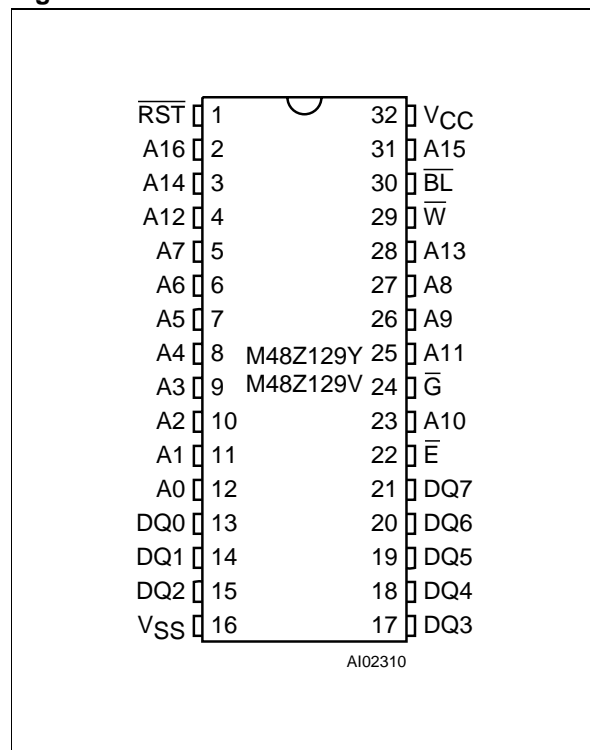
Symbol	Parameter	Value	Unit
T <sub>A</sub>	Ambient Operating Temperature	0 to 70	°C
T <sub>STG</sub>	Storage Temperature (V <sub>CC</sub> Off)	–40 to 70	°C
T <sub>BIAS</sub>	Temperature Under Bias	–10 to 70	°C
T <sub>SLD</sub> <sup>(2)</sup>	Lead Solder Temperature for 10 seconds	260	°C
V <sub>IO</sub>	Input or Output Voltages	–0.3 to V <sub>CC</sub> +0.3	V
V <sub>CC</sub>	Supply Voltage	M48Z129Y –0.3 to 7.0 M48Z129V –0.3 to 4.6	V

Note: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.

2. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

**CAUTION:** Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.

Figure 2A. DIP Pin Connections



## DESCRIPTION

The M48Z129Y/V ZEROPOWER SRAM is a 1,048,576 bit non-volatile static RAM organized as 131,072 words by 8 bits. The device combines an internal lithium battery, a CMOS SRAM and a control circuit in a plastic 32 pin DIP Module. The M48Z129Y/V directly replaces industry standard

128K x 8 SRAM. It also provides the non-volatility of FLASH without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z129Y/V also has its own Power-Fail Detect circuit. This control circuitry constantly monitors the supply voltage for an out of tolerance condition. When V<sub>CC</sub> is out of tolerance, the circuit write protects the SRAM, providing data security in the midst of unpredictable system operation. As V<sub>CC</sub> falls, the control circuitry automatically switches to the battery, maintaining data until valid power is restored.

## READ MODE

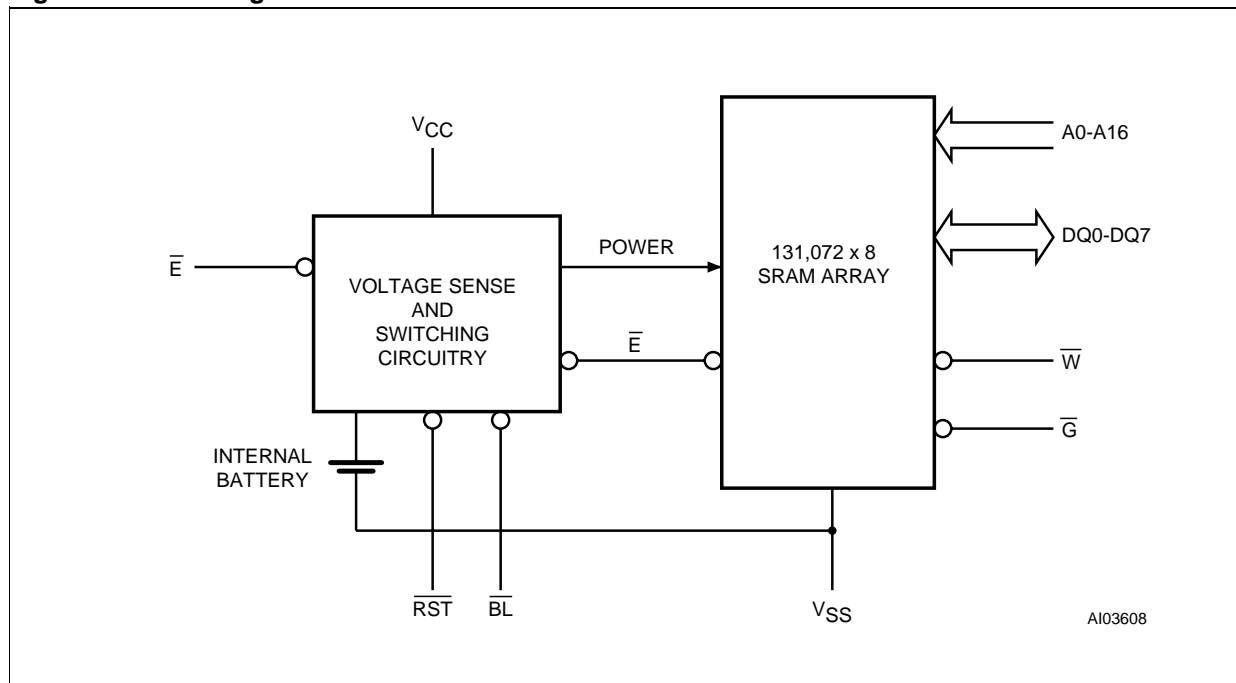
The M48Z129Y/V is in the Read Mode whenever  $\overline{W}$  (Write Enable) is high and  $\overline{E}$  (Chip Enable) is low. The unique address specified by the 17 Address Inputs defines which one of the 131,072 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t<sub>AVQV</sub> (Address Access Time) after the last address input signal is stable, providing the  $\overline{E}$  and  $\overline{G}$  access times are also satisfied. If the  $\overline{E}$  and  $\overline{G}$  access times are not met, valid data will be available after the latter of the Chip Enable Access Times (t<sub>ELQV</sub>) or Output Enable Access Time (t<sub>GLQV</sub>).

The state of the eight three-state Data I/O signals is controlled by  $\overline{E}$  and  $\overline{G}$ . If the outputs are activated before t<sub>AVQV</sub>, the data lines will be driven to an indeterminate state until t<sub>AVQV</sub>. If the Address Inputs are changed while  $\overline{E}$  and  $\overline{G}$  remain active, output data will remain valid for t<sub>AXQX</sub> (Output Data Hold Time) but will go indeterminate until the next Address Access.

**Table 3. Operating Modes <sup>(1)</sup>**

Mode	V <sub>CC</sub>	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.5V to 5.5V (M48Z129Y) or 3.0V to 3.6V (M48Z129V)	V <sub>IH</sub>	X	X	High Z	Standby
Write		V <sub>IL</sub>	X	V <sub>IL</sub>	D <sub>IN</sub>	Active
Read		V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>	Active
Read		V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	High Z	Active
Deselect	V <sub>SO</sub> to V <sub>PF</sub> D (min) <sup>(2)</sup>	X	X	X	High Z	CMOS Standby
Deselect	≤ V <sub>SO</sub> <sup>(2)</sup>	X	X	X	High Z	Battery Back-up Mode

Note: 1. X = V<sub>IH</sub> or V<sub>IL</sub>; V<sub>SO</sub> = Battery Back-up Switchover Voltage.  
 2. See Table 7 for details.

**Figure 3. Block Diagram****WRITE MODE**

The M48Z129Y/V is in the Write Mode whenever  $\overline{W}$  (Write Enable) and  $\overline{E}$  (Chip Enable) are active. The start of a write is referenced from the latter occurring falling edge of  $\overline{W}$  or  $\overline{E}$ . A write is terminated by the earlier rising edge of  $\overline{W}$  or  $\overline{E}$ . The addresses must be held valid throughout the cycle.  $\overline{E}$  or  $\overline{W}$  must return high for a minimum of  $t_{EHAX}$  from Chip Enable or  $t_{WHAX}$  from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid  $t_{DVWH}$  prior to the end of write and remain valid for  $t_{WHDx}$  afterward.  $\overline{G}$  should be kept high during write cycles to avoid

bus contention; although, if the output bus has been activated by a low on  $\overline{E}$  and  $\overline{G}$  a low on  $\overline{W}$  will disable the outputs  $t_{WLQZ}$  after  $\overline{W}$  falls.

**DATA RETENTION MODE**

With valid V<sub>CC</sub> applied, the M48Z129Y/V operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically deselect, write protecting itself when V<sub>CC</sub> falls between V<sub>PF</sub>D (max), V<sub>PF</sub>D (min) window. All outputs become high impedance and all inputs are treated as “don’t care”.

**Table 4. AC Measurement Conditions**

Input Rise and Fall Times	$\leq 5\text{ns}$
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

**Note:** A power failure during a write cycle may corrupt data at the current addressed location, but does not jeopardize the rest of the RAM's content. At voltages below  $V_{\text{PFD}}(\text{min})$ , the memory will be in a write protected state, provided the  $V_{\text{CC}}$  fall time is not less than  $t_{\text{F}}$ . The M48Z129Y/V may respond to transient noise spikes on  $V_{\text{CC}}$  that cross into the deselect window during the time the device is sampling  $V_{\text{CC}}$ . Therefore, decoupling of the power supply lines is recommended.

When  $V_{\text{CC}}$  drops below  $V_{\text{SO}}$ , the control circuit switches power to the internal battery, preserving data. The internal energy source will maintain data in the M48Z129Y/V for an accumulated period of at least 10 years at room temperature. As system power rises above  $V_{\text{SO}}$ , the battery is disconnected, and the power supply is switched to external  $V_{\text{CC}}$ . Deselect continues for  $t_{\text{REC}}$  after  $V_{\text{CC}}$  reaches  $V_{\text{PFD}}(\text{max})$ .

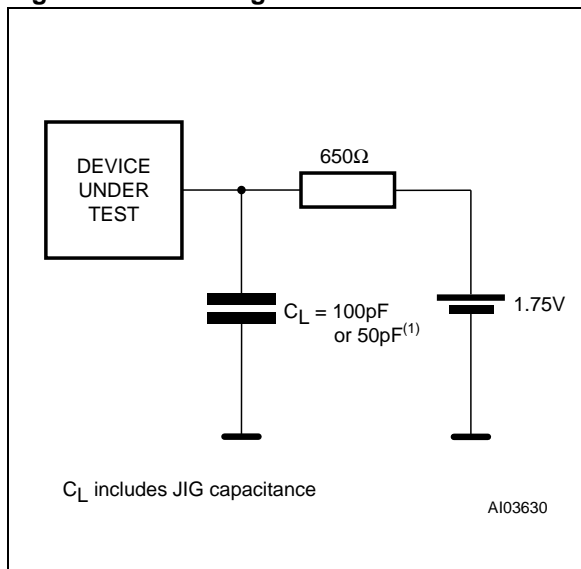
For more information on Battery Storage Life refer to the Application Note AN1012.

### POWER-ON RESET OUTPUT

All microprocessors have a reset input which forces them to a known state when starting. The M48Z129Y/V has a reset output ( $\overline{\text{RST}}$ ) pin which is guaranteed to be low below  $V_{\text{PFD}}(\text{min})$ . This signal is an open drain configuration. An appropriate pull-up resistor should be chosen to control the rise time. This signal will be valid for all voltage conditions, even when  $V_{\text{CC}}$  equals  $V_{\text{SS}}$ . Once  $V_{\text{CC}}$  exceeds the power failure detect voltage  $V_{\text{PFD}}$ , an internal timer keeps  $\overline{\text{RST}}$  low for  $t_{\text{REC}}$  to allow the power supply to stabilize.

### BATTERY LOW PIN

The M48Z129Y/V automatically performs battery voltage monitoring upon power-up, and at factory-

**Figure 4. AC Testing Load Circuit**

Note: 1. 50pF for M48Z129V (3.3V).

programmed time intervals of 24 hours. The Battery Low ( $\overline{\text{BL}}$ ) pin will be asserted if the battery voltage is found to be less than approximately 2.5V. If a battery low is generated during a power-up sequence, this indicates that the battery is below 2.5 volts and may not be able to maintain data integrity in the SRAM. Data should be considered suspect, and verified as correct.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal  $V_{\text{CC}}$  is supplied.

The M48Z129Y/V only monitors the battery when a nominal  $V_{\text{CC}}$  is applied to the device. Thus applications which require extensive durations in the battery back-up mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique. The  $\overline{\text{BL}}$  pin is an open drain output and an appropriate pull-up resistor should be chosen to control the rise time.

**Table 5. Capacitance <sup>(1)</sup>**(T<sub>A</sub> = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V		10	pF
C <sub>IO</sub> <sup>(2)</sup>	Input / Output Capacitance	V <sub>OUT</sub> = 0V		10	pF

Note: 1. Effective capacitance measured with power supply at 5V.

2. Outputs deselected.

**Table 6A. DC Characteristics**(T<sub>A</sub> = 0 to 70 °C; V<sub>CC</sub> = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I <sub>LI</sub> <sup>(1)</sup>	Input Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		±1	μA
I <sub>LO</sub> <sup>(1)</sup>	Output Leakage Current	0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>		±1	μA
I <sub>CC</sub>	Supply Current	Outputs open		95	mA
I <sub>CC1</sub>	Supply Current (Standby) TTL	$\bar{E} = V_{IH}$		7	mA
I <sub>CC2</sub>	Supply Current (Standby) CMOS	$\bar{E} = V_{CC} - 0.2V$		4	mA
V <sub>IL</sub>	Input Low Voltage		-0.3	0.8	V
V <sub>IH</sub>	Input High Voltage		2.2	V <sub>CC</sub> + 0.3	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1mA	2.4		V

Note: 1. Outputs deselected.

**Table 6B. DC Characteristics**(T<sub>A</sub> = 0 to 70 °C; V<sub>CC</sub> = 3.0V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I <sub>LI</sub> <sup>(1)</sup>	Input Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		±1	μA
I <sub>LO</sub> <sup>(1)</sup>	Output Leakage Current	0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>		±1	μA
I <sub>CC</sub>	Supply Current	Outputs open		50	mA
I <sub>CC1</sub>	Supply Current (Standby) TTL	$\bar{E} = V_{IH}$		4	mA
I <sub>CC2</sub>	Supply Current (Standby) CMOS	$\bar{E} = V_{CC} - 0.2V$		3	mA
V <sub>IL</sub>	Input Low Voltage		-0.3	0.6	V
V <sub>IH</sub>	Input High Voltage		2.2	V <sub>CC</sub> + 0.3	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1mA	2.2		V

Note: 1. Outputs deselected.

**Table 7. Power Down/Up Trip Points DC Characteristics <sup>(1)</sup>**  
 (T<sub>A</sub> = 0 to 70 °C)

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>PFD</sub>	Power-fail Deselect Voltage (M48Z129Y)	4.2	4.35	4.5	V
	Power-fail Deselect Voltage (M48Z129V)	2.7	2.9	3.0	
V <sub>SO</sub>	Battery Back-up Switchover Voltage (M48Z129Y)		3.0		V
	Battery Back-up Switchover Voltage (M48Z129V)		2.45		
t <sub>DR</sub> <sup>(2)</sup>	Expected Data Retention Time	10			YEARS

Note: 1. All voltages referenced to V<sub>SS</sub>.  
 2. At 25 °C.

**Table 8. Power Down/Up AC Characteristics**  
 (T<sub>A</sub> = 0 to 70 °C)

Symbol	Parameter	Min	Max	Unit
t <sub>F</sub> <sup>(1)</sup>	V <sub>PFD</sub> (max) to V <sub>PFD</sub> (min) V <sub>CC</sub> Fall Time	300		μs
t <sub>FB</sub> <sup>(2)</sup>	V <sub>PFD</sub> (min) to V <sub>SS</sub> V <sub>CC</sub> Fall Time (M48Z129Y)	10		μs
	V <sub>PFD</sub> (min) to V <sub>SS</sub> V <sub>CC</sub> Fall Time (M48Z129V)	150		
t <sub>R</sub>	V <sub>PFD</sub> (min) to V <sub>PFD</sub> (max) V <sub>CC</sub> Rise Time	10		μs
t <sub>RB</sub>	V <sub>SS</sub> to V <sub>PFD</sub> (min) V <sub>CC</sub> Rise Time	1		μs
t <sub>WPT</sub>	Write Protect Time (M48Z129Y)	40	150	μs
	Write Protect Time (M48Z129V)	40	250	
t <sub>REC</sub>	V <sub>PFD</sub> (max) to $\overline{\text{RST}}$ High	40	200	ms

Note: 1. V<sub>PFD</sub> (max) to V<sub>PFD</sub> (min) fall time of less than t<sub>F</sub> may result in deselection/write protection not occurring until 200μs after V<sub>CC</sub> passes V<sub>PFD</sub> (min).  
 2. V<sub>PFD</sub> (min) to V<sub>SS</sub> fall time of less than t<sub>FB</sub> may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

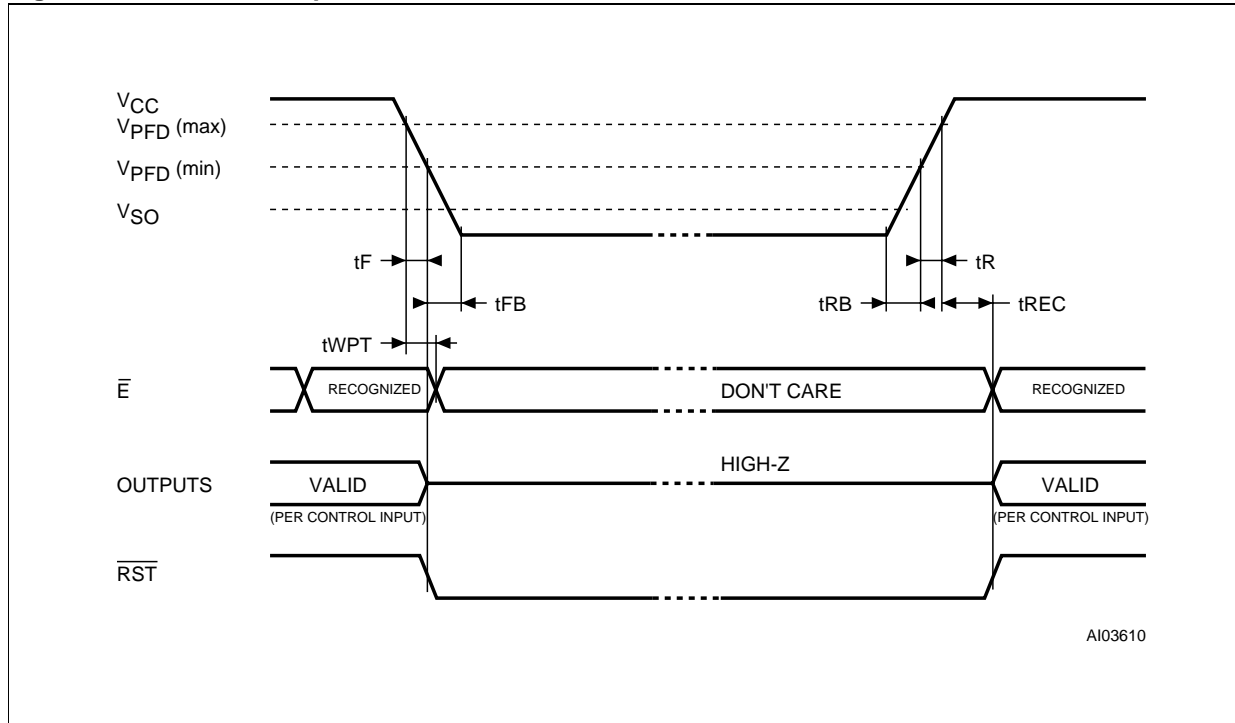


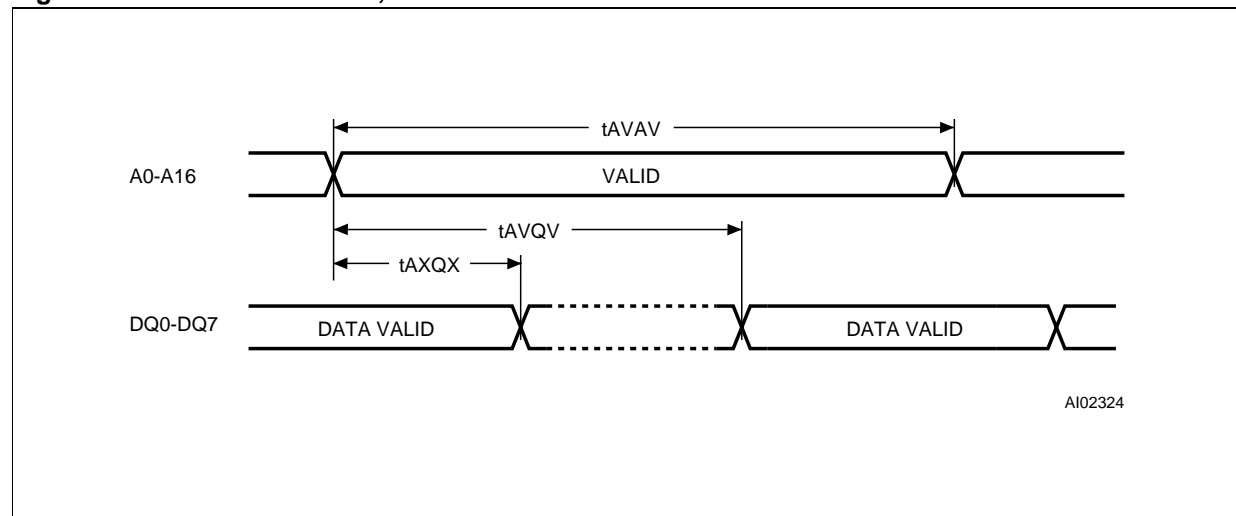
Table 9. Read Mode AC Characteristics

(T<sub>A</sub> = 0 to 70 °C; V<sub>CC</sub> = 4.5V to 5.5V or 3.0V to 3.6V)

Symbol	Parameter	M48Z129Y		M48Z129V		Unit
		-70		-85		
		Min	Max	Min	Max	
t <sub>AVAV</sub>	Read Cycle Time	70		85		ns
t <sub>AVQV</sub> <sup>(1)</sup>	Address Valid to Output Valid		70		85	ns
t <sub>ELQV</sub> <sup>(1)</sup>	Chip Enable Low to Output Valid		70		85	ns
t <sub>GLQV</sub> <sup>(1)</sup>	Output Enable Low to Output Valid		35		45	ns
t <sub>ELQX</sub> <sup>(2)</sup>	Chip Enable Low to Output Transition	5		5		ns
t <sub>GLQX</sub> <sup>(2)</sup>	Output Enable Low to Output Transition	3		5		ns
t <sub>EHQZ</sub> <sup>(2)</sup>	Chip Enable High to Output Hi-Z		30		40	ns
t <sub>GHQZ</sub> <sup>(2)</sup>	Output Enable High to Output Hi-Z		20		25	ns
t <sub>AXQX</sub> <sup>(1)</sup>	Address Transition to Output Transition	5		5		ns

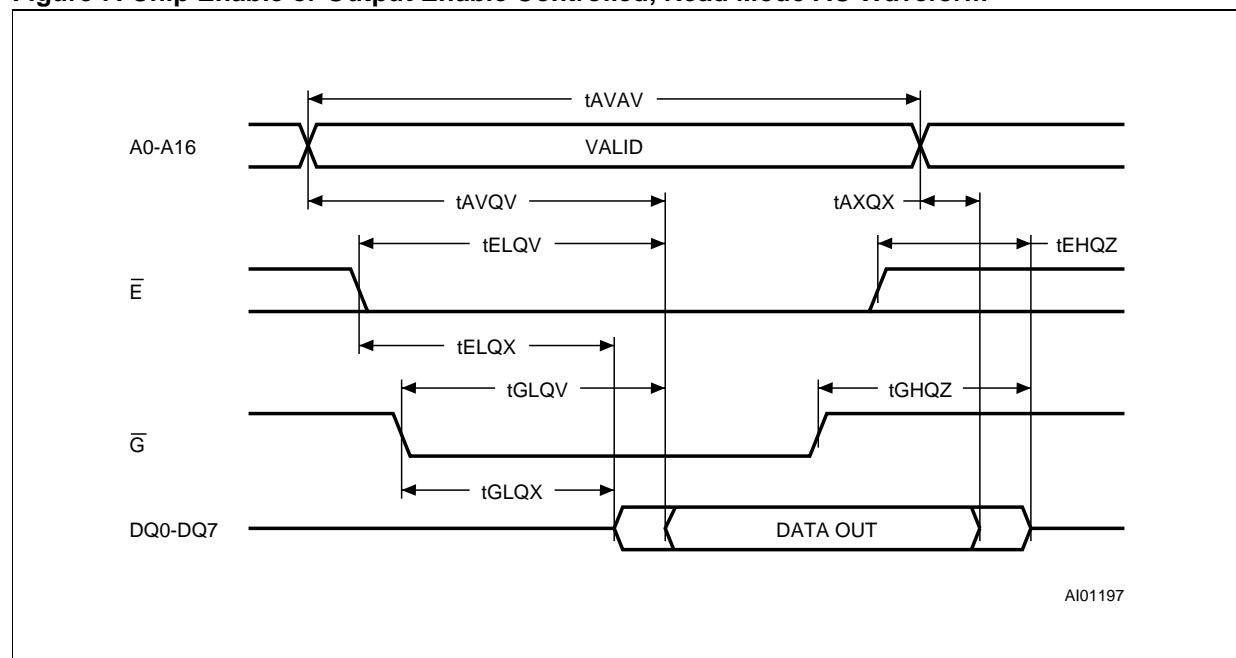
Note: 1. C<sub>L</sub> = 100pF or 50pF (see Figure 4).2. C<sub>L</sub> = 5pF (see Figure 4).

**Figure 6. Address Controlled, Read Mode AC Waveforms.**



Note: Chip Enable ( $\overline{E}$ ) and Output Enable ( $\overline{G}$ ) = Low, Write Enable ( $\overline{W}$ ) = High.

**Figure 7. Chip Enable or Output Enable Controlled, Read Mode AC Waveform**





**Table 10. Write Mode AC Characteristics**(T<sub>A</sub> = 0 to 70 °C; V<sub>CC</sub> = 4.5V to 5.5V or 3.0V to 3.6V)

Symbol	Parameter	M48Z129Y		M48Z129V		Unit
		-70		-85		
		Min	Max	Min	Max	
t <sub>AVAV</sub>	Write Cycle Time	70		85		ns
t <sub>AVWL</sub>	Address Valid to Write Enable Low	0		0		ns
t <sub>AVEL</sub>	Address Valid to Chip Enable Low	0		0		ns
t <sub>WLWH</sub>	Write Enable Pulse Width	55		65		ns
t <sub>LELH</sub>	Chip Enable Low to Chip Enable High	55		75		ns
t <sub>WHAX</sub>	Write Enable High to Address Transition	5		5		ns
t <sub>EHAX</sub>	Chip Enable High to Address Transition	15		15		ns
t <sub>DVWH</sub>	Input Valid to Write Enable High	30		35		ns
t <sub>DVEH</sub>	Input Valid to Chip Enable High	30		35		ns
t <sub>WHDX</sub>	Write Enable High to Input Transition	0		0		ns
t <sub>EHDX</sub>	Chip Enable High to Input Transition	10		15		ns
t <sub>WLQZ</sub> <sup>(1, 2)</sup>	Write Enable Low to Output Hi-Z		25		30	ns
t <sub>AVWH</sub>	Address Valid to Write Enable High	65		75		ns
t <sub>AVEH</sub>	Address Valid to Chip Enable High	65		75		ns
t <sub>WHQX</sub> <sup>(1, 2)</sup>	Write Enable High to Output Transition	5		5		ns

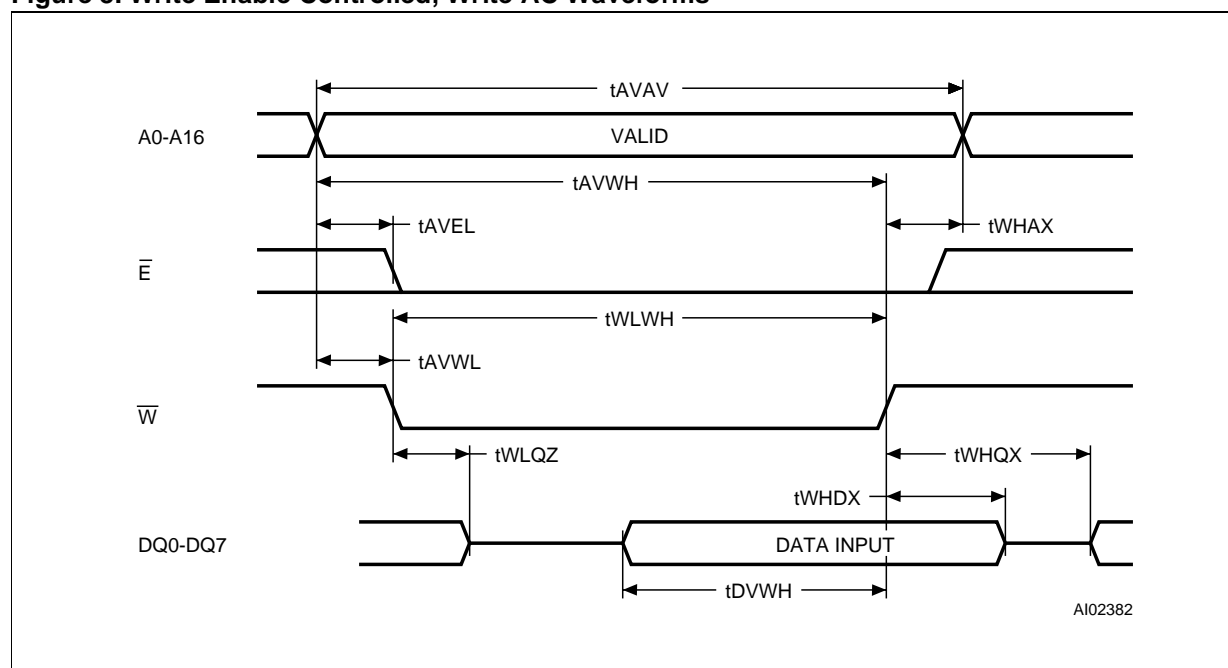
Note: 1. C<sub>L</sub> = 5pF (see Figure 4).2. If  $\overline{E}$  goes low simultaneously with  $\overline{W}$  going low, the outputs remain in the high impedance state.**Figure 8. Write Enable Controlled, Write AC Waveforms**

Figure 9. Chip Enable Controlled, Write AC Waveforms

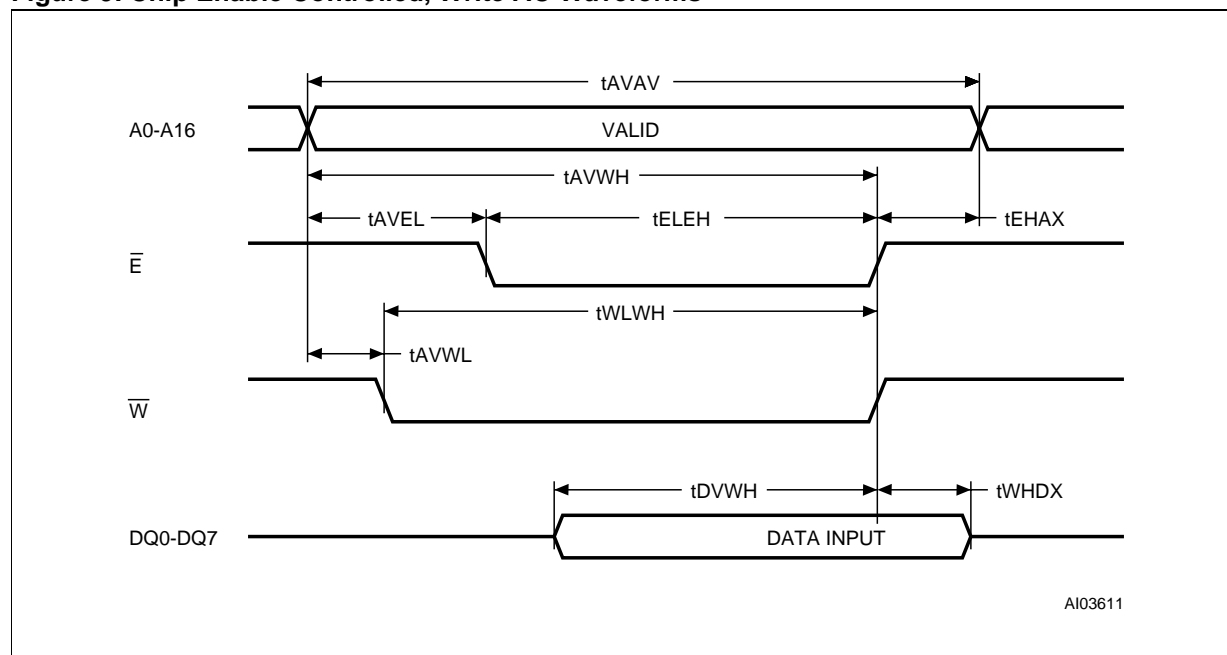
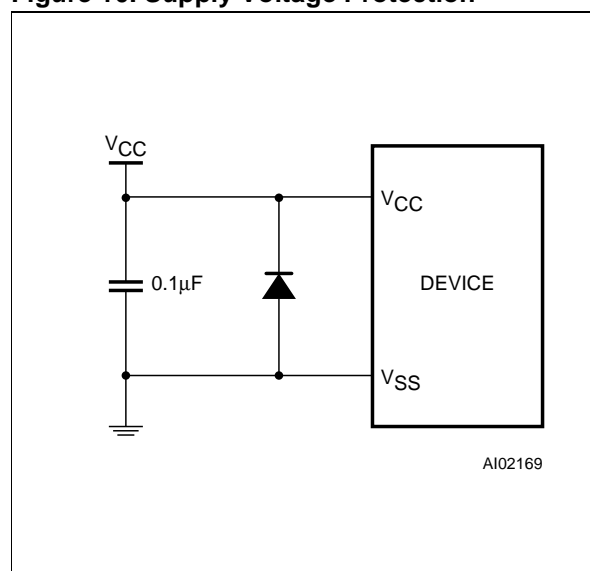


Figure 10. Supply Voltage Protection



#### POWER SUPPLY DECOUPLING AND UNDERSHOOT PROTECTION

ICC transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the  $V_{CC}$  bus. These transients can be reduced if capacitors are used to store energy, which stabilizes the  $V_{CC}$  bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1 microfarad is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on  $V_{CC}$  that drive it to values below  $V_{SS}$  by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a schottky diode from  $V_{CC}$  to  $V_{SS}$  (cathode connected to  $V_{CC}$ , anode to  $V_{SS}$ ). (Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount).

**Table 11. Ordering Information Scheme**

Example:	M48Z129Y	-70	PM	1
<b>Supply Voltage and Write Protect Voltage</b>				
129Y = $V_{CC} = 4.5V$ to $5.5V$ ; $V_{PFD} = 4.2V$ to $4.5V$				
129V = $V_{CC} = 3.0V$ to $3.6V$ ; $V_{PFD} = 2.7V$ to $3.0V$				
<b>Speed</b>				
-70 = 70ns (M48Z129Y)				
-85 = 85ns (M48Z129V)				
<b>Package</b>				
PM = PMDIP32				
<b>Temperature Range</b>				
1 = 0 to 70 °C				

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

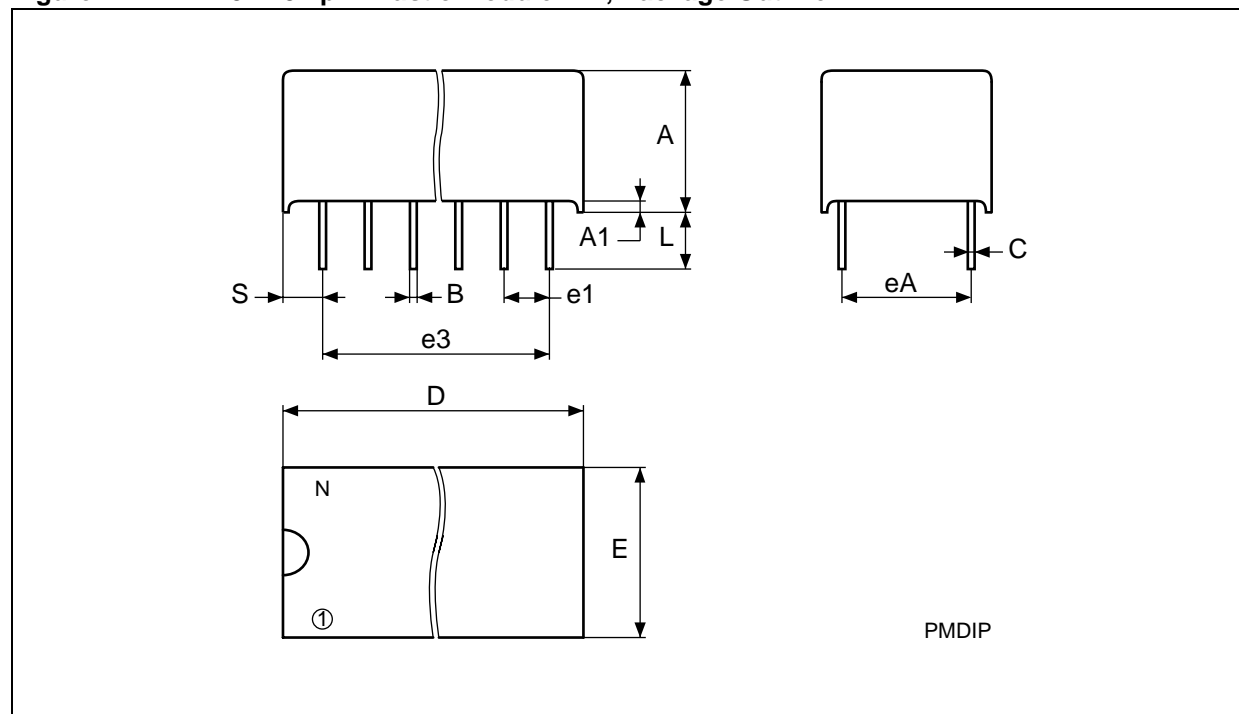
**Table 12. Revision History**

Date	Revision Details
December 1999	First Issue
03/30/00	From Preliminary Data to Data Sheet
06/20/00	t <sub>GLQX</sub> changed for M48Z129Y (Table 9)

Table 13. PMDIP32 - 32 pin Plastic Module DIP, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		9.27	9.52		0.365	0.375
A1		0.38	–		0.015	–
B		0.43	0.59		0.017	0.023
C		0.20	0.33		0.008	0.013
D		42.42	43.18		1.670	1.700
E		18.03	18.80		0.710	0.740
e1		2.29	2.79		0.090	0.110
e3		34.29	41.91		1.350	1.650
eA		14.99	16.00		0.590	0.630
L		3.05	3.81		0.120	0.150
S		1.91	2.79		0.075	0.110
N		32			32	

Figure 11. PMDIP32 - 32 pin Plastic Module DIP, Package Outline



Drawing is not to scale.

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