

16 Mb (2Mb x 8) ZEROPOWER[®] SRAM

- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERIES
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGES (V_{PFD} = Power-fail Deselect Voltage):
 - M48Z2M1: $4.5V \leq V_{PFD} \leq 4.75V$
 - M48Z2M1Y: $4.2V \leq V_{PFD} \leq 4.50V$
- BATTERIES ARE INTERNALLY ISOLATED UNTIL POWER IS APPLIED
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 2Mb x 8 SRAMs

DESCRIPTION

The M48Z2M1/2M1Y ZEROPOWER[®] RAM is a non-volatile 16,777,216 bit Static RAM organized as 2,097,152 words by 8 bits. The device combines two internal lithium batteries, CMOS SRAMs and a control circuit in a plastic 36 pin DIP long Module.

The ZEROPOWER RAM replaces industry standard SRAMs. It provides the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

Table 1. Signal Names

| | |
|-----------|-----------------------|
| A0-A20 | Address Inputs |
| DQ0-DQ7 | Data Inputs / Outputs |
| \bar{E} | Chip Enable |
| \bar{G} | Output Enable |
| \bar{W} | Write Enable |
| V_{CC} | Supply Voltage |
| V_{SS} | Ground |

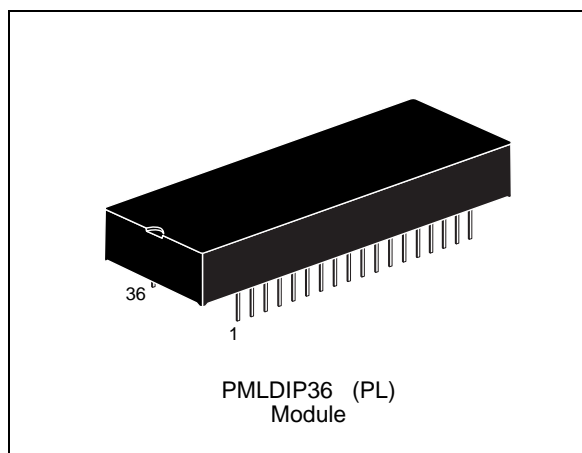
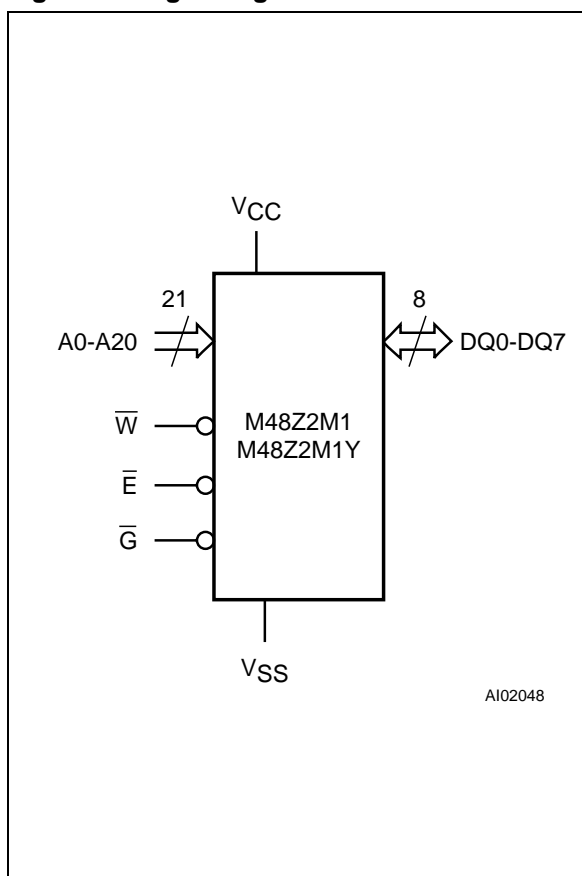


Figure 1. Logic Diagram



M48Z2M1, M48Z2M1Y

Table 2. Absolute Maximum Ratings ⁽¹⁾

| Symbol | Parameter | Value | Unit |
|---------------------------------|---|-----------|------|
| T _A | Ambient Operating Temperature | 0 to 70 | °C |
| T _{STG} | Storage Temperature (V _{CC} Off) | -40 to 85 | °C |
| T _{BIAS} | Temperature Under Bias | -40 to 85 | °C |
| T _{SLD} ⁽²⁾ | Lead Soldering Temperature for 10 seconds | 260 | °C |
| V _{IO} | Input or Output Voltages | -0.3 to 7 | V |
| V _{CC} | Supply Voltage | -0.3 to 7 | V |

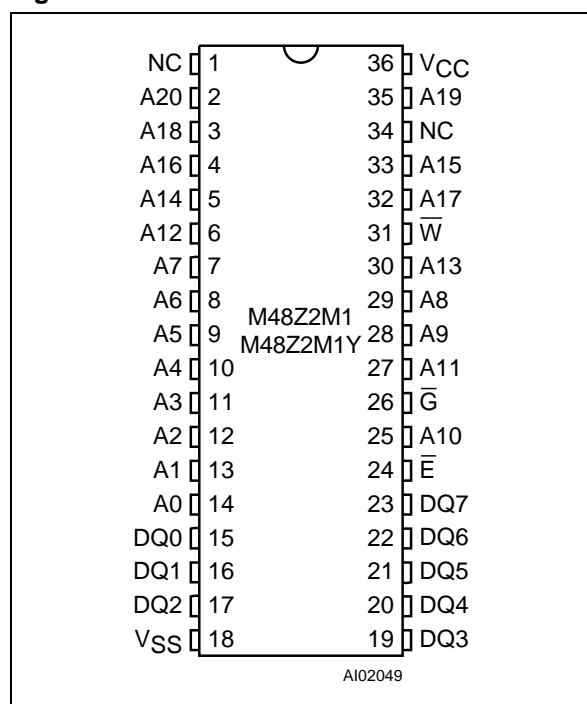
Notes: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.
2. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).
CAUTION: Negative undershoots below -0.3 volts are not allowed on any pin while in the Battery Back-up mode.

Table 3. Operating Modes

| Mode | V _{CC} | \bar{E} | \bar{G} | \bar{W} | DQ0-DQ7 | Power |
|----------|--|-----------------|-----------------|-----------------|------------------|----------------------|
| Deselect | 4.75V to 5.5V or 4.5V to 5.5V | V _{IH} | X | X | High Z | Standby |
| Write | | V _{IL} | X | V _{IL} | D _{IN} | Active |
| Read | | V _{IL} | V _{IL} | V _{IH} | D _{OUT} | Active |
| Read | | V _{IL} | V _{IH} | V _{IH} | High Z | Active |
| Deselect | V _{SO} to V _{PF} D (min) | X | X | X | High Z | CMOS Standby |
| Deselect | ≤ V _{SO} | X | X | X | High Z | Battery Back-up Mode |

Notes: X = V_{IH} or V_{IL}; V_{SO} = Battery Back-up Switchover Voltage.

Figure 2. DIP Pin Connections



Warning: NC = Not Connected.

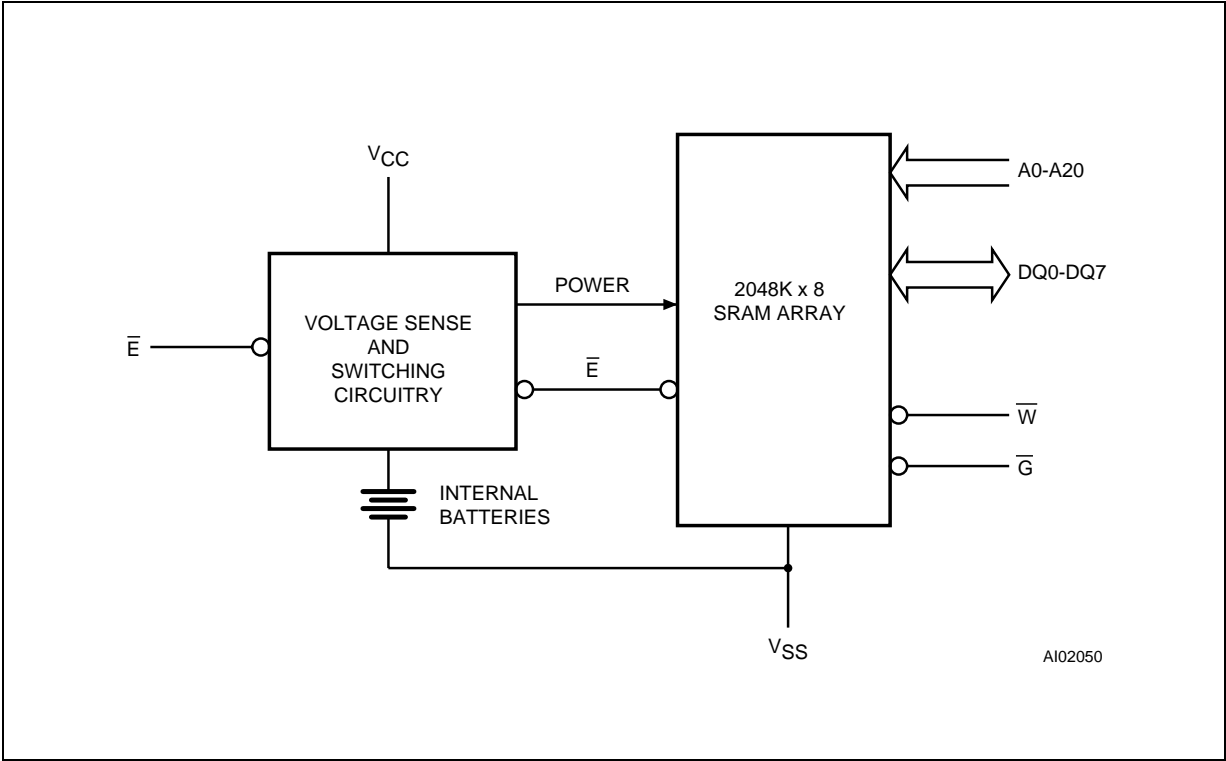
DESCRIPTION (cont'd)

The M48Z2M1/2M1Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the batteries which sustain data until valid power returns.

READ MODE

The M48Z2M1/2M1Y is in the Read Mode whenever \bar{W} (Write Enable) is high and \bar{E} (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 16,777,216 locations in the static storage array. Thus, the unique address specified by the 21 Address Inputs defines which one of the 2,097,152 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within Address Access time (t_{AVQV}) after the last address input signal is stable, providing that the \bar{E} (Chip Enable) and \bar{G} (Output Enable) access times are also satisfied. If the \bar{E} and \bar{G} access times are not met, valid data will be avail-

Figure 3. Block Diagram



able after the later of Chip Enable Access time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}). The state of the eight three-state Data I/O signals is controlled by \bar{E} and \bar{G} . If the outputs are activated before t_{AVQV} , the data lines will be driven to an indeterminate state until t_{AVQV} . If the Address Inputs are changed while \bar{E} and \bar{G} remain low, output data will remain valid for Output Data Hold time (t_{AXQX}) but will go indeterminate until the next Address Access.

WRITE MODE

The M48Z2M1/2M1Y is in the Write Mode whenever \bar{W} and \bar{E} are active. The start of a write is referenced from the latter occurring falling edge of \bar{W} or \bar{E} . A write is terminated by the earlier rising edge of \bar{W} or \bar{E} .

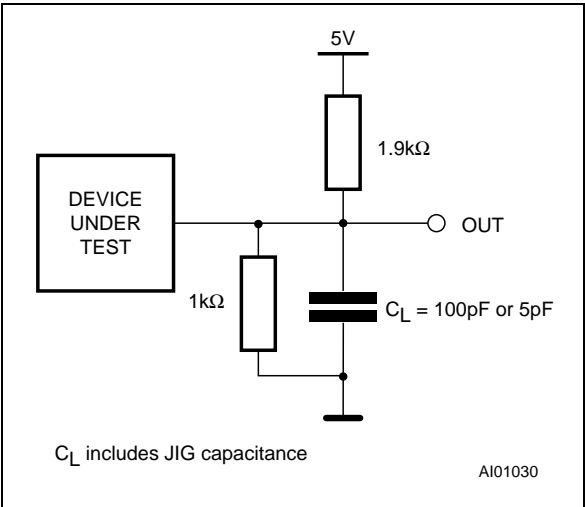
The addresses must be held valid throughout the cycle. \bar{E} or \bar{W} must return high for minimum of t_{EHAX} from \bar{E} or t_{WHAX} from \bar{W} prior to the initiation of another read or write cycle. Data-in must be valid t_{DVEH} or t_{DVWH} prior to the end of write and remain valid for t_{EHDX} or t_{WHDX} afterward. \bar{G} should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on \bar{E} and \bar{G} , a low on \bar{W} will disable the outputs t_{WLQZ} after \bar{W} falls.

Table 4. AC Measurement Conditions

| | |
|---------------------------------------|-------------------|
| Input Rise and Fall Times | $\leq 5\text{ns}$ |
| Input Pulse Voltages | 0 to 3V |
| Input and Output Timing Ref. Voltages | 1.5V |

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit



M48Z2M1, M48Z2M1Y

Table 5. Capacitance ^(1, 2)
($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|----------------|----------------------------|----------------|-----|-----|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0V$ | | 40 | pF |
| $C_{IO}^{(3)}$ | Input / Output Capacitance | $V_{OUT} = 0V$ | | 40 | pF |

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 6. DC Characteristics
($T_A = 0$ to 70°C ; $V_{CC} = 4.75V$ to $5.5V$ or $4.5V$ to $5.5V$)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|----------------|-------------------------------|-----------------------------------|------|----------------|---------|
| $I_{LI}^{(1)}$ | Input Leakage Current | $0V \leq V_{IN} \leq V_{CC}$ | | ± 4 | μA |
| $I_{LO}^{(1)}$ | Output Leakage Current | $0V \leq V_{OUT} \leq V_{CC}$ | | ± 4 | μA |
| I_{CC} | Supply Current | $\bar{E} = V_{IL}$, Outputs open | | 140 | mA |
| I_{CC1} | Supply Current (Standby) TTL | $\bar{E} = V_{IH}$ | | 10 | mA |
| I_{CC2} | Supply Current (Standby) CMOS | $\bar{E} \geq V_{CC} - 0.2V$ | | 8 | mA |
| V_{IL} | Input Low Voltage | | -0.3 | 0.8 | V |
| V_{IH} | Input High Voltage | | 2.2 | $V_{CC} + 0.3$ | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1mA$ | | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -1mA$ | 2.4 | | V |

Note: 1. Outputs deselected.

Table 7. Power Down/Up Trip Points DC Characteristics ⁽¹⁾
($T_A = 0$ to 70°C)

| Symbol | Parameter | Min | Typ | Max | Unit |
|----------------|--|-----|-----|------|-------|
| V_{PFD} | Power-fail Deselect Voltage (M48Z2M1) | 4.5 | 4.6 | 4.75 | V |
| V_{PFD} | Power-fail Deselect Voltage (M48Z2M1Y) | 4.2 | 4.3 | 4.5 | V |
| V_{SO} | Battery Back-up Switchover Voltage | | 3 | | V |
| $t_{DR}^{(2)}$ | Data Retention Time | 10 | | | YEARS |

Notes: 1. All voltages referenced to V_{SS} .
2. At 25°C

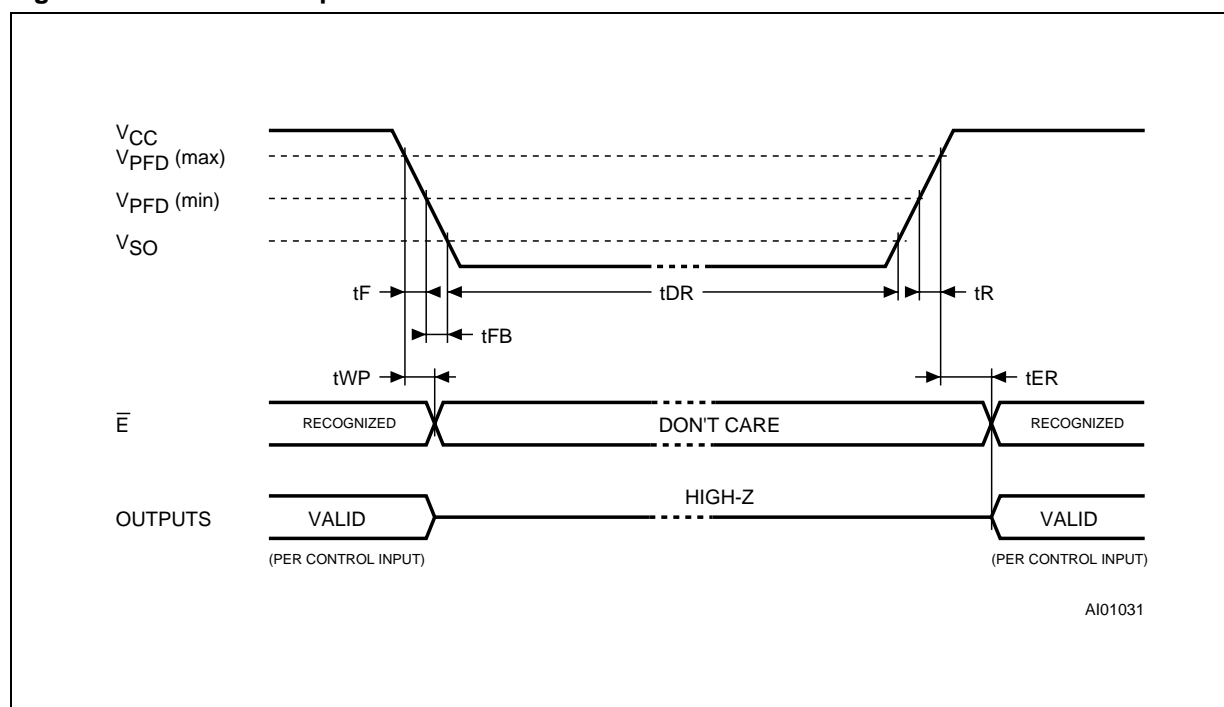
Table 8. Power Down/Up Mode AC Characteristics
 ($T_A = 0$ to 70°C)

| Symbol | Parameter | Min | Max | Unit |
|----------------|---|-----|-----|---------------|
| $t_F^{(1)}$ | $V_{PFD}(\text{max})$ to $V_{PFD}(\text{min})$ V_{CC} Fall Time | 300 | | μs |
| $t_{FB}^{(2)}$ | $V_{PFD}(\text{min})$ to V_{SO} V_{CC} Fall Time | 10 | | μs |
| t_{WP} | Write Protect Time from $V_{CC} = V_{PFD}$ | 40 | 150 | μs |
| t_R | V_{SO} to $V_{PFD}(\text{max})$ V_{CC} Rise Time | 0 | | μs |
| t_{ER} | \bar{E} Recovery Time | 40 | 120 | ms |

Notes: 1. $V_{PFD}(\text{max})$ to $V_{PFD}(\text{min})$ fall time of less than t_F may result in deselection/write protection not occurring until $200\text{ }\mu\text{s}$ after V_{CC} passes $V_{PFD}(\text{min})$.

2. $V_{PFD}(\text{min})$ to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms



M48Z2M1, M48Z2M1Y

Table 9. Read Mode AC Characteristics

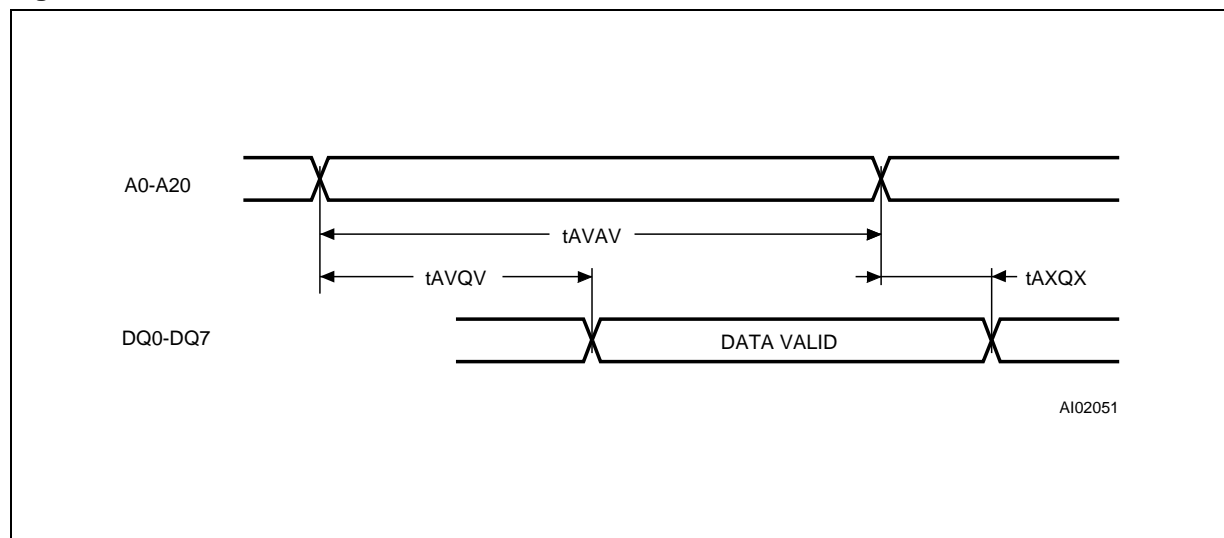
($T_A = 0$ to 70°C ; $V_{CC} = 4.75\text{V}$ to 5.5V or 4.5V to 5.5V)

| Symbol | Parameter | M48Z2M1 / M48Z2M1Y | | Unit |
|----------------------------------|---|--------------------|-----|------|
| | | -70 | | |
| | | Min | Max | |
| t _{AVAV} | Read Cycle Time | 70 | | ns |
| t _{AVQV} ⁽¹⁾ | Address Valid to Output Valid | | 70 | ns |
| t _{ELQV} ⁽¹⁾ | Chip Enable Low to Output Valid | | 70 | ns |
| t _{GLQV} ⁽¹⁾ | Output Enable Low to Output Valid | | 35 | ns |
| t _{ELQX} ⁽²⁾ | Chip Enable Low to Output Transition | 5 | | ns |
| t _{GLQX} ⁽²⁾ | Output Enable Low to Output Transition | 5 | | ns |
| t _{EHQZ} ⁽²⁾ | Chip Enable High to Output Hi-Z | | 30 | ns |
| t _{GHQZ} ⁽²⁾ | Output Enable High to Output Hi-Z | | 25 | ns |
| t _{AXQX} ⁽¹⁾ | Address Transition to Output Transition | 5 | | ns |

Notes: 1. $C_L = 100\text{pF}$ (see Figure 4).

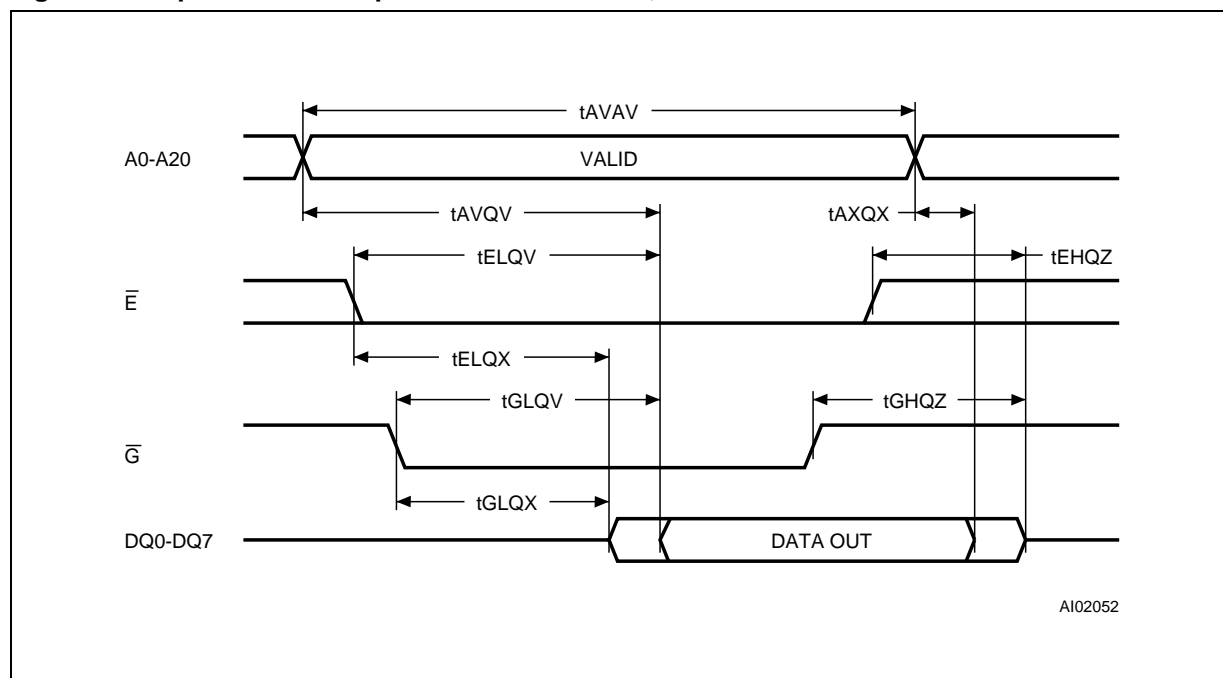
2. $C_L = 5\text{pF}$ (see Figure 4)

Figure 6. Address Controlled, Read Mode AC Waveforms



Note: Chip Enable (\overline{E}) and Output Enable (\overline{G}) = Low, Write Enable (\overline{W}) = High.

Figure 7. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: Write Enable (\overline{W}) = High.

DATA RETENTION MODE

With valid V_{CC} applied, the M48Z2M1/2M1Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD} . All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP} , write protection takes place. When V_{CC} drops be-

low V_{SO} , the control circuit switches power to the internal energy source which preserves data.

The internal coin cells will maintain data in the M48Z2M1/2M1Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO} . As system power returns and V_{CC} rises above V_{SO} , the batteries are disconnected, and the power supply is switched to external V_{CC} . Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER} , normal RAM operation can resume.

For more information on Battery Storage life refer to the Application Note AN1012.

Table 10. Write Mode AC Characteristics
 $(T_A = 0 \text{ to } 70^\circ\text{C}; V_{CC} = 4.75\text{V to } 5.5\text{V or } 4.5\text{V to } 5.5\text{V})$

| Symbol | Parameter | M48Z2M1 / M48Z2M1Y | | Unit |
|------------------------------------|---|--------------------|-----|------|
| | | -70 | | |
| | | Min | Max | |
| t _{AVAV} | Write Cycle Time | 70 | | ns |
| t _{AVWL} | Address Valid to Write Enable Low | 0 | | ns |
| t _{AVEL} | Address Valid to Chip Enable Low | 0 | | ns |
| t _{WLWH} | Write Enable Pulse Width | 55 | | ns |
| t _{ELEH} | Chip Enable Low to Chip Enable High | 55 | | ns |
| t _{WHAX} | Write Enable High to Address Transition | 5 | | ns |
| t _{EHAX} | Chip Enable High to Address Transition | 15 | | ns |
| t _{DVWH} | Input Valid to Write Enable High | 30 | | ns |
| t _{DVEH} | Input Valid to Chip Enable High | 30 | | ns |
| t _{WHDX} | Write Enable High to Input Transition | 0 | | ns |
| t _{EHDX} | Chip Enable High to Input Transition | 10 | | ns |
| t _{WLQZ} ^(1,2) | Write Enable Low to Output Hi-Z | | 25 | ns |
| t _{AVWH} | Address Valid to Write Enable High | 65 | | ns |
| t _{AVEH} | Address Valid to Chip Enable High | 65 | | ns |
| t _{WHQX} ^(1,2) | Write Enable High to Output Transition | 5 | | ns |

Notes: 1. $C_L = 5\text{pF}$ (see Figure 4).

2. If E goes low simultaneously with W going low, the outputs remain in the high-impedance state.

POWER SUPPLY DECOUPLING and UNDER-SHOOT PROTECTION

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy, which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A bypass capacitor value of $0.1\mu\text{F}$ (as shown in Figure 8) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one Volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC} , anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

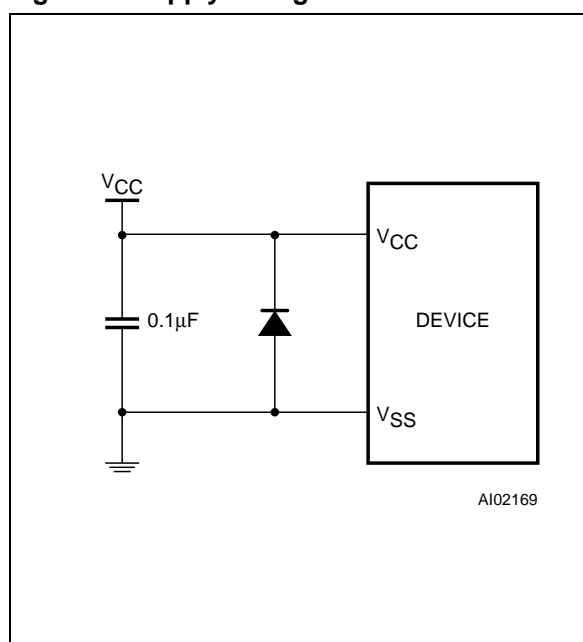
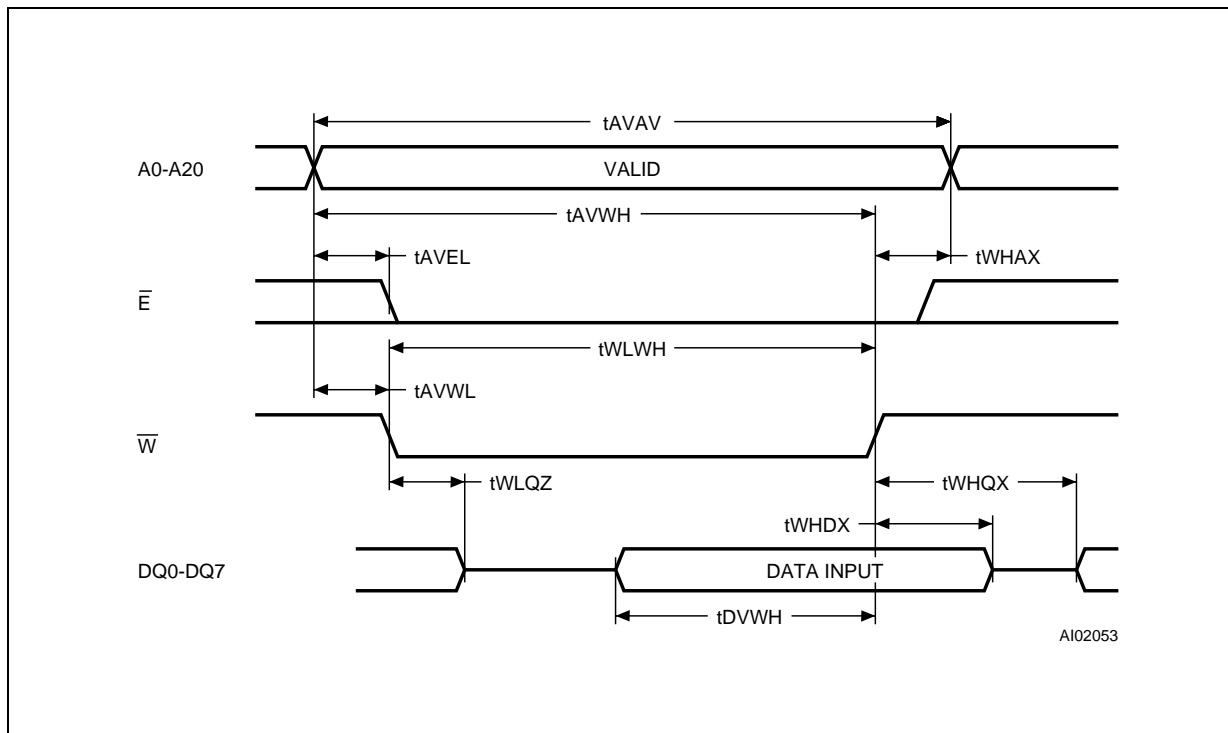
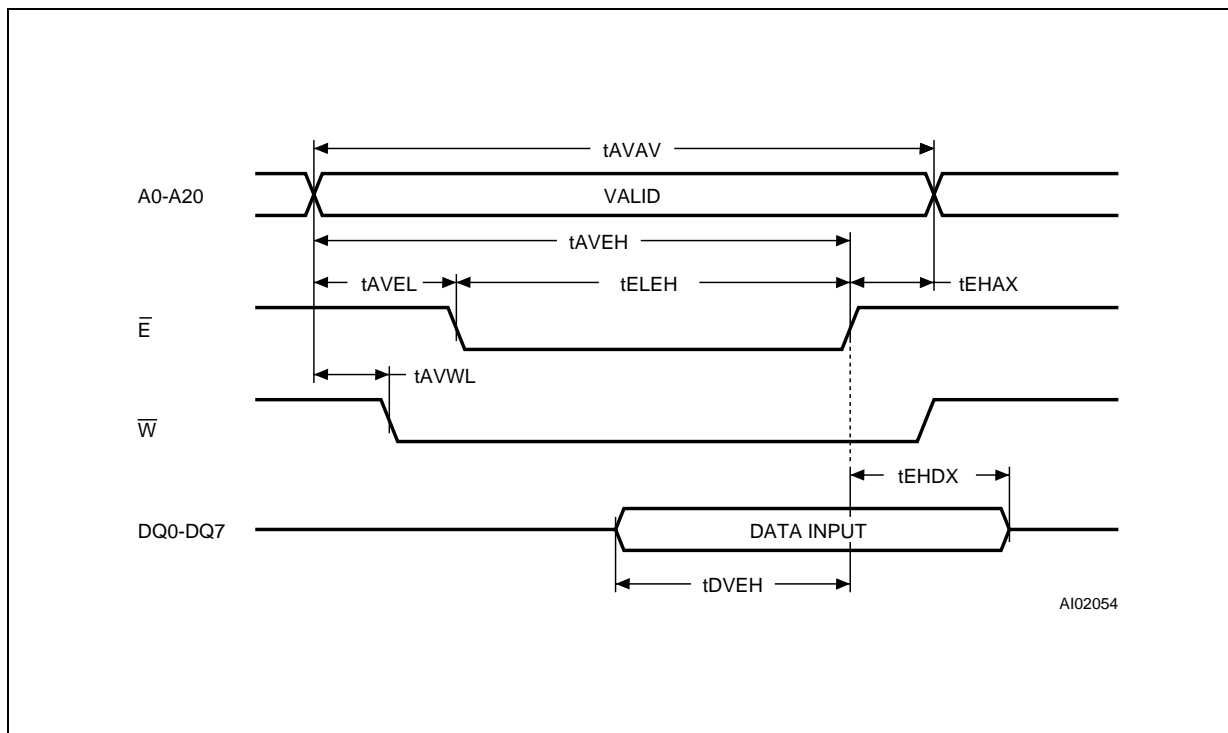
Figure 8. Supply Voltage Protection


Figure 9. Write Enable Controlled, Write AC Waveforms



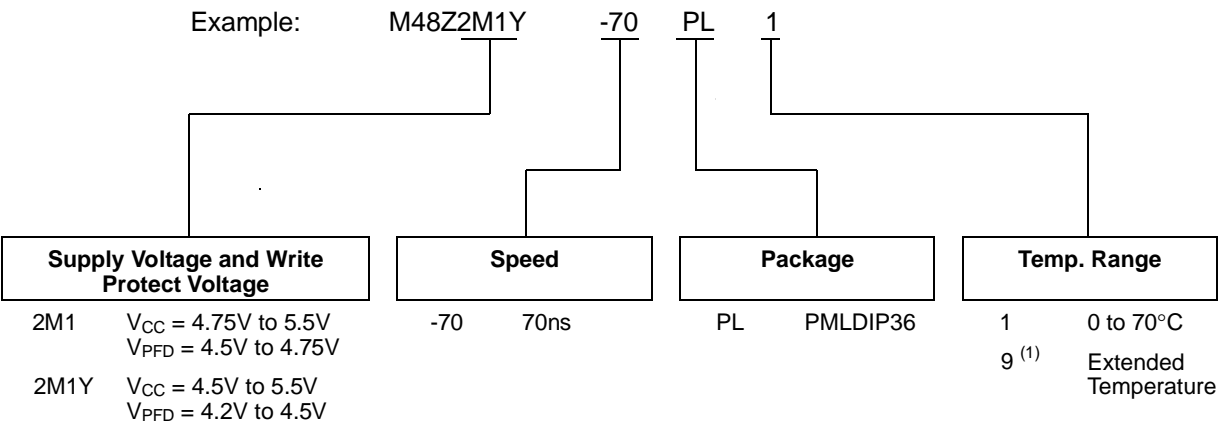
Note: Output Enable (\overline{G}) = High.

Figure 10. Chip Enable Controlled, Write AC Waveforms



Note: Output Enable (\overline{G}) = High.

ORDERING INFORMATION SCHEME



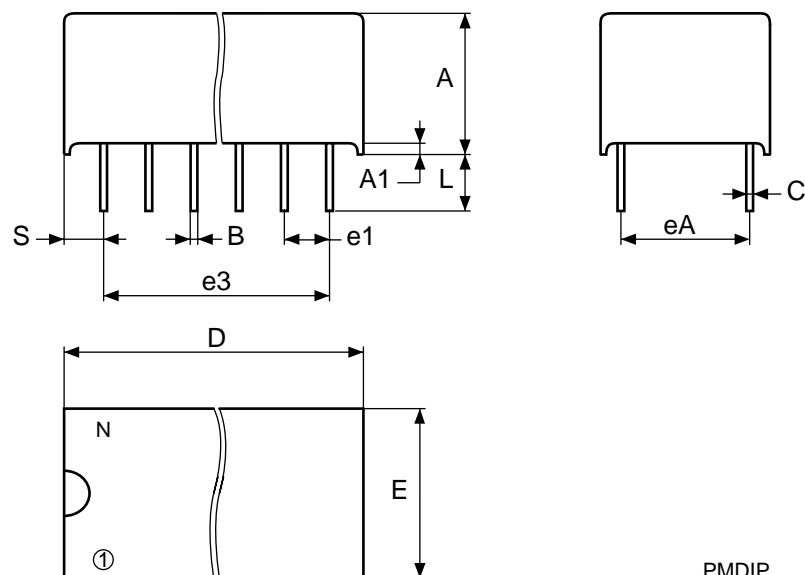
Note: 1. Contact Sales Offices for availability of Extended Temperature.

For a list of available options (Speed, Package, etc.) or for further information or any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PMLDIP36 - 36 pin Plastic DIP Long Module

| Symb | mm | | | inches | | |
|------|-----|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 9.27 | 9.52 | | 0.365 | 0.375 |
| A1 | | 0.38 | – | | 0.015 | – |
| B | | 0.43 | 0.59 | | 0.017 | 0.023 |
| C | | 0.20 | 0.33 | | 0.008 | 0.013 |
| D | | 52.58 | 53.34 | | 2.070 | 2.100 |
| E | | 18.03 | 18.80 | | 0.710 | 0.740 |
| e1 | | 2.30 | 2.81 | | 0.090 | 0.110 |
| e3 | | 38.86 | 47.50 | | 1.530 | 1.870 |
| eA | | 14.99 | 16.00 | | 0.590 | 0.630 |
| L | | 3.05 | 3.81 | | 0.120 | 0.150 |
| S | | 4.45 | 5.33 | | 0.175 | 0.210 |
| N | | 36 | | | 36 | |

PMLDIP36



PMDIP

Drawing is not to scale.

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