

## CMOS 32K x 8 ZEROPOWER SRAM

- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 32K x 8 SRAMs
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z30:  $4.5V \leq V_{PFD} \leq 4.75V$
  - M48Z30Y:  $4.2V \leq V_{PFD} \leq 4.50V$
- BATTERY INTERNALLY ISOLATED UNTIL POWER IS APPLIED

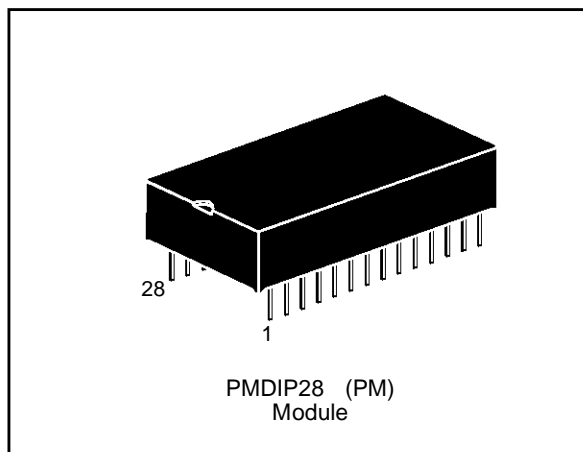
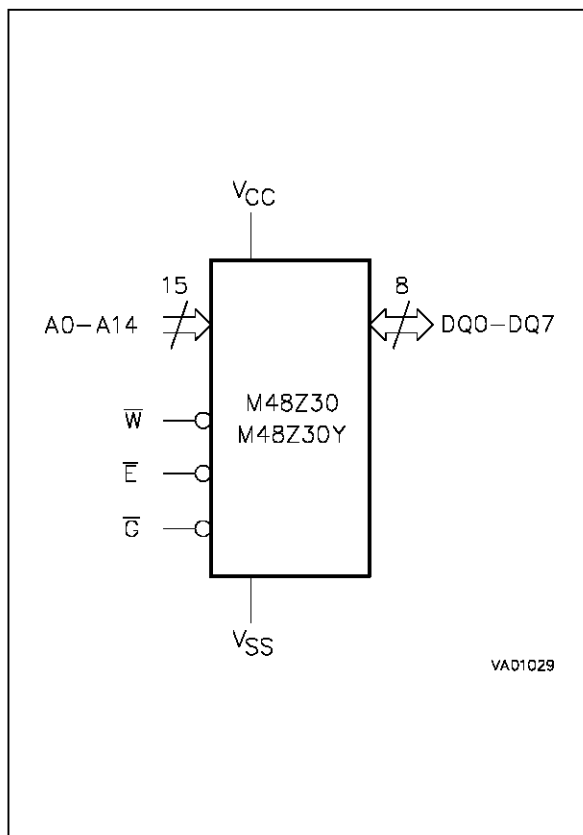


Figure 1. Logic Diagram



### DESCRIPTION

The M48Z30/30Y 32K x 8 ZEROPOWER® RAM is a non-volatile 262,144 bit Static RAM organized as 32,768 words by 8 bits. The device combines an internal lithium battery and a full CMOS SRAM in a plastic 28 pin DIP Module. The ZEROPOWER

Table 1. Signal Names

A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
$\bar{W}$	Write Enable
V <sub>CC</sub>	Supply Voltage
V <sub>SS</sub>	Ground

**Table 2. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
T <sub>A</sub>	Ambient Operating Temperature	0 to 70	°C
T <sub>STG</sub>	Storage Temperature (V <sub>CC</sub> Off)	–40 to 70	°C
T <sub>BIAS</sub>	Temperature Under Bias	–10 to 70	°C
T <sub>SLD</sub>	Lead Soldering Temperature for 10 seconds	260	°C
V <sub>IO</sub>	Input or Output Voltages	–0.3 to 7	V
V <sub>CC</sub>	Supply Voltage	–0.3 to 7	V

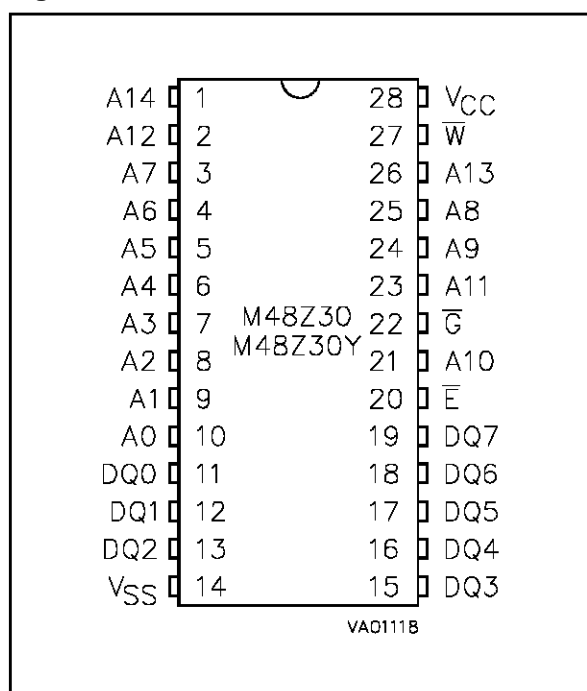
**Note:** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

**CAUTION:** Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.

**Table 3. Operating Modes**

Mode	V <sub>CC</sub>	$\bar{E}$	$\bar{G}$	$\bar{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V <sub>IH</sub>	X	X	High Z	Standby
Write		V <sub>IL</sub>	X	V <sub>IL</sub>	D <sub>IN</sub>	Active
Read		V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>	Active
Read		V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	High Z	Active
Deselect	V <sub>SO</sub> to V <sub>PF</sub> D (min)	X	X	X	High Z	CMOS Standby
Deselect	≤ V <sub>SO</sub>	X	X	X	High Z	Battery Back-up Mode

**Note:** X = V<sub>IH</sub> or V<sub>IL</sub>

**Figure 2. DIP Pin Connections**

**DESCRIPTION (cont'd)**

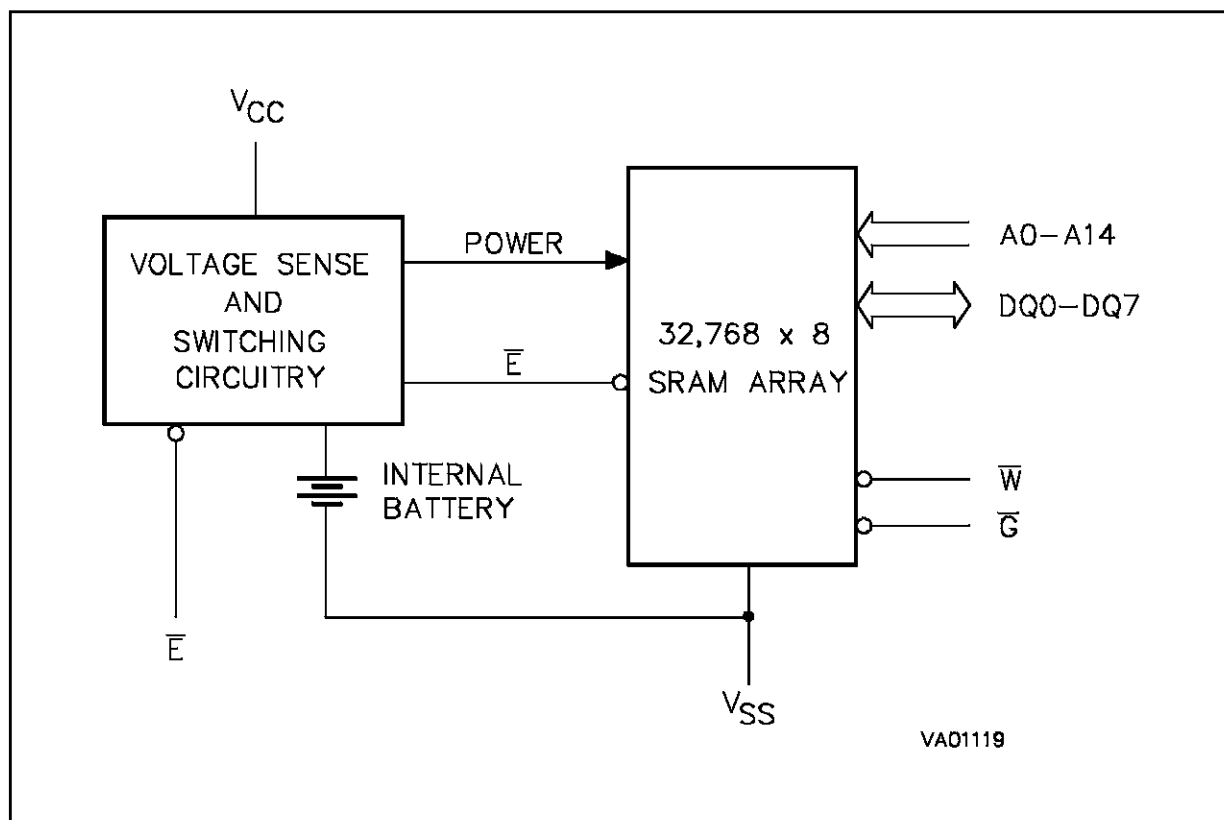
RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z30/30Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V<sub>CC</sub> is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V<sub>CC</sub>. As V<sub>CC</sub> falls below approximately 3V, the control circuitry connects the battery which sustains data until valid power returns.

**READ MODE**

The M48Z30/30Y is in the Read Mode whenever  $\bar{W}$  (Write Enable) is high and  $\bar{E}$  (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address

Figure 3. Block Diagram



specified by the 15 Address Inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within  $t_{AVQV}$  (Address Access Time) after the last address input signal is stable, providing that the  $\overline{E}$  and  $\overline{G}$  (Output Enable) access times are also satisfied. If the  $\overline{E}$  and  $\overline{G}$  access times are not met, valid data will be available after the later of Chip Enable Access Time ( $t_{ELQV}$ ) or Output Enable Access Time ( $t_{GLQV}$ ).

The state of the eight three-state Data I/O signals is controlled by  $\overline{E}$  and  $\overline{G}$ . If the outputs are activated before  $t_{AVQV}$ , the data lines will be driven to an indeterminate state until  $t_{AVQV}$ . If the Address Inputs are changed while  $\overline{E}$  and  $\overline{G}$  remain low, output data will remain valid for  $t_{AXQX}$  (Output Data Hold Time) but will go indeterminate until the next Address Access.

### WRITE MODE

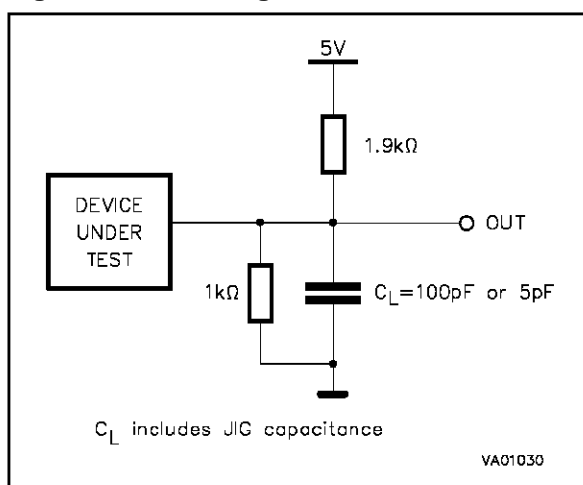
The M48Z30/30Y is in the Write Mode whenever  $\overline{W}$  and  $\overline{E}$  are active. The start of a write is referenced from the latter occurring falling edge of  $\overline{W}$  or  $\overline{E}$ .

### AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	$\leq 5\text{ns}$
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit



**Table 4. Capacitance** <sup>(1, 2)</sup> ( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

Symbol	Parameter	Test Condition	Min	Max	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$		10	pF
$C_{IO}^{(3)}$	Input / Output Capacitance	$V_{OUT} = 0V$		10	pF

**Notes:** 1. Effective capacitance measured with power supply at 5V.

2. Sampled only, not 100% tested.

3. Outputs deselected

**Table 5. DC Characteristics** ( $T_A = 0\text{ to }70^\circ\text{C}$ ;  $V_{CC} = 4.75V\text{ to }5.5V\text{ or }4.5V\text{ to }5.5V$ )

Symbol	Parameter	Test Condition	Min	Max	Unit
$I_{LI}^{(1)}$	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		$\pm 1$	$\mu A$
$I_{LO}^{(1)}$	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		$\pm 1$	$\mu A$
$I_{CC}$	Supply Current	$\bar{E} = V_{IL}$ , Outputs open		85	mA
$I_{CC1}$	Supply Current (Standby) TTL	$\bar{E} = V_{IH}$		7	mA
$I_{CC2}$	Supply Current (Standby) CMOS	$\bar{E} \geq V_{CC} - 0.2V$		4	mA
$V_{IL}$	Input Low Voltage		-0.3	0.8	V
$V_{IH}$	Input High Voltage		2.2	$V_{CC} + 0.3$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1mA$		0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -1mA$	2.4		V

**Note:** 1. Outputs deselected.

**Table 6. Power Down/Up Trip Points DC Characteristics** <sup>(1)</sup> ( $T_A = 0\text{ to }70^\circ\text{C}$ )

Symbol	Parameter	Min	Typ	Max	Unit
$V_{PFD}$	Power-fail Deselect Voltage (M48Z30)	4.5	4.6	4.75	V
$V_{PFD}$	Power-fail Deselect Voltage (M48Z30Y)	4.2	4.3	4.5	V
$V_{SO}$	Battery Back-up Switchover Voltage		3		V
$t_{DR}^{(2)}$	Data Retention Time	10			YEARS

**Notes:** 1. All voltages referenced to  $V_{SS}$ .

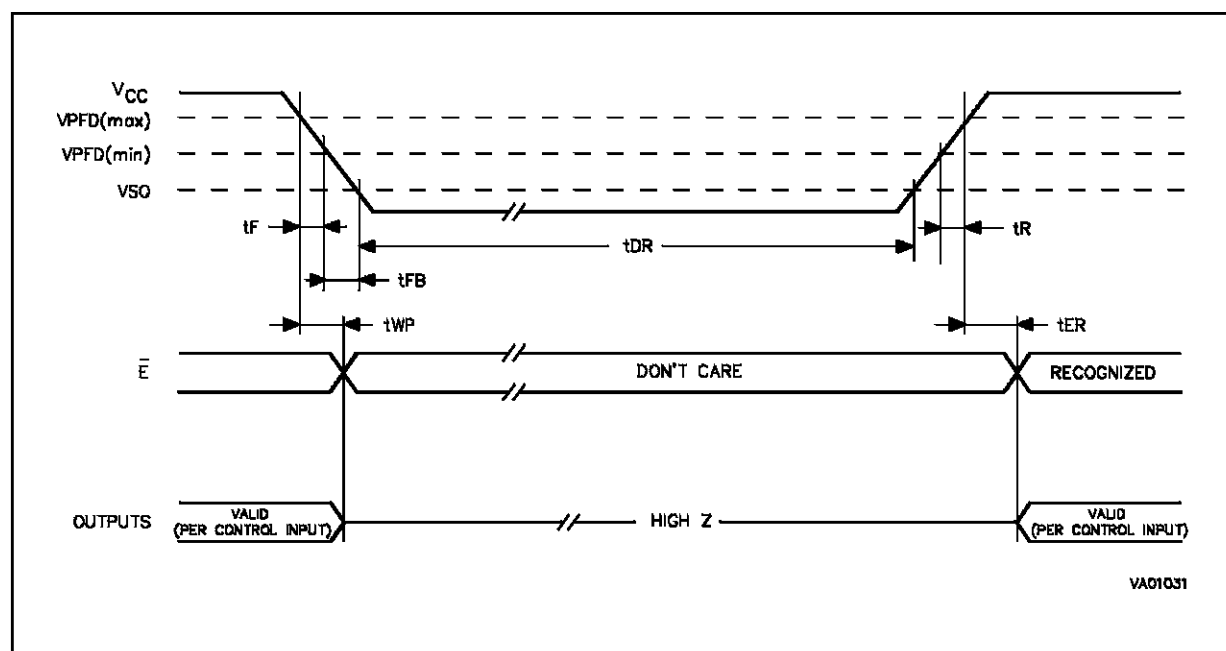
2. @  $25^\circ\text{C}$

**Table 7. Power Down/Up Mode AC Characteristics** ( $T_A = 0$  to  $70^\circ\text{C}$ )

Symbol	Parameter	Min	Max	Unit
$t_F^{(1)}$	$V_{PFD}(\text{max})$ to $V_{PFD}(\text{min})$ $V_{CC}$ Fall Time	300		$\mu\text{s}$
$t_{FB}^{(2)}$	$V_{PFD}(\text{min})$ to $V_{SO}$ $V_{CC}$ Fall Time	10		$\mu\text{s}$
$t_{WP}$	Write Protect Time from $V_{CC} = V_{PFD}$	40	150	$\mu\text{s}$
$t_R$	$V_{SO}$ to $V_{PFD}(\text{max})$ $V_{CC}$ Rise Time	0		$\mu\text{s}$
$t_{ER}$	$\overline{E}$ Recovery Time	40	120	ms

**Notes:** 1.  $V_{PFD}(\text{max})$  to  $V_{PFD}(\text{min})$  fall time of less than  $t_F$  may result in deselection/write protection not occurring until  $200\text{ }\mu\text{s}$  after  $V_{CC}$  passes  $V_{PFD}(\text{min})$ .

2.  $V_{PFD}(\text{min})$  to  $V_{SO}$  fall time of less than  $t_{FB}$  may cause corruption of RAM data.

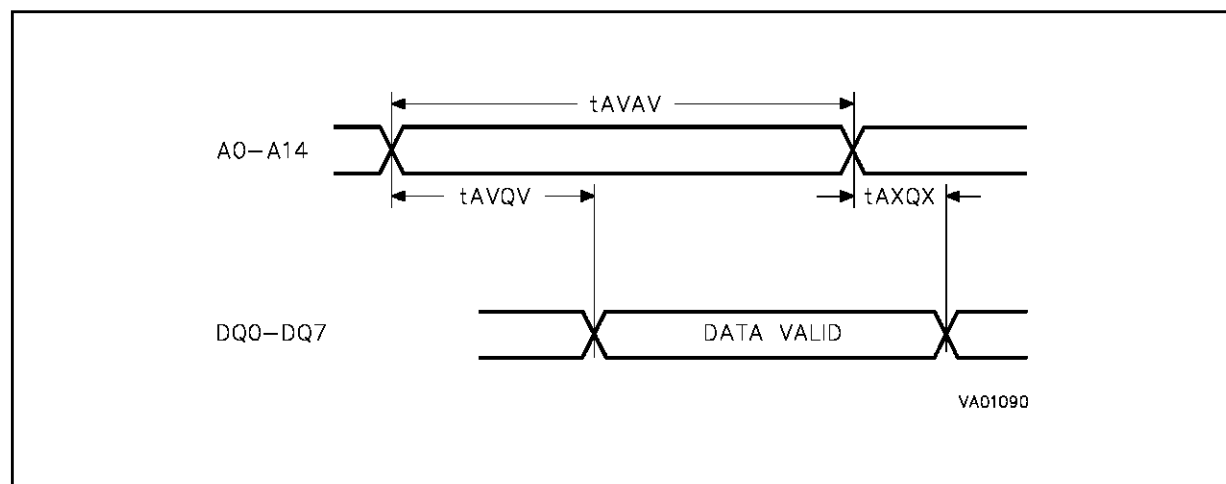
**Figure 5. Power Down/Up Mode AC Waveforms**

**Table 8. Read Mode AC Characteristics** ( $T_A = 0$  to  $70^\circ\text{C}$ ;  $V_{CC} = 4.75\text{V}$  to  $5.5\text{V}$  or  $4.5\text{V}$  to  $5.5\text{V}$ )

Symbol	Parameter	M48Z30 / 30Y				Unit
		-85		-100		
		Min	Max	Min	Max	
t <sub>AVAV</sub>	Read Cycle Time	85		100		ns
t <sub>AVQV</sub> <sup>(1)</sup>	Address Valid to Output Valid		85		100	ns
t <sub>ELQV</sub> <sup>(1)</sup>	Chip Enable Low to Output Valid		85		100	ns
t <sub>GLQV</sub> <sup>(1)</sup>	Output Enable Low to Output Valid		45		50	ns
t <sub>ELQX</sub> <sup>(2)</sup>	Chip Enable Low to Output Transition	5		5		ns
t <sub>GLQX</sub> <sup>(2)</sup>	Output Enable Low to Output Transition	5		5		ns
t <sub>EHQZ</sub> <sup>(2)</sup>	Chip Enable High to Output Hi-Z		40		40	ns
t <sub>GHQZ</sub> <sup>(2)</sup>	Output Enable High to Output Hi-Z		35		35	ns
t <sub>AXQX</sub> <sup>(1)</sup>	Address Transition to Output Transition	10		10		ns

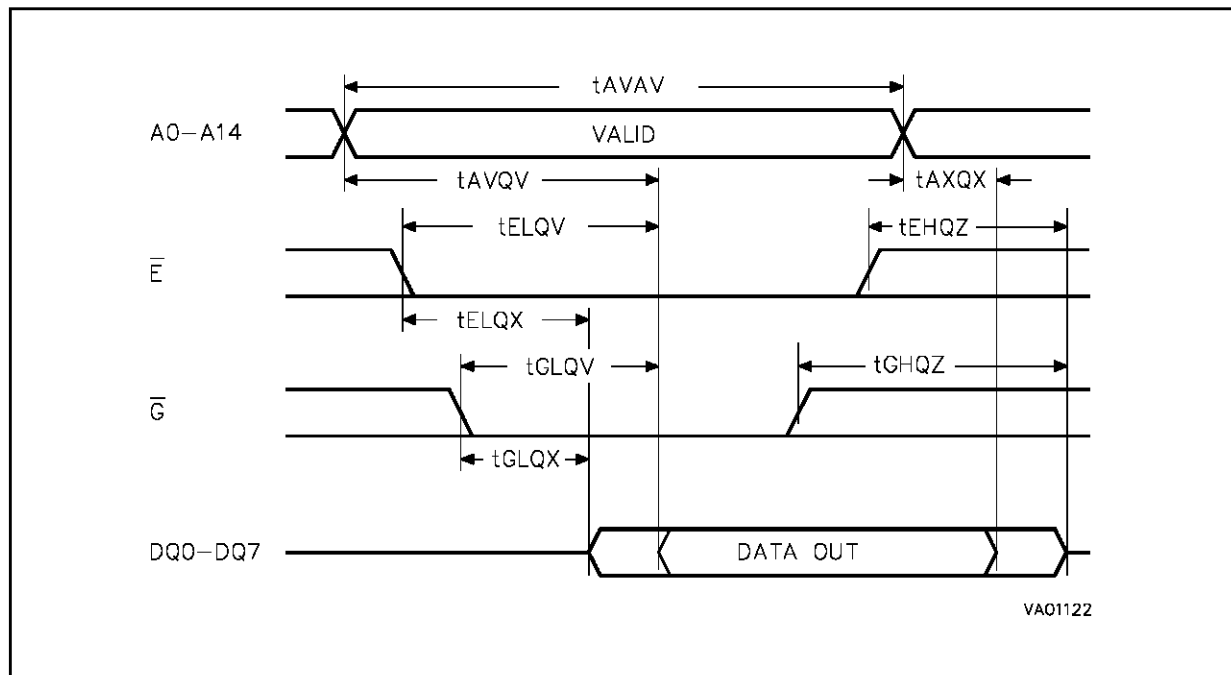
Notes: 1.  $C_L = 100\text{pF}$  (see Figure 4).

2.  $C_L = 5\text{pF}$  (see Figure 4)

**Figure 6. Address Controlled, Read Mode AC Waveforms**


Note:  $\overline{E}$  = Low,  $\overline{G}$  = Low,  $\overline{W}$  = High.

Figure 7. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note:  $\bar{W}$  = High.

### WRITE MODE (cont'd)

A write is terminated by the earlier rising edge of  $\bar{W}$  or  $\bar{E}$ . The addresses must be held valid throughout the cycle.  $\bar{E}$  or  $\bar{W}$  must return high for minimum of  $t_{EHAX}$  from  $\bar{E}$  or  $t_{WHAX}$  from  $\bar{W}$  prior to the initiation of another read or write cycle. Data-in must be valid  $t_{DVWH}$  prior to the end of write and remain valid for  $t_{WHDX}$  or  $t_{EHDX}$  afterward.  $\bar{G}$  should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on  $\bar{E}$  and  $\bar{G}$ , a low on  $\bar{W}$  will disable the outputs  $t_{WLQZ}$  after  $\bar{W}$  falls.

### DATA RETENTION MODE

With valid  $V_{CC}$  applied, the M48Z30/30Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will

automatically power-fail deselect, write protecting itself  $t_{WP}$  after  $V_{CC}$  falls below  $V_{PFD}$ . All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time  $t_{WP}$ , write protection takes place. When  $V_{CC}$  drops below  $V_{SO}$ , the control circuit switches power to the internal energy source which preserves data.

The internal coin cell will maintain data in the M48Z30/30Y after the initial application of  $V_{CC}$  for an accumulated period of at least 10 years when  $V_{CC}$  is less than  $V_{SO}$ . As system power returns and  $V_{CC}$  rises above  $V_{SO}$ , the battery is disconnected, and the power supply is switched to external  $V_{CC}$ . Write protection continues for  $t_{ER}$  after  $V_{CC}$  reaches  $V_{PFD}$  to allow for processor stabilization. After  $t_{ER}$ , normal RAM operation can resume.

**Table 9. Write Mode AC Characteristics** ( $T_A = 0$  to  $70^\circ\text{C}$ ;  $V_{CC} = 4.75\text{V}$  to  $5.5\text{V}$  or  $4.5\text{V}$  to  $5.5\text{V}$ )

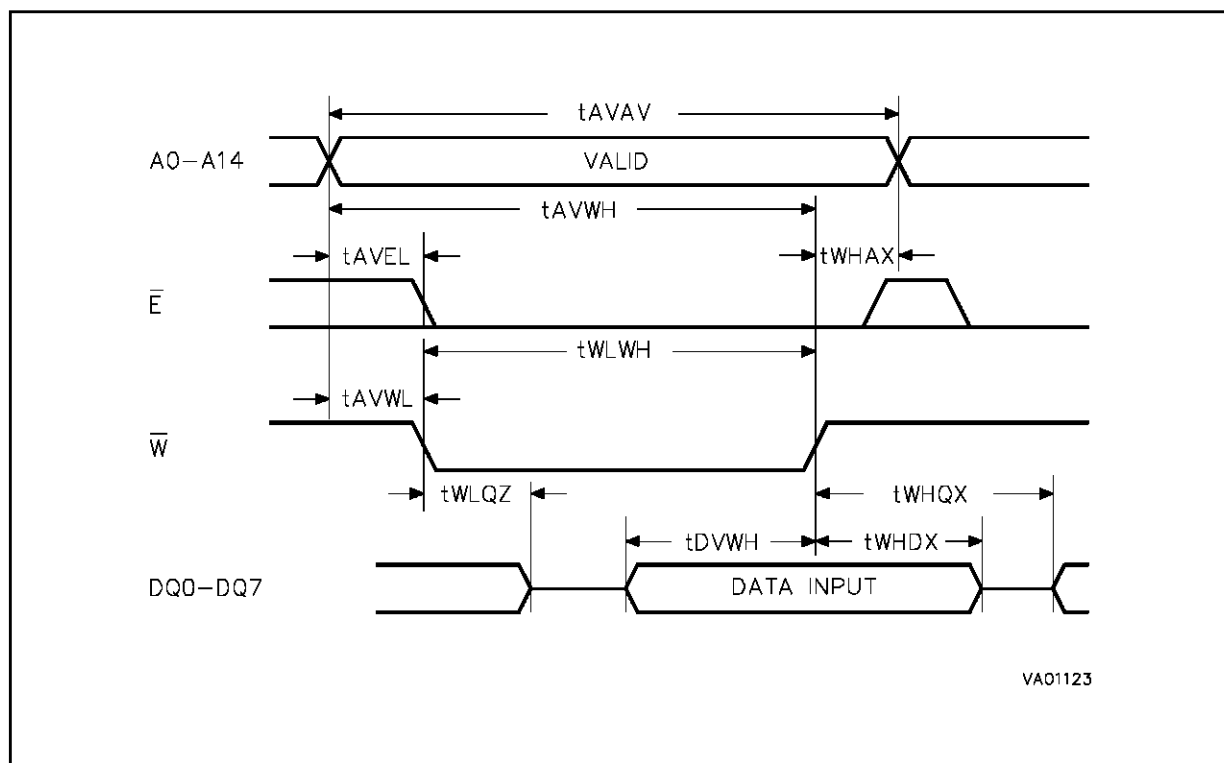
Symbol	Parameter	M48Z30 / 30Y				Unit
		-85		-100		
		Min	Max	Min	Max	
t <sub>AVAV</sub>	Write Cycle Time	85		100		ns
t <sub>AVWL</sub>	Address Valid to Write Enable Low	0		0		ns
t <sub>AVEL</sub>	Address Valid to Chip Enable Low	0		0		ns
t <sub>WLWH</sub>	Write Enable Pulse Width	65		75		ns
t <sub>ELEH</sub>	Chip Enable Low to Chip Enable High	75		90		ns
t <sub>WHAX</sub>	Write Enable High to Address Transition	5		5		ns
t <sub>EHAX</sub>	Chip Enable High to Address Transition	15		15		ns
t <sub>DVWH</sub>	Input Valid to Write Enable High	35		40		ns
t <sub>DVEH</sub>	Input Valid to Chip Enable High	35		40		ns
t <sub>WHDX</sub>	Write Enable High to Input Transition	0		0		ns
t <sub>EHDX</sub>	Chip Enable High to Input Transition	15		15		ns
t <sub>WLQZ</sub> <sup>(1,2)</sup>	Write Enable Low to Output Hi-Z		35		35	ns
t <sub>AVWH</sub>	Address Valid to Write Enable High	75		80		ns
t <sub>AVEH</sub>	Address Valid to Chip Enable High	75		80		ns
t <sub>WHQX</sub> <sup>(1,2)</sup>	Write Enable High to Output Transition	5		5		ns

Notes: 1.  $C_L = 5\text{pF}$  (see Figure 4).

2. If  $\overline{E}$  goes low simultaneously with  $\overline{W}$  going low after  $\overline{W}$  going low, the outputs remain in the high-impedance state.

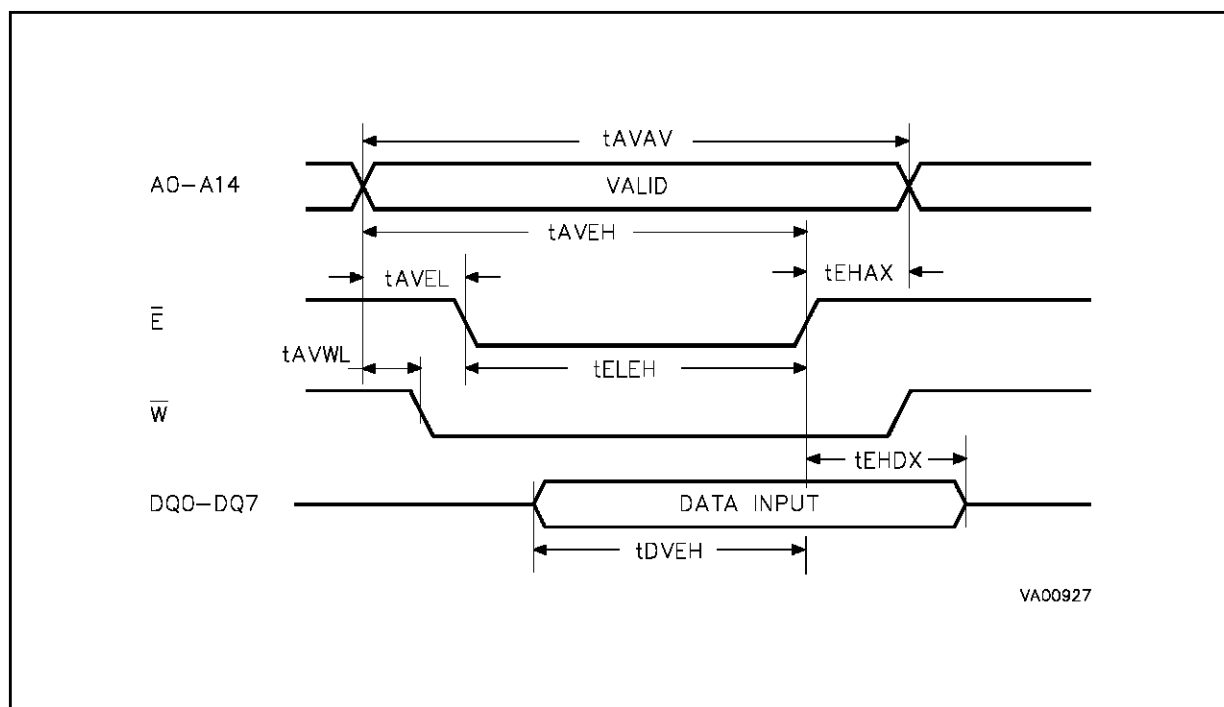


Figure 8. Write Enable Controlled, Write AC Waveforms



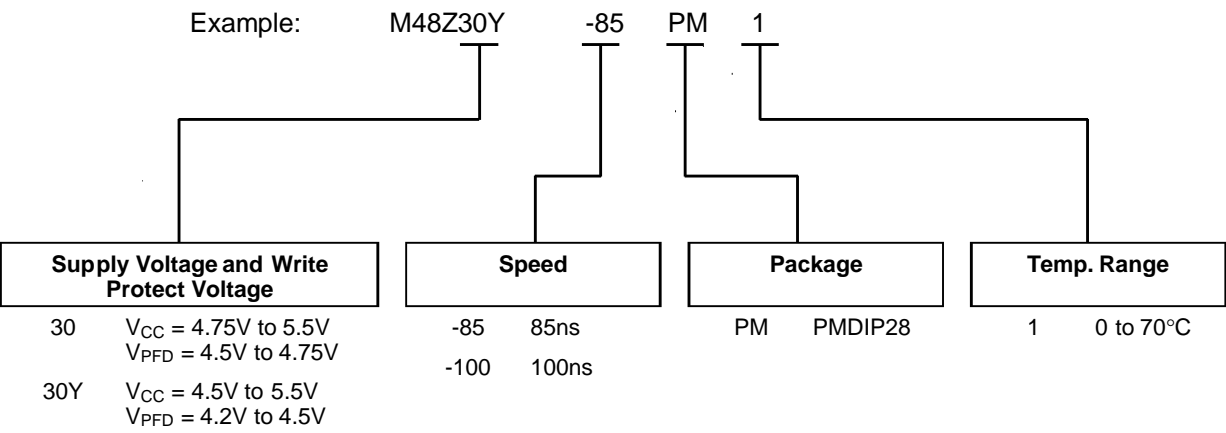
Note:  $\overline{G}$  = High.

Figure 9. Chip Enable Controlled, Write AC Waveforms



Note:  $\overline{G}$  = High.

ORDERING INFORMATION SCHEME



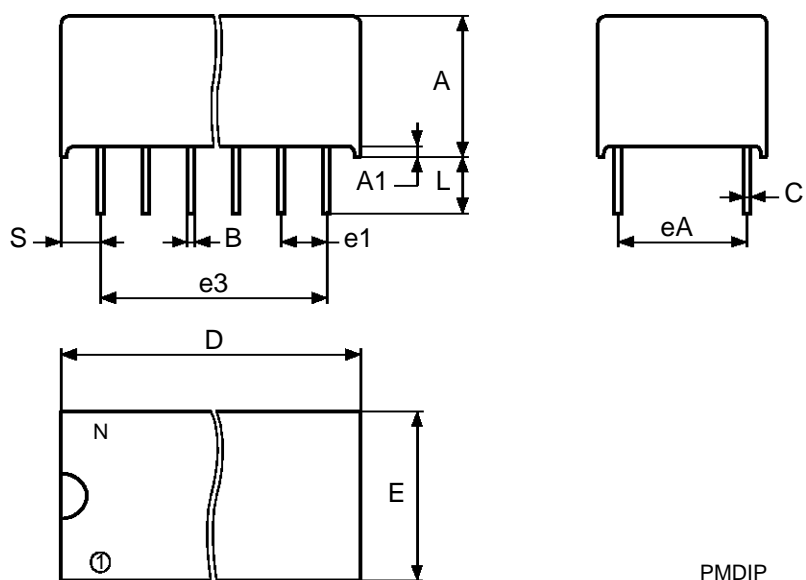
For a list of available options (Package and Speed) refer to the current Memory Shortform catalogue.

For further information or any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

# PMDIP28 - 28 pin Plastic DIP Module

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		9.27	9.52		0.365	0.375
A1		0.38	–		0.015	–
B		0.43	0.59		0.017	0.023
C		0.20	0.33		0.008	0.013
D		37.34	38.10		1.470	1.500
E		18.03	18.80		0.710	0.740
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		14.99	16.00		0.590	0.630
L		3.05	3.81		0.120	0.150
S		1.91	2.79		0.075	0.110
N	28			28		

PMDIP28



Drawing is not to scale

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