



# M48Z35AY M48Z35AV

## 256 Kbit (32Kb x8) ZEROPOWER® SRAM

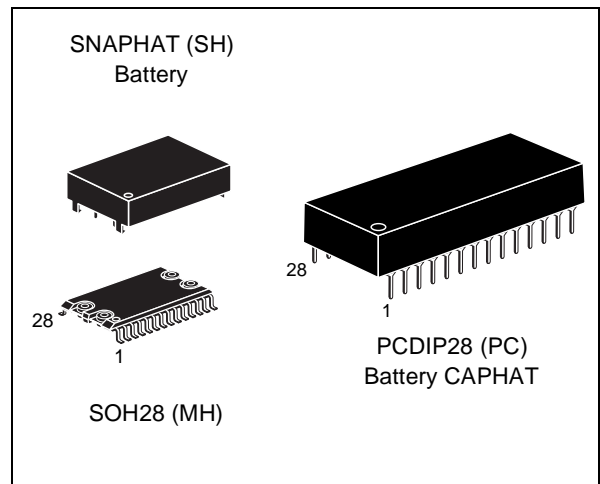
- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- BATTERY LOW FLAG ( $\overline{\text{BOK}}$ )
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGES  
( $V_{\text{PFD}}$  = Power-fail Deselect Voltage):
  - M48Z35AY:  $4.20\text{V} \leq V_{\text{PFD}} \leq 4.50\text{V}$
  - M48Z35AV:  $2.7\text{V} \leq V_{\text{PFD}} \leq 3.0\text{V}$
- SELF-CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- PACKAGING INCLUDES a 28-LEAD SOIC and SNAPHAT® TOP  
(to be Ordered Separately)
- SOIC PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT TOP which CONTAINS the BATTERY and CRYSTAL
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 32K x8 SRAMs

### DESCRIPTION

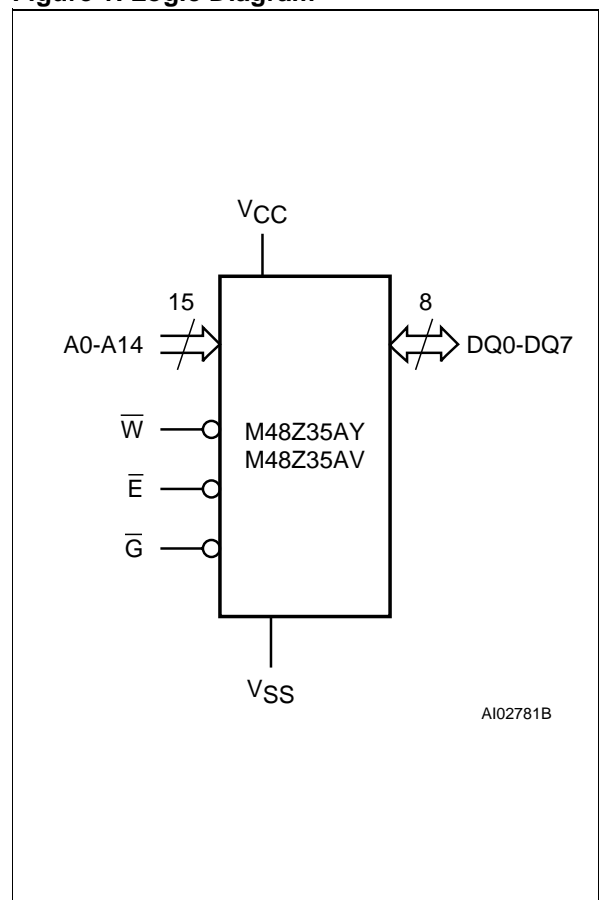
The M48Z35AY/35AV ZEROPOWER® RAM is a 32 Kbit x8 non-volatile static RAM that integrates power-fail deselect circuitry and battery control logic on a single die. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory solution.

**Table 1. Signal Names**

A0-A14	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{\text{E}}$	Chip Enable
$\overline{\text{G}}$	Output Enable
$\overline{\text{W}}$	Write Enable
$V_{\text{CC}}$	Supply Voltage
$V_{\text{SS}}$	Ground



**Figure 1. Logic Diagram**



## M48Z35AY, M48Z35AV

Figure 2A. DIP Pin Connections

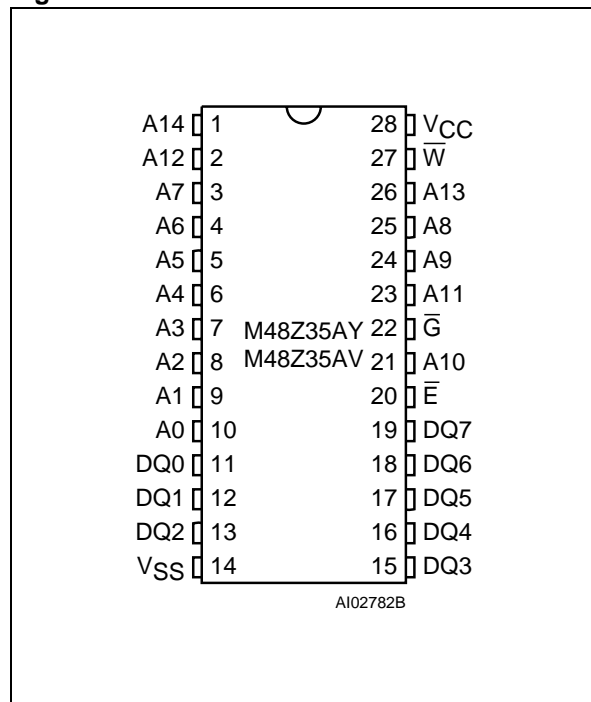


Figure 2B. SOIC Pin Connections

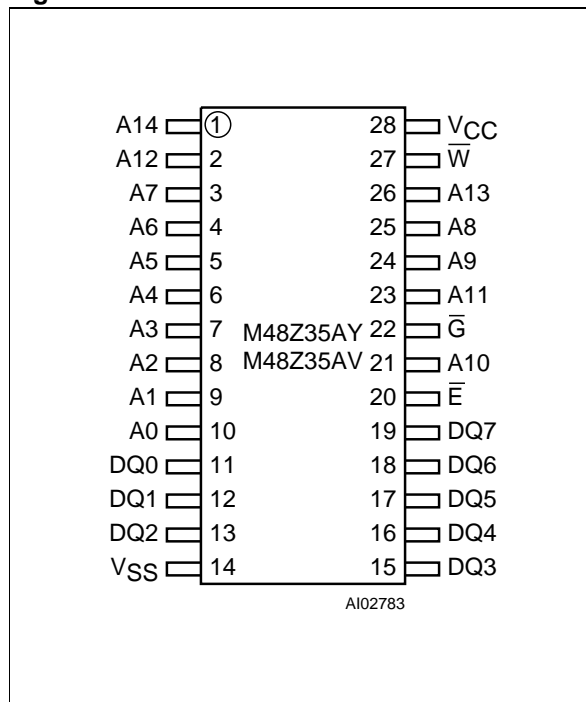


Table 2. Absolute Maximum Ratings <sup>(1)</sup>

Symbol	Parameter	Value	Unit
T <sub>A</sub>	Ambient Operating Temperature Grade 1 Grade 6	0 to 70 -40 to 85	°C
T <sub>STG</sub>	Storage Temperature (V <sub>CC</sub> Off) SNAPHAT SOIC	-40 to 85 -55 to 125	°C
T <sub>SLD</sub> <sup>(2)</sup>	Lead Solder Temperature for 10 seconds	260	°C
V <sub>IO</sub>	Input or Output Voltages	-0.3 to 7	V
V <sub>CC</sub>	Supply Voltage	-0.3 to 7	V
I <sub>O</sub>	Output Current	20	mA
P <sub>D</sub>	Power Dissipation	1	W

Note: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.

2. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

**CAUTION:** Negative undershoots below -0.3V are not allowed on any pin while in the Battery Back-up mode.

**CAUTION:** Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.

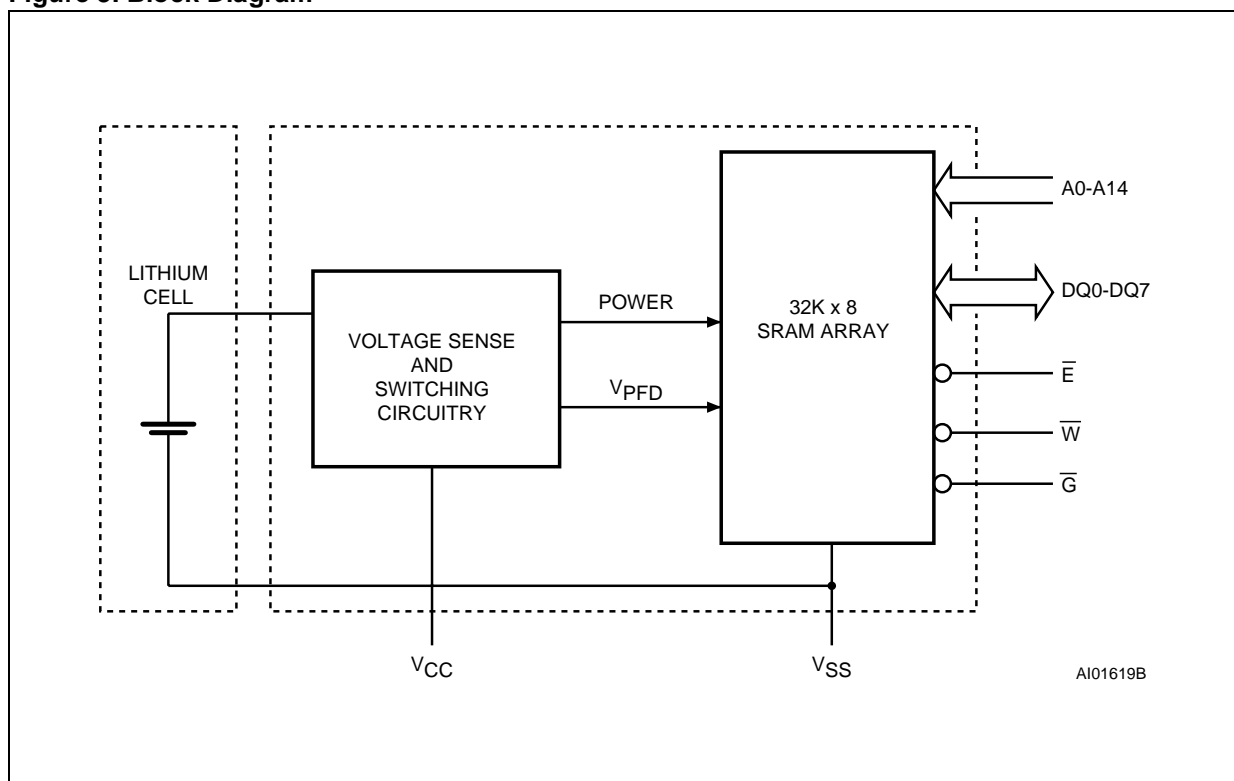
Table 3. Operating Modes <sup>(1)</sup>

Mode	V <sub>CC</sub>	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.5V to 5.5V or 3.0V to 3.6V	V <sub>IH</sub>	X	X	High Z	Standby
Write		V <sub>IL</sub>	X	V <sub>IL</sub>	D <sub>IN</sub>	Active
Read		V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>	Active
Read		V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	High Z	Active
Deselect	V <sub>SO</sub> to V <sub>PFD</sub> (min) <sup>(2)</sup>	X	X	X	High Z	CMOS Standby
Deselect	≤ V <sub>SO</sub>	X	X	X	High Z	Battery Back-up Mode

Note: 1. X = V<sub>IH</sub> or V<sub>IL</sub>; V<sub>SO</sub> = Battery Back-up Switchover Voltage.

2. See Table 7 for details.

Figure 3. Block Diagram



The M48Z35AY/35AV is a non-volatile pin and function equivalent to any JEDEC standard 32K x8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed. The 28 pin 600mil DIP CAPHAT™ houses the M48Z35AY/35AV silicon with a long life lithium button cell in a single package.

The 28 pin 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

**Table 4. AC Measurement Conditions**

Input Rise and Fall Times	$\leq 5\text{ns}$
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

The SOIC and battery packages are shipped separately in plastic anti-static tubes or in Tape & Reel form.

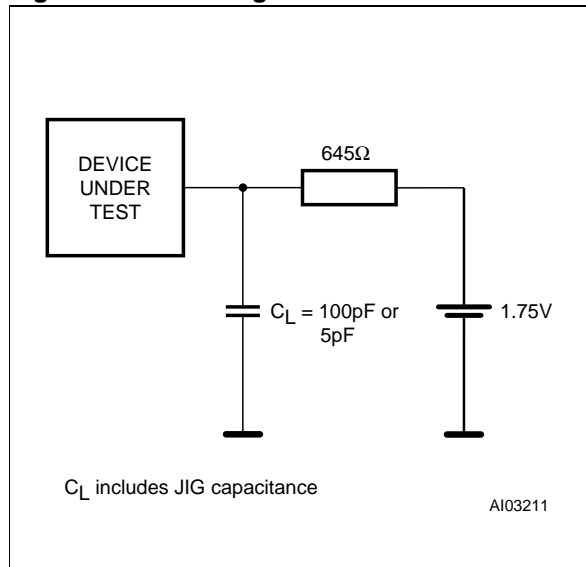
For the 28 lead SOIC, the battery package (i.e. SNAPHAT) part number is "M4Z28-BR00SH1".

The M48Z35AY/35AV also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When  $V_{CC}$  is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low  $V_{CC}$ . As  $V_{CC}$  falls below approximately 3V, the control circuitry connects the battery which maintains data until valid power returns.

## READ MODE

The M48Z35AY/35AV is in the Read Mode whenever  $\overline{W}$  (Write Enable) is high,  $\overline{E}$  (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 264,144 locations in the static storage array. Thus, the unique address specified by the 15 Address Inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within Address Access time ( $t_{AVQV}$ ) after the last address input signal is stable, providing that the  $\overline{E}$  and  $\overline{G}$  access times are also satisfied. If the  $\overline{E}$  and  $\overline{G}$  access times are not met, valid data will be available after the latter of the Chip Enable Access time ( $t_{ELQV}$ ) or Output Enable Access time ( $t_{GLQV}$ ).

The state of the eight three-state Data I/O signals is controlled by  $\overline{E}$  and  $\overline{G}$ . If the outputs are activat-

**Figure 4. AC Testing Load Circuit**


ed before  $t_{AVQV}$ , the data lines will be driven to an indeterminate state until  $t_{AVQV}$ . If the Address Inputs are changed while  $\overline{E}$  and  $\overline{G}$  remain active, output data will remain valid for Output Data Hold time ( $t_{AXQX}$ ) but will go indeterminate until the next Address Access.

## WRITE MODE

The M48Z35AY/35AV is in the Write Mode whenever  $\overline{W}$  and  $\overline{E}$  are low. The start of a write is referenced from the latter occurring falling edge of  $\overline{W}$  or  $\overline{E}$ . A write is terminated by the earlier rising edge of  $\overline{W}$  or  $\overline{E}$ . The addresses must be held valid throughout the cycle.  $\overline{E}$  or  $\overline{W}$  must return high for a minimum of  $t_{EHAX}$  from Chip Enable or  $t_{WHAX}$  from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid  $t_{DVWH}$  prior to the end of write and remain valid for  $t_{WHDH}$  afterward.  $\overline{G}$  should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on  $\overline{E}$  and  $\overline{G}$ , a low on  $\overline{W}$  will disable the outputs  $t_{WLQZ}$  after  $\overline{W}$  falls.

**Table 5. Capacitance (1, 2)**  
( $T_A = 25\text{ }^{\circ}\text{C}$ )

Symbol	Parameter	Test Condition	Min	Max	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$		10	pF
$C_{IO}^{(3)}$	Input / Output Capacitance	$V_{OUT} = 0V$		10	pF

Note: 1. Effective capacitance measured with power supply at 5V.  
 2. Sampled only, not 100% tested.  
 3. Outputs deselected.

**Table 6. DC Characteristics**  
( $T_A = 0\text{ to }70\text{ }^{\circ}\text{C}$  or  $-40\text{ to }85\text{ }^{\circ}\text{C}$ ;  $V_{CC} = 4.5V\text{ to }5.5V$  or  $3.0V\text{ to }3.6V$ )

Symbol	Parameter	Test Condition	Min	Max	Unit
$I_{LI}^{(1)}$	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		$\pm 1$	$\mu A$
$I_{LO}^{(1)}$	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		$\pm 5$	$\mu A$
$I_{CC}$	Supply Current	Outputs open		50	mA
$I_{CC1}$	Supply Current (Standby) TTL	$\bar{E} = V_{IH}$		3	mA
$I_{CC2}$	Supply Current (Standby) CMOS	$\bar{E} = V_{CC} - 0.2V$		3	mA
$V_{IL}^{(2)}$	Input Low Voltage		-0.3	0.8	V
$V_{IH}$	Input High Voltage		2.2	$V_{CC} + 0.3$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1mA$		0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -1mA$	2.4		V

Note: 1. Outputs deselected.  
 2. Negative spikes of -1V allowed for up to 10ns once per cycle.

**Table 7. Power Down/Up Trip Points DC Characteristics (1)**  
( $T_A = 0\text{ to }70\text{ }^{\circ}\text{C}$  or  $-40\text{ to }85\text{ }^{\circ}\text{C}$ )

Symbol	Parameter	Min	Typ	Max	Unit
$V_{PFD}$	Power-fail Deselect Voltage (M48Z35AY)	4.2	4.35	4.5	V
$V_{PFD}$	Power-fail Deselect Voltage (M48Z35AV)	2.7	2.9	3.0	V
$V_{SO}$	Battery Back-up Switchover Voltage (M48Z35AY)		3.0		V
$V_{SO}$	Battery Back-up Switchover Voltage (M48Z35AV)		$V_{PFD} - 100mV$		V
$t_{DR}^{(2)}$	Expected Data Retention Time	10			YEARS

Note: 1. All voltages referenced to  $V_{SS}$ .  
 2. At  $25\text{ }^{\circ}\text{C}$ .

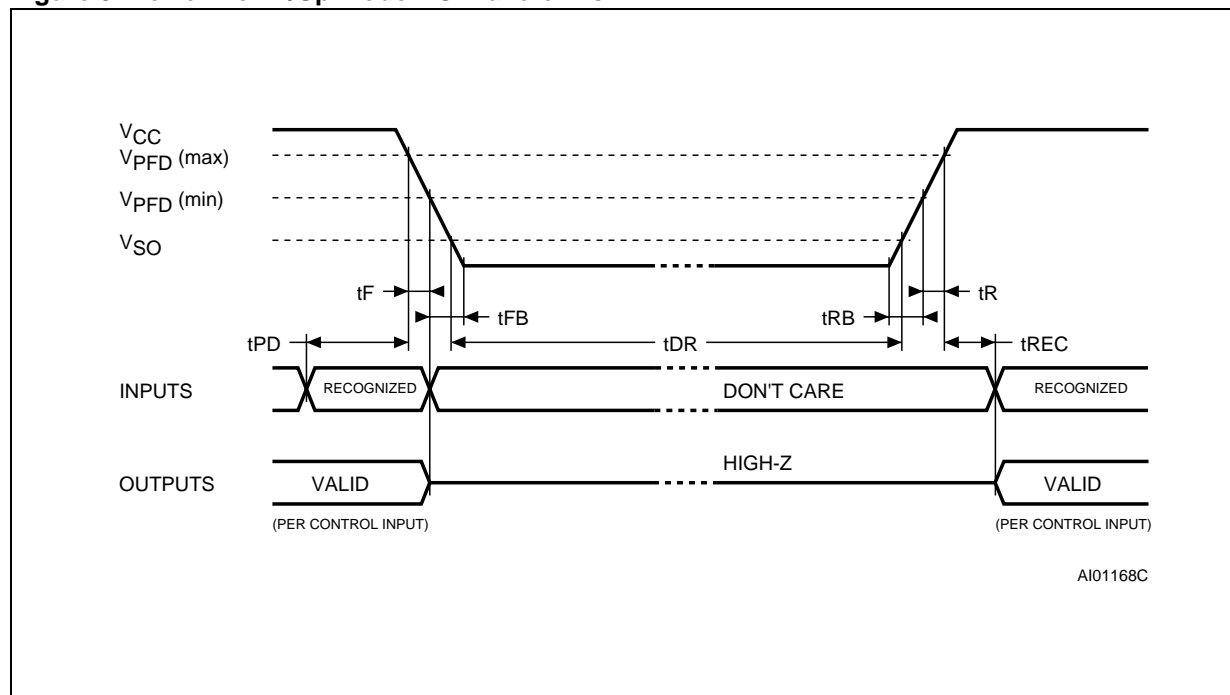
**Table 8. Power Down/Up AC Characteristics**
 $(T_A = 0 \text{ to } 70 \text{ }^{\circ}\text{C or } -40 \text{ to } 85 \text{ }^{\circ}\text{C})$ 

Symbol	Parameter	Min	Max	Unit
$t_{PD}$	$\overline{E}$ or $\overline{W}$ at $V_{IH}$ before Power Down	0		$\mu\text{s}$
$t_F^{(1)}$	$V_{PFD}(\text{max})$ to $V_{PFD}(\text{min})$ $V_{CC}$ Fall Time	300		$\mu\text{s}$
$t_{FB}^{(2)}$	$V_{PFD}(\text{min})$ to $V_{SS}$ $V_{CC}$ Fall Time	10		$\mu\text{s}$
$t_R$	$V_{PFD}(\text{min})$ to $V_{PFD}(\text{max})$ $V_{CC}$ Rise Time	10		$\mu\text{s}$
$t_{RB}$	$V_{SS}$ to $V_{PFD}(\text{min})$ $V_{CC}$ Rise Time	1		$\mu\text{s}$
$t_{REC}^{(3)}$	$V_{PFD}(\text{max})$ to Inputs Recognized	40	200	ms

Note: 1.  $V_{PFD}(\text{max})$  to  $V_{PFD}(\text{min})$  fall time of less than  $t_F$  may result in deselection/write protection not occurring until 200 $\mu\text{s}$  after  $V_{CC}$  passes  $V_{PFD}(\text{min})$ .

2.  $V_{PFD}(\text{min})$  to  $V_{SS}$  fall time of less than  $t_{FB}$  may cause corruption of RAM data.

3.  $t_{REC}(\text{min}) = 20\text{ms}$  for industrial temperature grade (6) device.

**Figure 5. Power Down/Up Mode AC Waveforms**


### Table 9. Read Mode AC Characteristics

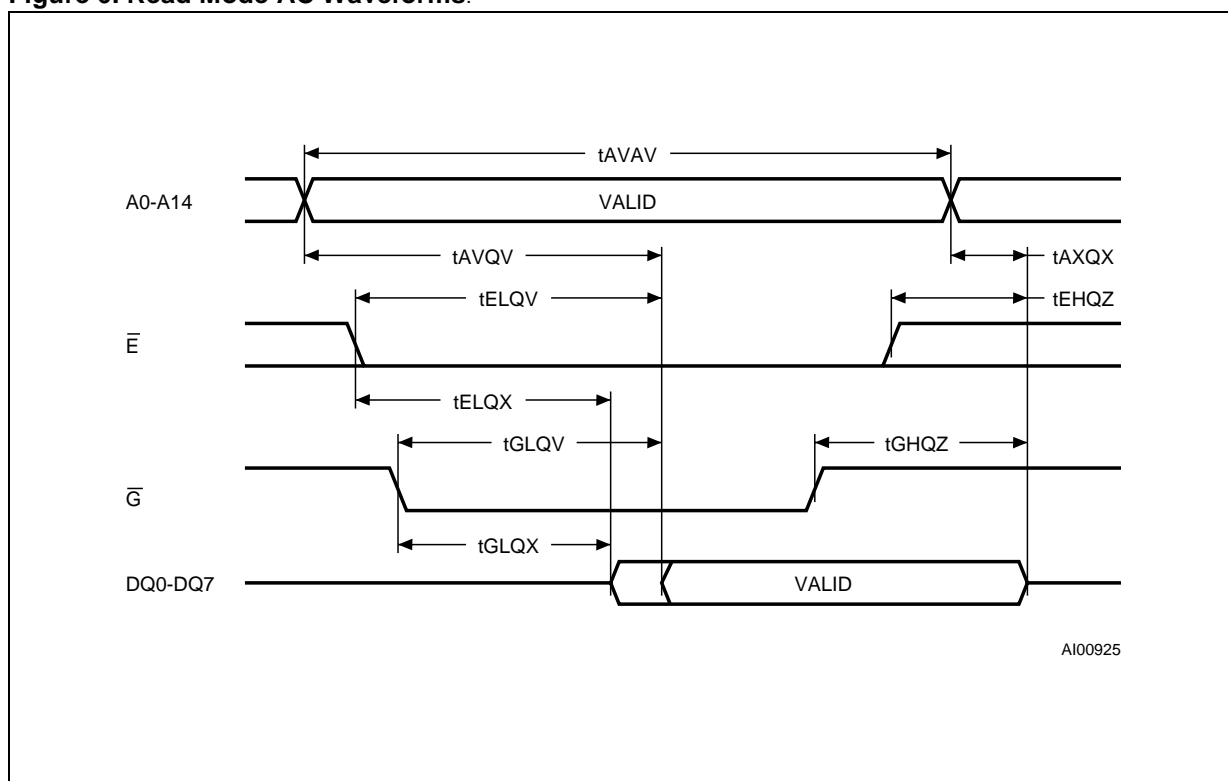
(T<sub>A</sub> = 0 to 70 °C or -40 to 85 °C; V<sub>CC</sub> = 4.5V to 5.5V or 3.0V to 3.6V)

Symbol	Parameter	M48Z35AY		M48Z35AV		Unit
		-70		-100		
		Min	Max	Min	Max	
t <sub>AVAV</sub>	Read Cycle Time	70		100		ns
t <sub>AVQV</sub> <sup>(1)</sup>	Address Valid to Output Valid		70		100	ns
t <sub>ELQV</sub> <sup>(1)</sup>	Chip Enable Low to Output Valid		70		100	ns
t <sub>GLQV</sub> <sup>(1)</sup>	Output Enable Low to Output Valid		35		50	ns
t <sub>ELQX</sub> <sup>(2)</sup>	Chip Enable Low to Output Transition	5		10		ns
t <sub>GLQX</sub> <sup>(2)</sup>	Output Enable Low to Output Transition	5		5		ns
t <sub>EHQZ</sub> <sup>(2)</sup>	Chip Enable High to Output Hi-Z		25		50	ns
t <sub>GHQZ</sub> <sup>(2)</sup>	Output Enable High to Output Hi-Z		25		40	ns
t <sub>AXQX</sub> <sup>(1)</sup>	Address Transition to Output Transition	10		10		ns

Note: 1.  $C_L = 100\text{pF}$  (see Figure 4).

2.  $C_L = 5\text{pF}$  (see Figure 4).

**Figure 6. Read Mode AC Waveforms.**



Note: Write Enable ( $\overline{W}$ ) = High.

**Table 10. Write Mode AC Characteristics**
 $(T_A = 0 \text{ to } 70^\circ\text{C or } -40 \text{ to } 85^\circ\text{C}; V_{CC} = 4.5\text{V to } 5.5\text{V or } 3.0\text{V to } 3.6\text{V})$ 

Symbol	Parameter	M48Z35AY		M48Z35AV		Unit
		-70		-100		
		Min	Max	Min	Max	
t <sub>AVAV</sub>	Write Cycle Time	70		100		ns
t <sub>AVWL</sub>	Address Valid to Write Enable Low	0		0		ns
t <sub>AVEL</sub>	Address Valid to Chip Enable Low	0		0		ns
t <sub>WLWH</sub>	Write Enable Pulse Width	50		80		ns
t <sub>ELEH</sub>	Chip Enable Low to Chip Enable High	55		80		ns
t <sub>WHAX</sub>	Write Enable High to Address Transition	0		10		ns
t <sub>EHAX</sub>	Chip Enable High to Address Transition	0		10		ns
t <sub>DVWH</sub>	Input Valid to Write Enable High	30		50		ns
t <sub>DVEH</sub>	Input Valid to Chip Enable High	30		50		ns
t <sub>WHDX</sub>	Write Enable High to Input Transition	5		5		ns
t <sub>EHDX</sub>	Chip Enable High to Input Transition	5		5		ns
t <sub>WLQZ</sub> <sup>(1, 2)</sup>	Write Enable Low to Output Hi-Z		25		50	ns
t <sub>AVWH</sub>	Address Valid to Write Enable High	60		80		ns
t <sub>AVEH</sub>	Address Valid to Chip Enable High	60		80		ns
t <sub>WHQX</sub> <sup>(1, 2)</sup>	Write Enable High to Output Transition	5		10		ns

Note: 1.  $C_L = 5\text{pF}$  (see Figure 4).

2. If  $\overline{E}$  goes low simultaneously with  $\overline{W}$  going low, the outputs remain in the high impedance state.

## DATA RETENTION MODE

With valid  $V_{CC}$  applied, the M48Z35AY/35AV operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when  $V_{CC}$  falls within the  $V_{PFD}(\text{max})$ ,  $V_{PFD}(\text{min})$  window. All outputs become high impedance, and all inputs are treated as "don't care."

**Note:** A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below  $V_{PFD}(\text{min})$ , the user can be assured the memory will be in a write protected state, provided the  $V_{CC}$  fall time is not less than  $t_F$ . The M48Z35AY/35AV may respond to transient noise spikes on  $V_{CC}$  that reach into the deselect

window during the time the device is sampling  $V_{CC}$ . Therefore, decoupling of the power supply lines is recommended.

When  $V_{CC}$  drops below  $V_{SO}$ , the control circuit switches power to the internal battery which preserves data. The internal button cell will maintain data in the M48Z35AY/35AV for an accumulated period of at least 10 years (at  $25^\circ\text{C}$ ) when  $V_{CC}$  is less than  $V_{SO}$ .

As system power returns and  $V_{CC}$  rises above  $V_{SO}$ , the battery is disconnected, and the power supply is switched to external  $V_{CC}$ . Write protection continues until  $V_{CC}$  reaches  $V_{PFD}(\text{min})$  plus  $t_{REC}(\text{min})$ . Normal RAM operation can resume  $t_{REC}$  after  $V_{CC}$  exceeds  $V_{PFD}(\text{max})$ .

Figure 7. Write Enable Controlled, Write AC Waveform

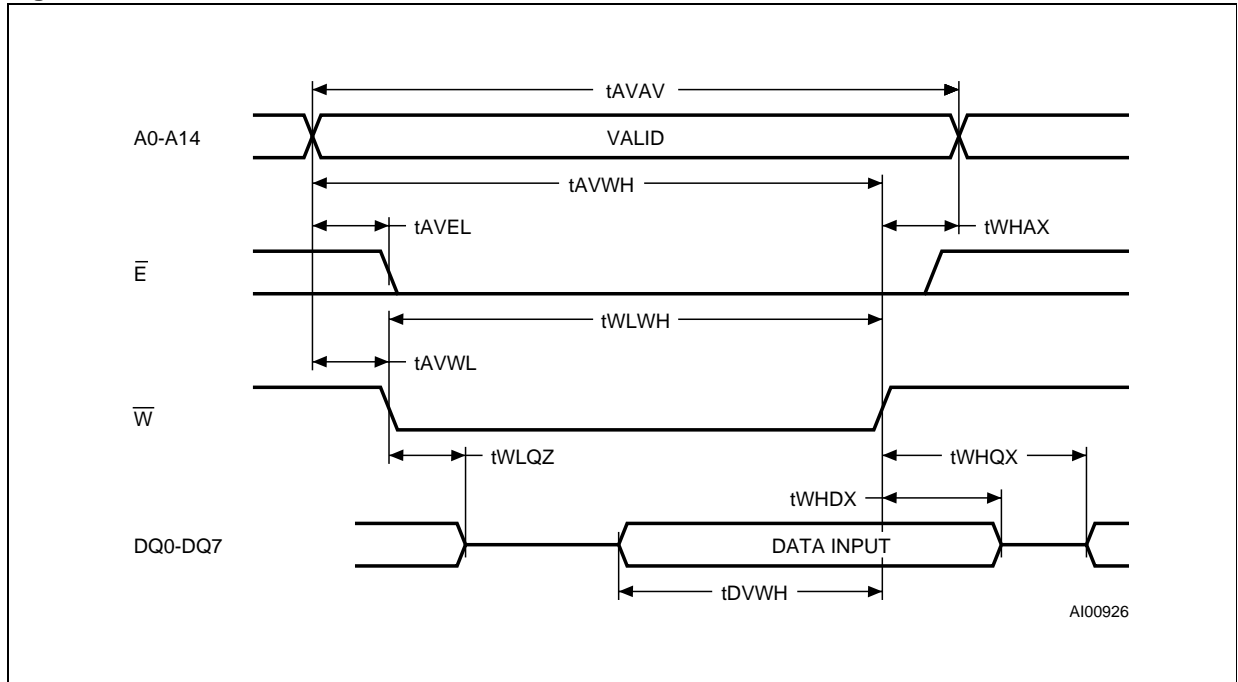


Figure 8. Chip Enable Controlled, Write AC Waveforms

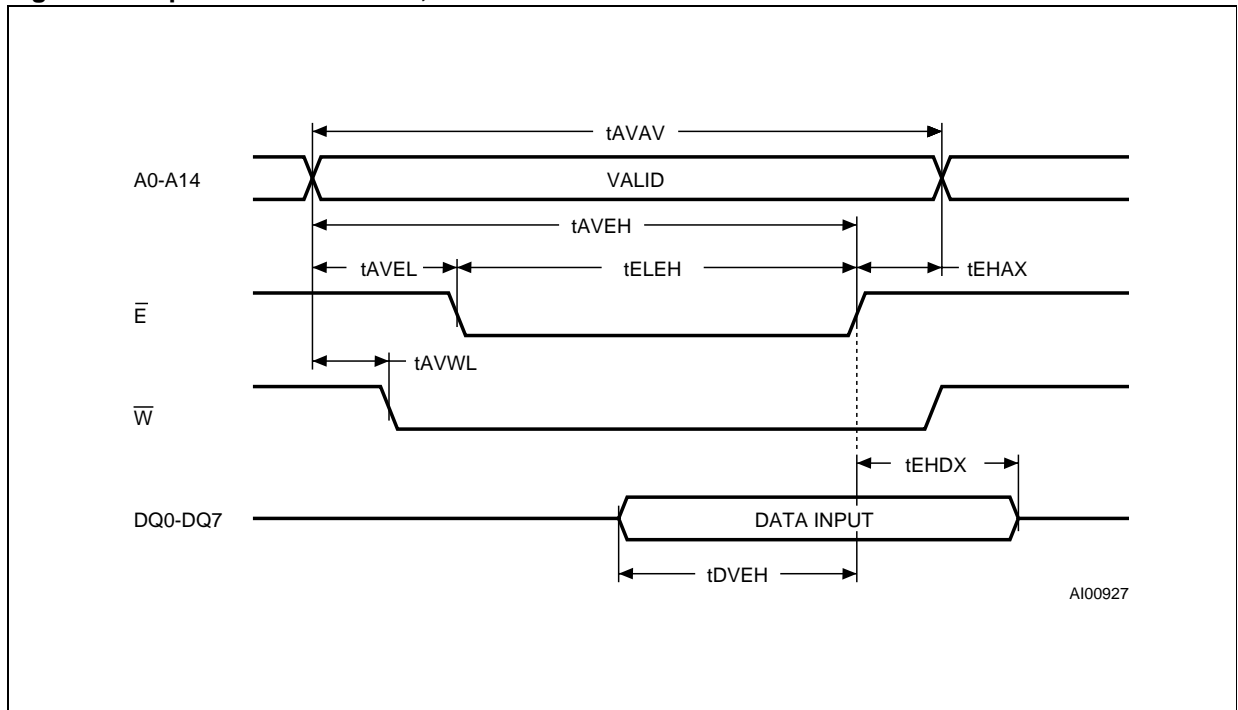
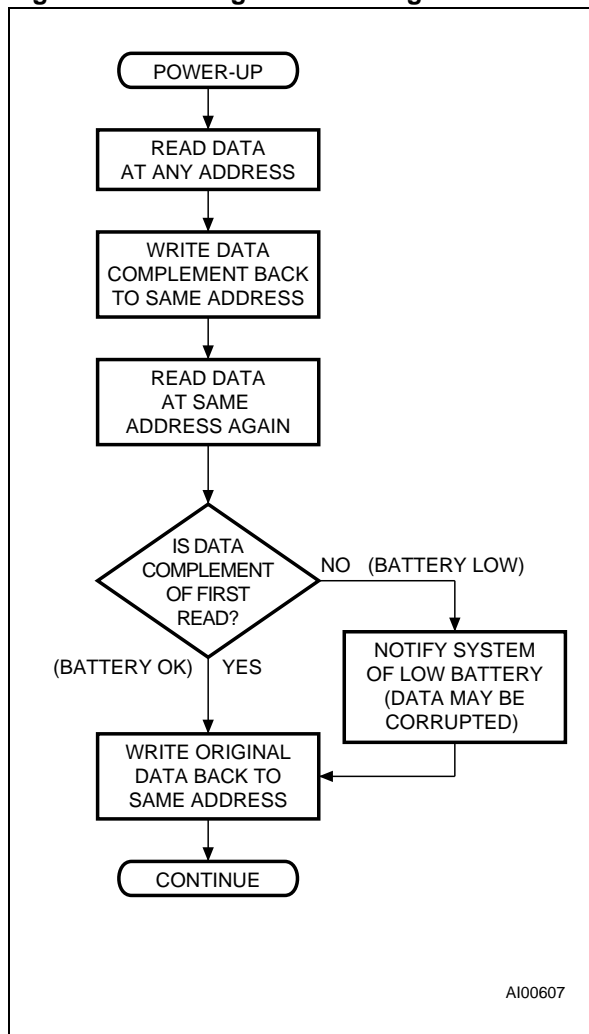


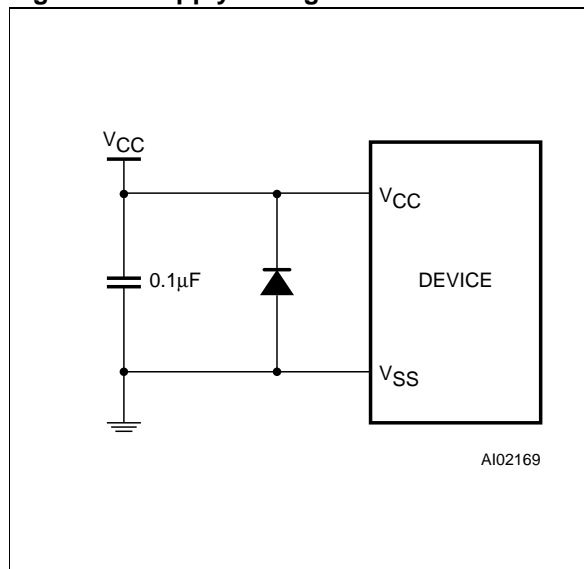
Figure 9. Checking the BOK Flag Status



Also, as  $V_{CC}$  rises, the battery voltage is checked. If the voltage is less than approximately 2.5V, an internal Battery Not OK (BOK) flag will be set. The BOK flag can be checked after power up. If the BOK flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 9 illustrates how a BOK check routine could be structured.

For more information on Battery Storage Life refer to the Application Note AN1012.

Figure 10. Supply Voltage Protection



#### POWER SUPPLY DECOUPLING and UNDERSHOOT PROTECTION

$I_{CC}$  transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the  $V_{CC}$  bus. These transients can be reduced if capacitors are used to store energy, which stabilizes the  $V_{CC}$  bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of  $0.1\mu F$  (as shown in Figure 10) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on  $V_{CC}$  that drive it to values below  $V_{SS}$  by as much as one Volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a schottky diode from  $V_{CC}$  to  $V_{SS}$  (cathode connected to  $V_{CC}$ , anode to  $V_{SS}$ ). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

**Table 11. Ordering Information Scheme**

Example:

M48Z35AY -70 MH 1 TR

**Supply Voltage and Write Protect Voltage**35AY =  $V_{CC} = 4.5V$  to  $5.5V$ ;  $V_{PFD} = 4.2V$  to  $4.5V$ 35AV =  $V_{CC} = 3.0V$  to  $3.6V$ ;  $V_{PFD} = 2.7V$  to  $3.0V$ **Speed**

-70 = 70ns (M48Z35AY)

-100 = 100ns (M48Z35AV)

**Package**

PC = PCDIP28

MH <sup>(1)</sup> = SOH28**Temperature Range**

1 = 0 to 70 °C

6 <sup>(2)</sup> = -40 to 85 °C**Shipping Method for SOIC**

blank = Tubes

TR = Tape &amp; Reel

Note: 1. The SOIC package (SOH28) requires the battery package (SNAPHAT) which is ordered separately under the part number "M4Zxx-BR00SH1" in plastic tube or "M4Zxx-BR00SH1TR" in Tape & Reel form.

2. Industrial temperature grade available in SOIC package (SOH28) only.

**Caution:** Do not place the SNAPHAT battery package "M4Z28-BR00SH1" in conductive foam since will drain the lithium button-cell battery.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

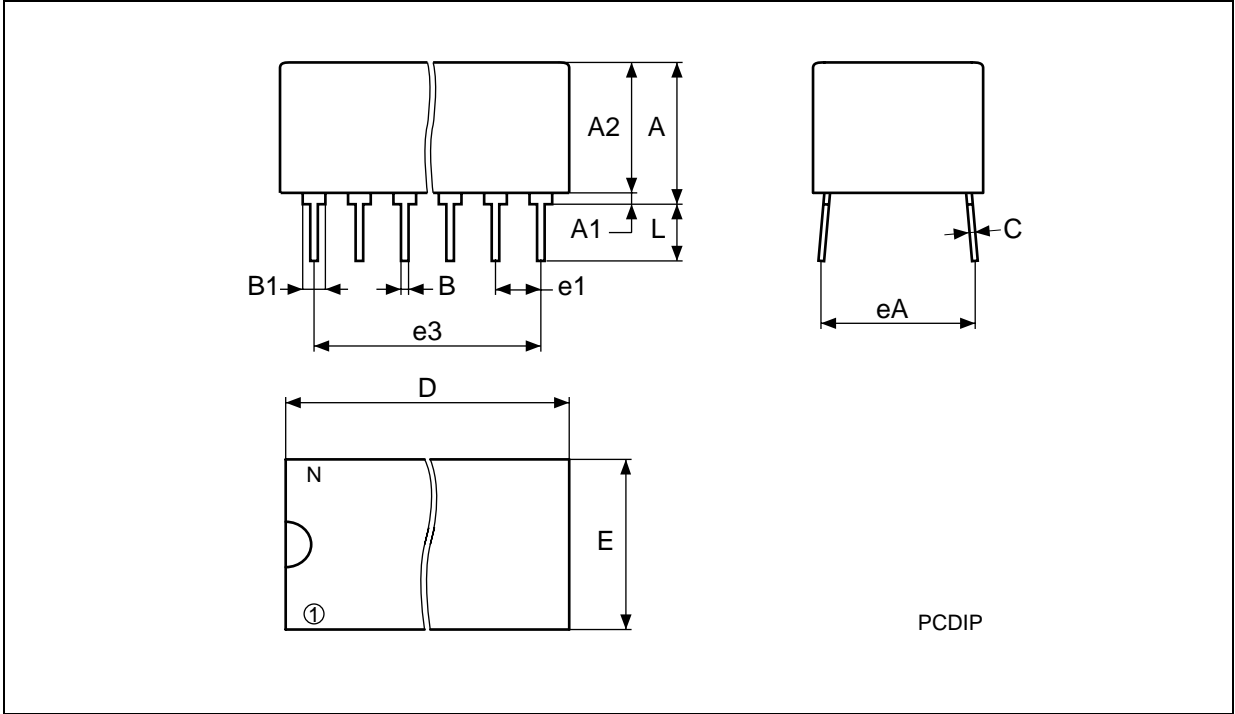
**Table 12. Revision History**

Date	Revision Details
September 1999	First Issue
04/20/00	SH and SH28 packages for 2-pin and 2-socket removed

Table 13. PCDIP28 - 28 pin Plastic DIP, battery CAPHAT, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N		28			28	

Figure 11. PCDIP28 - 28 pin Plastic DIP, battery CAPHAT, Package Outline

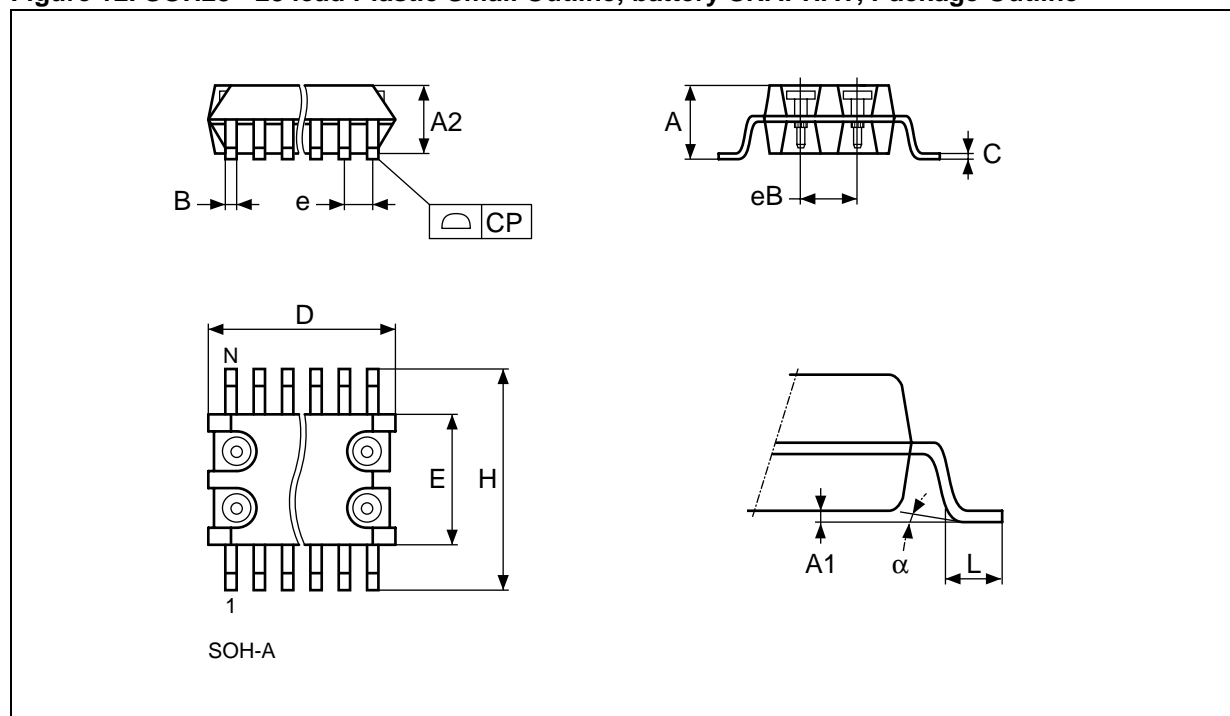


Drawing is not to scale.

Table 14. SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
$\alpha$		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

Figure 12. SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT, Package Outline

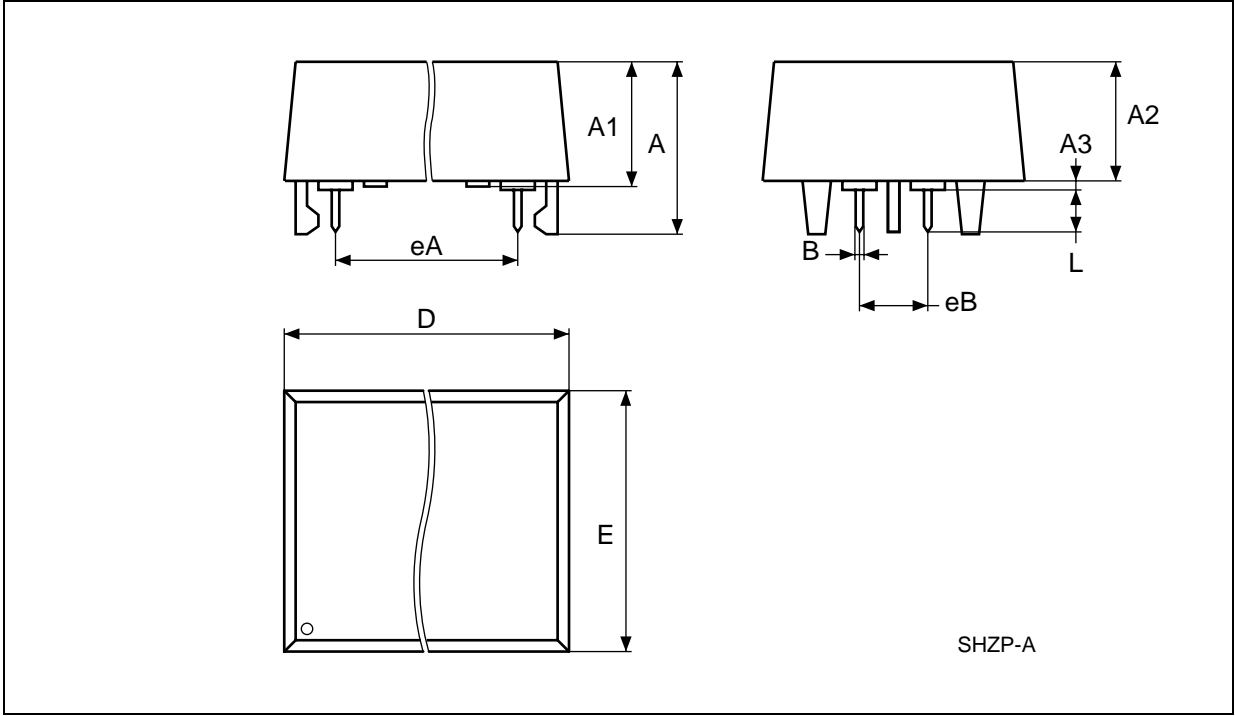


Drawing is not to scale.

Table 15. SH - SNAPHAT Housing for 48 mAh Battery, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 13. SH - SNAPHAT Housing for 48 mAh Battery, Package Outline

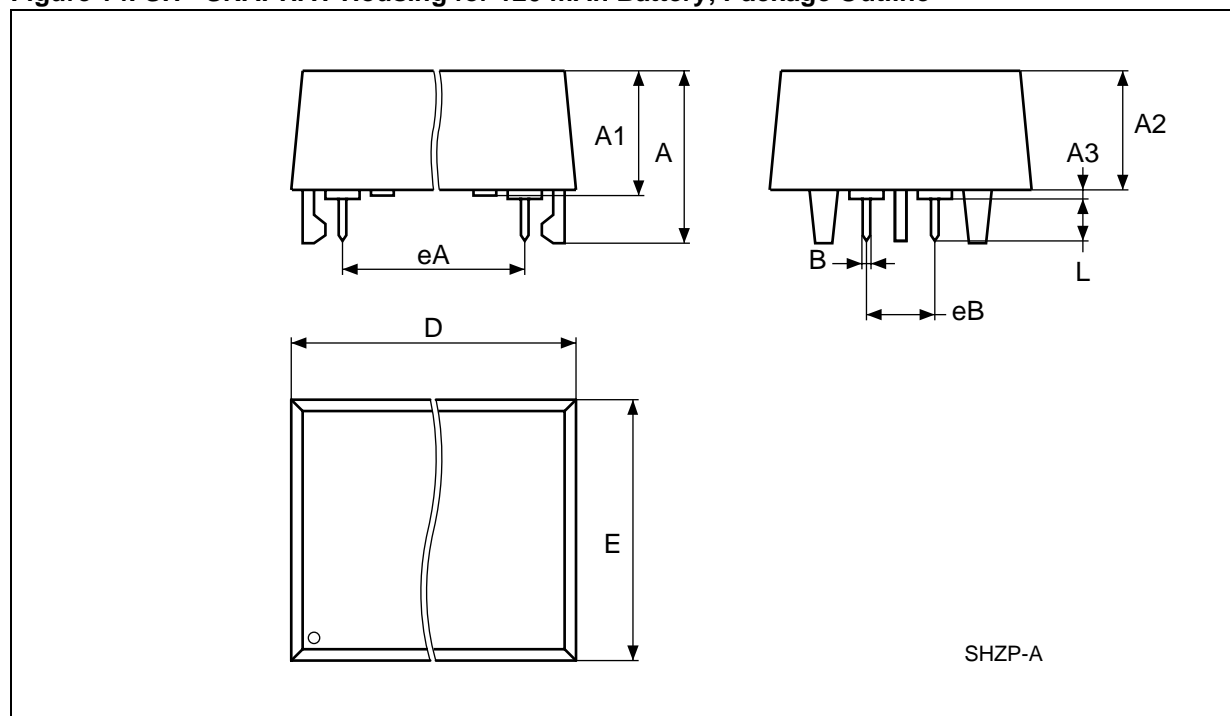


Drawing is not to scale.

Table 16. SH - SNAPHAT Housing for 120 mAh Battery, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54			0.415
A1		8.00	8.51		0.315	0.335
A2		7.24	8.00		0.285	0.315
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	0.710
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 14. SH - SNAPHAT Housing for 120 mAh Battery, Package Outline



Drawing is not to scale.

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