M7040N

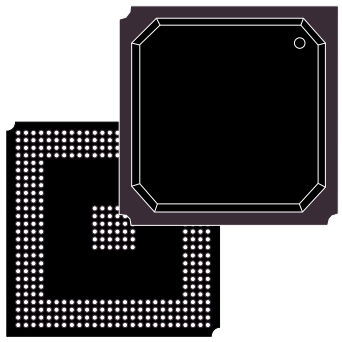
64K x 72-bit Entry NETWORK PACKET SEARCH ENGINE

PRELIMINARY DATA

FEATURES SUMMARY

- 64K DATA ENTRIES IN 72-BIT MODE
- TABLE MAY BE PARTITIONED INTO UP TO EIGHT (8) OCTANTS
  (Data entry width in each octant is configurable as 36, 72, 144, or 288 bits.)
- UP TO 100 MILLION SUSTAINED SEARCHES PER SECOND IN 72-BIT and 144-BIT CONFIGURATIONS
- UP TO 50 MILLION SEARCHES PER SECOND IN 36-BIT and 288-BIT CONFIGURATIONS
- SEARCHES ANY SUB-FIELD IN A SINGLE CYCLE
- OFFERS BIT-BY-BIT and GLOBAL MASKING
- SYNCHRONOUS, PIPELINED OPERATION
- UP TO 31 SEARCH ENGINES CASCADABLE WITHOUT PERFORMANCE DEGRADATION
- WHEN CASCADED, THE DATABASE ENTRIES CAN SCALE FROM 496K TO 3968K DEPENDING ON THE WIDTH OF THE ENTRY
- GLUELESS INTERFACE TO INDUSTRY-STANDARD SRAMS
- SIMPLE HARDWARE INSTRUCTION INTERFACE
- IEEE 1149.1 TEST ACCESS PORT
- OPERATING SUPPLY VOLTAGES INCLUDE:
  V_{DD} (Operating Core Supply Voltage) = 1.5V for 66 and 83MSPS; 1.65V for 100MSPS
  V_{DDQ} (Operating Supply Voltage for I/O) = 2.5 or 3.3V
- 388 PBGA, 35mm x 35mm

Figure 1. 388-ball PBGA Package



388-ball PBGA
35mm x 35mm

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DESCRIPTION

Overview

ST Microelectronics, Inc.'s M7040N Search Engine incorporates patent-pending Associative Processing Technology™ (APT) and is designed to be a high-performance, pipelined, synchronous, 64K-entry network database search engine. The M7040N database entry size can be 72 bits, 144 bits, or 288 bits. In the 72-bit entry mode, the size of the database is 64K entries. In the 144-bit mode, the size of the database is 32K entries, and in the 288-bit mode, the size of the database is 16K entries. The M7040N is configurable to support multiple databases with different entry sizes. The 36-bit entry table can be implemented using the Global Mask Registers (GMRs) building-database size of 128K entries with a single device.

Performance

The Search Engine can sustain 100 million transactions per second when the database is programmed or configured as 72 or 144 bits. When the database is programmed to have an entry size of 36 or 288 bits, the Search Engine will perform at 50 million transactions per second. STM's M7040N can be used to accelerate network protocols such as Longest-prefix Match (CIDR), ARP, MPLS, and other Layer 2, 3, and 4 protocols.

Applications

This high-speed, high-capacity Search Engine can be deployed in a variety of networking and communications applications. The performance and features of the M7040N make it attractive in applications such as Enterprise LAN switches and routers and broadband switching and/or routing equipment supporting multiple data rates at OC–48 and beyond. The Search Engine is designed to be scalable in order to support network database sizes to 3968K entries specifically for environments that require large network policy databases. Figure 4, page 10 shows the block diagram for the M7040N device.

Table 1. Product Range

Part Number	Operating Supply Voltage	Operating I/O Voltage	Speed	Temperature Range
M7040N-100ZA1	1.65V	2.5 or 3.3V	100MHz	Commercial
M7040N-083ZA1	1.5V	2.5 or 3.3V	83MHz	Commercial
M7040N-066ZA1	1.5V	2.5 or 3.3V	66MHz	Commercial

Figure 2. Switch/Router Implementation Using the M7040N

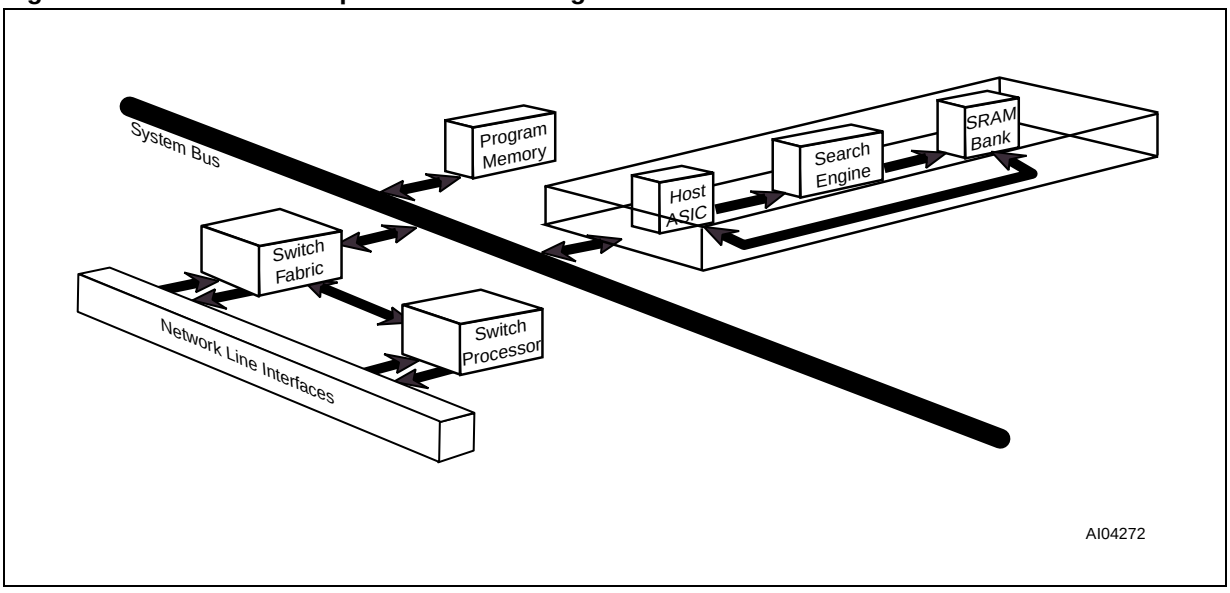


Table 2. Signal Names

Symbol	Type(1)	Description
Clocks and Reset		
CLK_MODE	I	Clock Mode
CLK2X_CLK1X	I	Master Clock
PHS_L	I	Phase
TEST_CO(2)	I	Test Output (ST Use Only)
TEST	I	Test Input (ST Use Only)
TEST_FM	I	Test Input (ST Use Only)
RST_L	I	Reset
TEST_PB(3)	I	Test Input (ST Use Only)
CFG_L	I	Configuration
Command and DQ Bus		
CMD[10:0]	I	Command Bus
CMDV	I	Command Valid
DQ[71:0]	I/O	Address/Data Bus
ACK(4)	T	READ Acknowledge
EOT(4)	T	End of Transfer
SSF	T	SEARCH Successful Flag
SSV	T	SEARCH Successful Flag Valid
MULTI_HIT	O	Multiple Hit Flag
HIGH_SPEED	I	100MHz Indicator
CLKTUNE[3:0]	I	PLL Tuner
SRAM Interface		
SADR[23:0]	T	SRAM Address
CE_L	T	SRAM Chip Enable
WE_L	T	SRAM Write Enable
OE_L	T	SRAM Output Enable
ALE_L	T	Address Latch Enable
Cascade Interface		
LHI[6:0]	I	Local Hit In
LHO[1:0]	O	Local Hit Out
BHI[2:0]	I	Block Hit In
BHO[2:0]	O	Block Hit Out
FULI[6:0]	I	Full In
FULO[1:0]	O	Full Out
FULL	O	Full Flag
Device Identification		
ID[4:0]	I	Device Identification
Supplies		
V_{DD}	n/a	Chip Core Supply (1.5V for 66 and 83MSPS; 1.65 for 100MSPS)
V_{DDQ}	n/a	Chip I/O Supply (2.5 or 3.3V)
Test Access Port		
TDI	I	Test Access Port's Test Data In
TCK	I	Test Access Port's Test Clock
TDO	T	Test Access Port's Test Data Out
TMS	I	Test Access Port's Test Mode Select
TRST_L	I	Test Access Port's Reset

Note: 1. Signal types are: I = Input only; I/O = Input or Output; O = Output; and T = Tristate
See DESCRIPTIONS FOR CONNECTION DIAGRAM (Figure 3, page 9), page 152 for individual connection details.
2. In the previous versions of this specification, this signal was called, "CLK_OUT."
3. In previous versions of this specification, this signal was called, "PLL_BYPASS."
4. ACK and EOT Signals require a weak, external pull-down resistor of 47 KΩ or 100 KΩ.

Figure 3. Connections

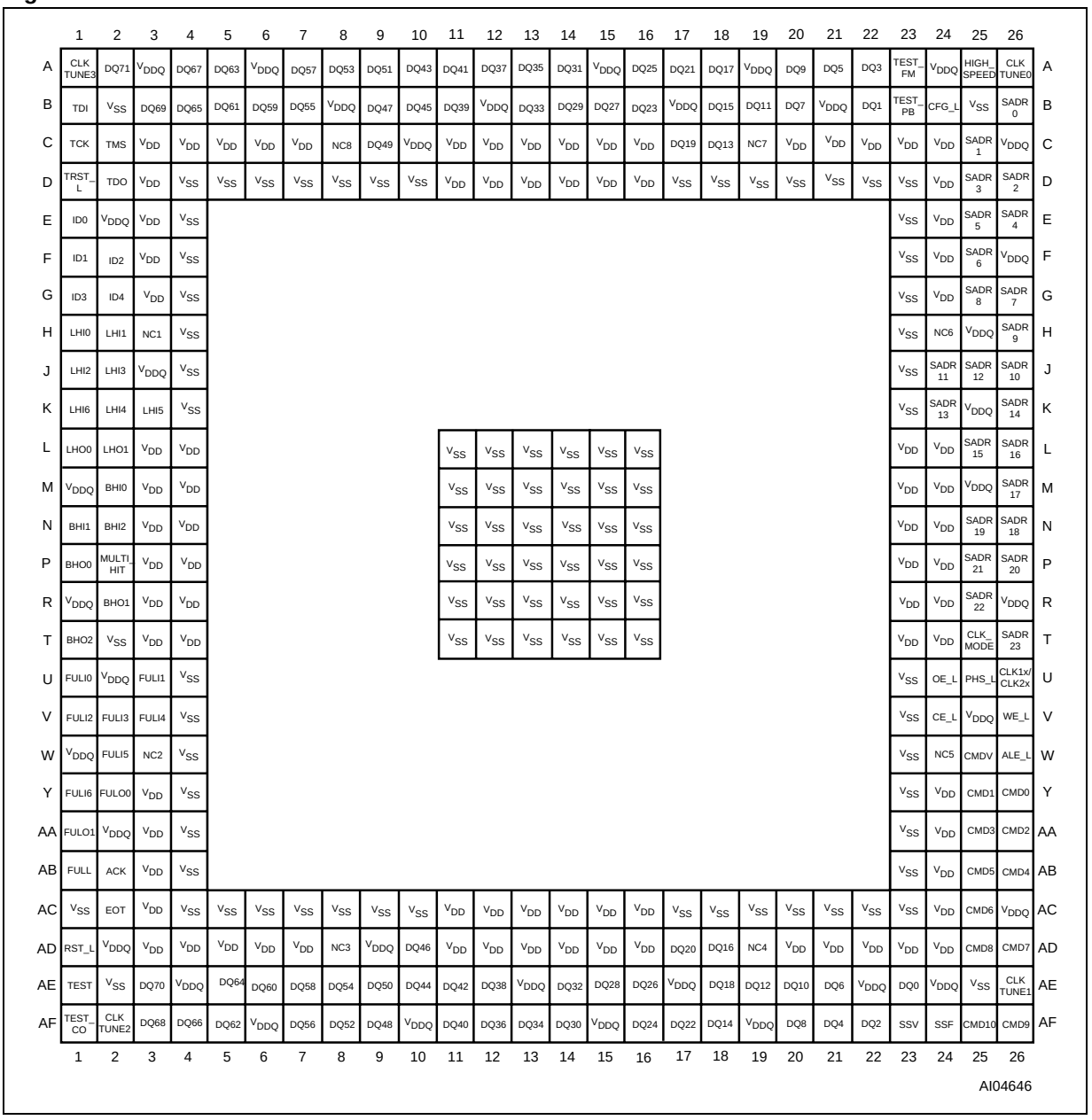
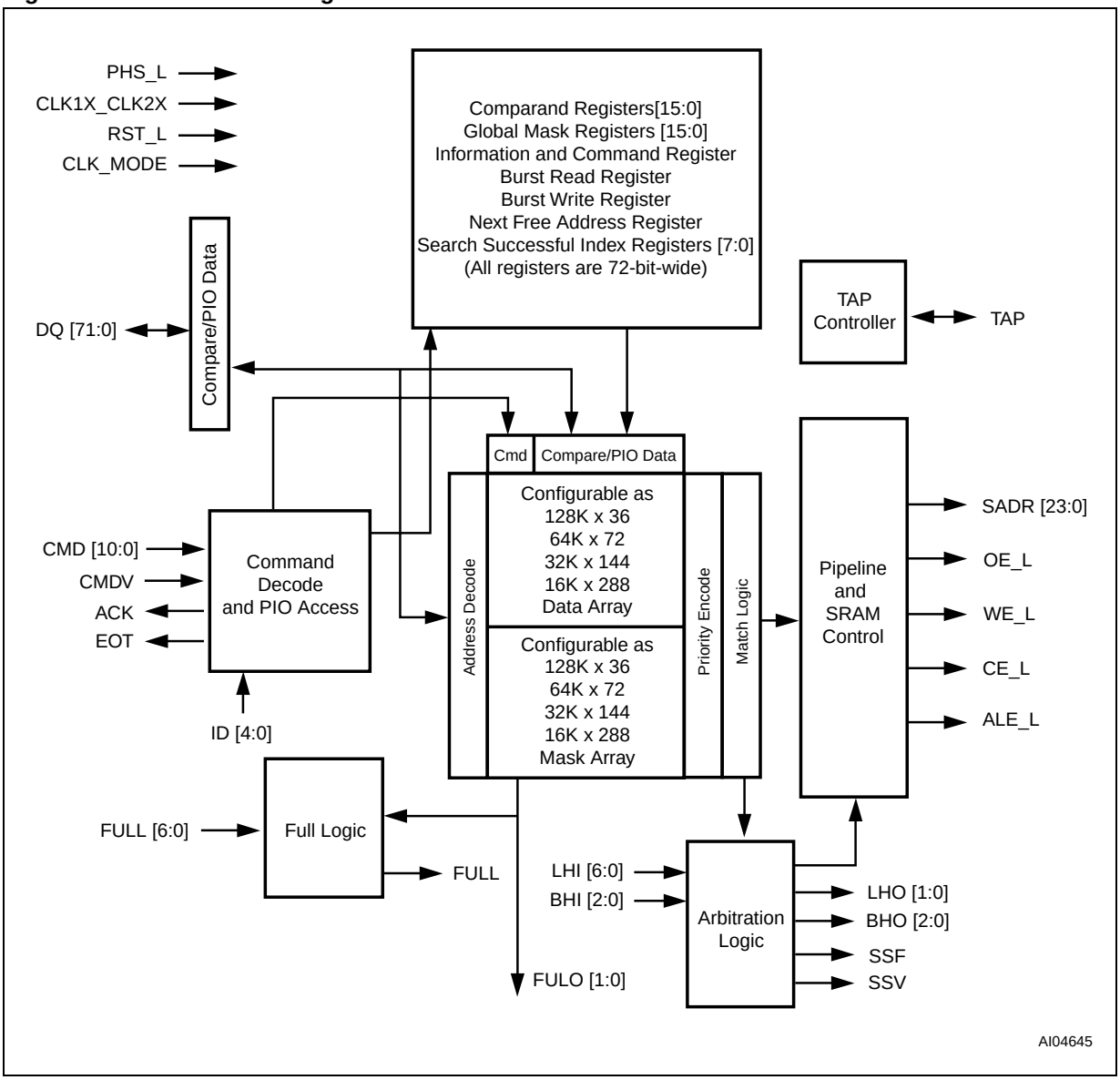


Figure 4. M7040N Block Diagram



MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_{STG}	Storage Temperature (V_{DD} Off)		–0 to 70	°C
T_{SLD}(1)	Lead Solder Temperature for 10 seconds		235	°C
V_{DD}	V_{DD} Operating Supply Voltage	CLK1X = 83MHz	1.575	V
		CLK1X = 100MHz	1.733	V
V_{DDQ}	V_{DDQ} Voltage for I/O (3.3V)		3.5	V
V_{DDQ}	V_{DDQ} Voltage for I/O (2.5V)		2.625	V
V_{DDQ}	V_{DDQ} Voltage for I/O (1.8V)		1.9	V
I_O	Output Current		100	mA

Note: 1. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 4. DC and AC Measurement Conditions

Sym	Parameter		Min	Max	Units
V_{DD}	V_{DD} Operating Supply Voltage	CLK1X = 83MHz	1.425	1.575	V
		CLK1X = 100MHz	1.568	1.733	V
V_{DDQ}	V_{DDQ} Voltage for I/O (3.3V)		3.1	3.5	V
V_{DDQ}	V_{DDQ} Voltage for I/O (2.5V)		2.375	2.625	V
V_{DDQ}	V_{DDQ} Voltage for I/O (1.8V)		1.7	1.9	V
t_A	Ambient Operating Temperature		0	70	°C
	Supply Voltage Tolerance		–5	+5	%
	Input Pulse Levels (V_{DDQ} = 3.3V)			GND to 3.0	V
	Input Pulse Levels (V_{DDQ} = 2.5V)			GND to 2.5	V
	Input Pulse Levels (V_{DDQ} = 1.8V)			GND to 1.8	V
	Input Rise and Fall Times at 0.3V and 2.7V (V_{DDQ} = 3.3V)			≤ 2ns (see Figure 6, page 13)	ns
	Input Rise and Fall Times at 0.25V and 2.25V (V_{DDQ} = 2.5V)			≤ 2ns (see Figure 6, page 13)	ns
	Input Timing Reference Levels (V_{DDQ} = 3.3V)			1.5	V
	Input Timing Reference Levels (V_{DDQ} = 2.5V)			1.25	V
	Input Timing Reference Levels (V_{DDQ} = 1.8V)			0.9	V
	Output Timing Reference Levels (V_{DDQ} = 3.3V)			1.5	V
	Output Timing Reference Levels (V_{DDQ} = 2.5V)			1.25	V
	Output Timing Reference Levels (V_{DDQ} = 1.8V)			0.9	V
	Output Load			(see Figure 5 and Figure 7, page 13)	V

Note: 1. Maximum allowable applies to overshoot only (V_{DDQ} is 3.3V supply).
2. Minimum allowable applies to undershoot only.

Figure 5. M7040N 1.8, 2.5, or 3.3V AC Testing Load

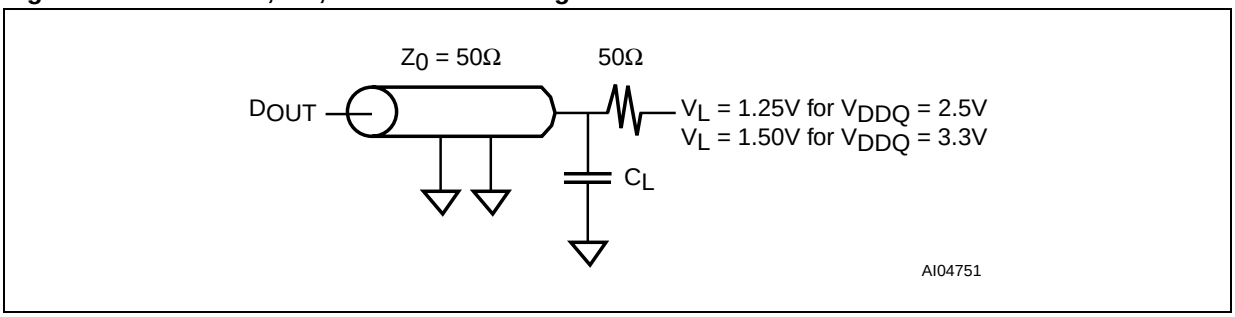


Figure 6. M7040N 1.8, 2.5, or 3.3V Input Waveform

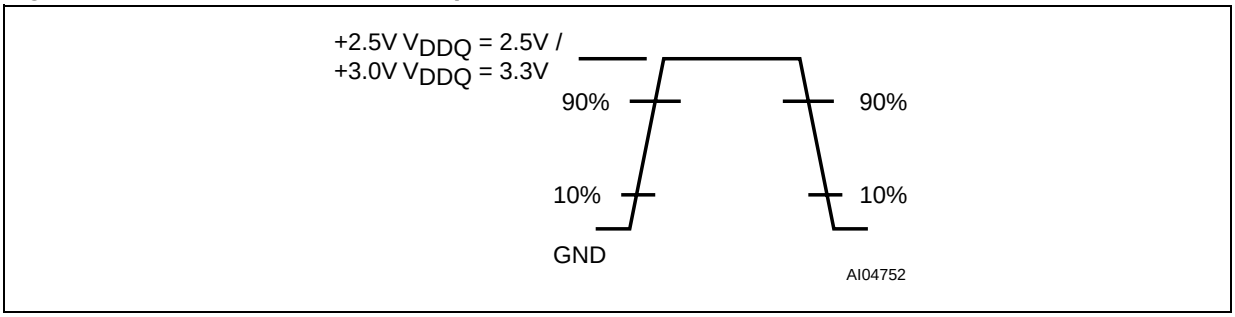
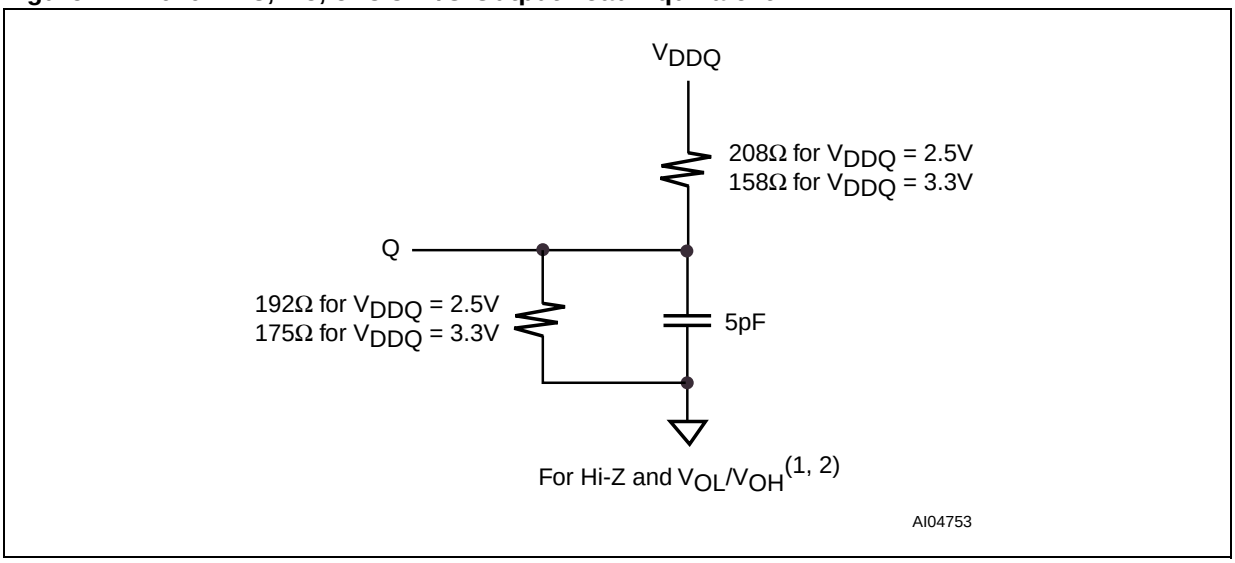


Figure 7. M7040N 1.8, 2.5, or 3.3V I/O Output Load Equivalent



Note: 1. Output loading is specified with CL = 5pF as in Figure 7. Transition is measured at ± 200 mV from steady-state voltage.
2. The load used for V_{OH}, V_{OL} testing is shown in Figure 7.

Table 5. Capacitance

Symbol	Parameter	Test Condition(1,2)	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{IO}(3)	Output Capacitance	V_{OUT} = 0V		6	pF

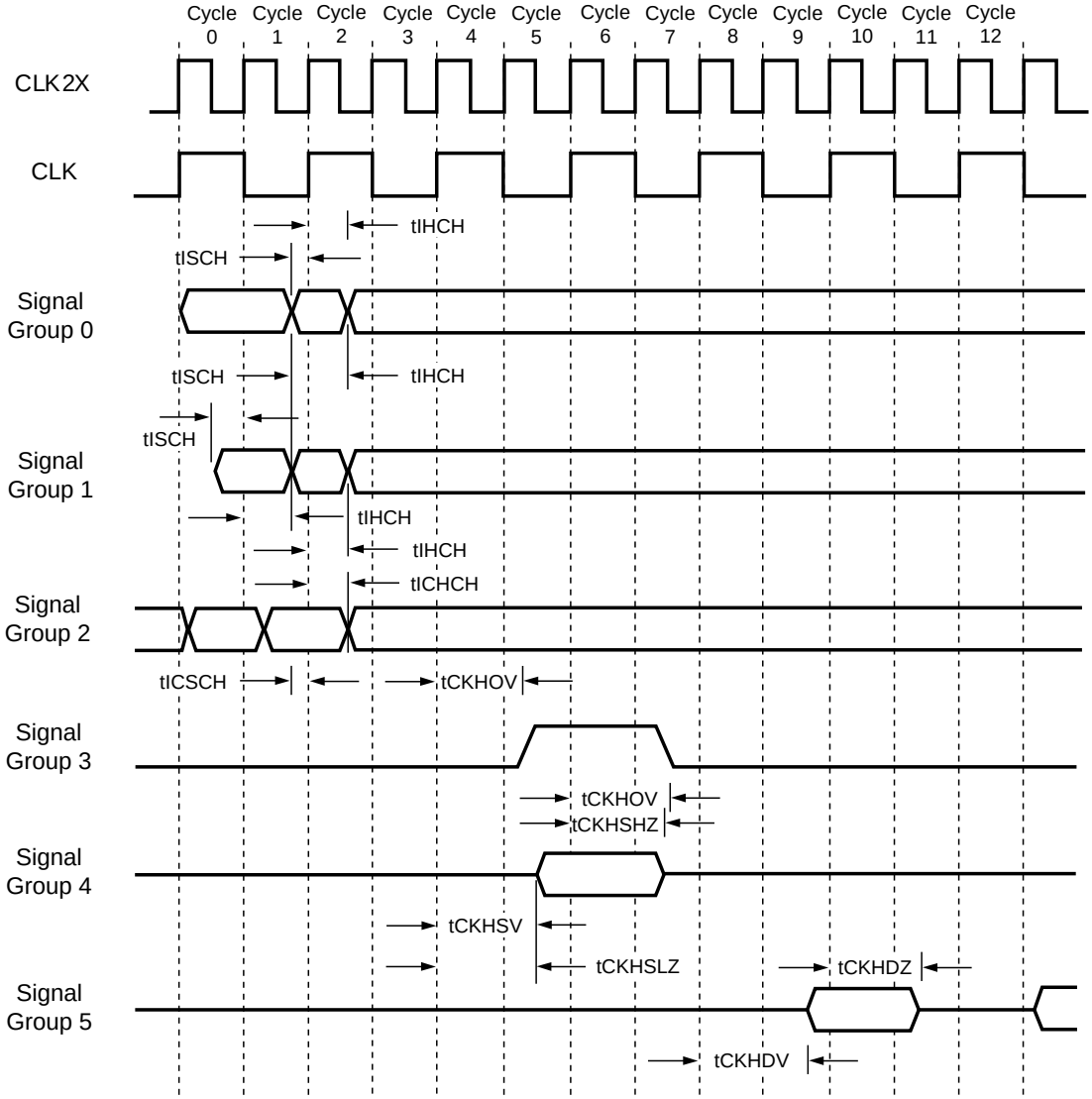
Note: 1. Effective capacitance measured with power supply. Sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs deselected.

Table 6. DC Characteristics

Sym	Parameter	Test Condition(1)	Min	Max	Unit
I_{LI}	Input Leakage Current	V_{DDQ} = V_{DDQ}(max), V_{IN} = 0 to V_{DDQ}(max)	–10	+10	µA
I_{LO}	Output Leakage Current	V_{DDQ} = V_{DDQ}(max), V_{IN} = 0 to V_{DDQ}(max)	–10	+10	µA
V_{IL}	Input Low Voltage (V_{DDQ} = 3.3V)		–0.3	0.8	V
V_{IH}	Input High Voltage (V_{DDQ} = 3.3V)		2.0	V_{DDQ} + 0.3	V
V_{IL}	Input Low Voltage (V_{DDQ} = 2.5V)		–0.3	0.7	V
V_{IH}	Input High Voltage (V_{DDQ} = 2.5V)		1.7	V_{DDQ} + 0.3	V
V_{IL}	Input Low Voltage (V_{DDQ} = 1.8V)		–0.3	0.35 * V_{DDQ}	V
V_{IH}	Input High Voltage (V_{DDQ} = 1.8V)		0.7 * V_{DDQ}	V_{DDQ} + 0.3	V
V_{OL}	Output Low Voltage (V_{DDQ} = 3.3V)	V_{DDQ} = V_{DDQ}(min), I_{OL} = 16mA		0.4	V
V_{OH}	Output High Voltage (V_{DDQ} = 3.3V)	V_{DDQ} = V_{DDQ}(min), I_{OH} = 8mA	2.4		V
V_{OL}	Output Low Voltage (V_{DDQ} = 2.5V)	V_{DDQ} = V_{DDQ}(min), I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage (V_{DDQ} = 2.5V)	V_{DDQ} = V_{DDQ}(min), I_{OH} = 8mA	2.0		V
V_{OL}	Output Low Voltage (V_{DDQ} = 1.8V)	V_{DDQ} = V_{DDQ}(min), I_{OL} = 8mA		0.45	V
V_{OH}	Output High Voltage (V_{DDQ} = 1.8V)	V_{DDQ} = V_{DDQ}(min), I_{OH} = 8mA	V_{DD} – 0.45		V
I_{DD1}	1.65V Supply Current at V_{DD}(max)	100MHz Search Rate		6.0	A
	1.5V Supply Current at V_{DD}(max)	83MHz Search Rate		5.0	A
	1.5V Supply Current at V_{DD}(max)	66MHz Search Rate		4.0	A
I_{DD2}	3.3V Supply Current at V_{DD}(max)	100MHz Search Rate, I_{OUT} = 0mA		350	mA
		83MHz Search Rate, I_{OUT} = 0mA		300	mA
		66MHz Search Rate, I_{OUT} = 0mA		240	mA
I_{DD2}	2.5V Supply Current at V_{DD}(max)	100MHz Search Rate, I_{OUT} = 0mA		350	mA
		83MHz Search Rate, I_{OUT} = 0mA		300	mA
		66MHz Search Rate, I_{OUT} = 0mA		240	mA

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{DD} = 1.5V.

Figure 8. AC Timing Waveforms with CLK2X



Signal Group 0: PHS_L, RST_L
Signal Group 1: DQ, CMD, CMDV
Signal Group 2: LHI, BHI, FULI
Signal Group 3: LHO, BHO, FULO, FULL
Signal Group 4: SADR, CE_L, OE_L, WE_L, ALE_L, SSF, SSV
Signal Group 5: DQ, ACK, EOT

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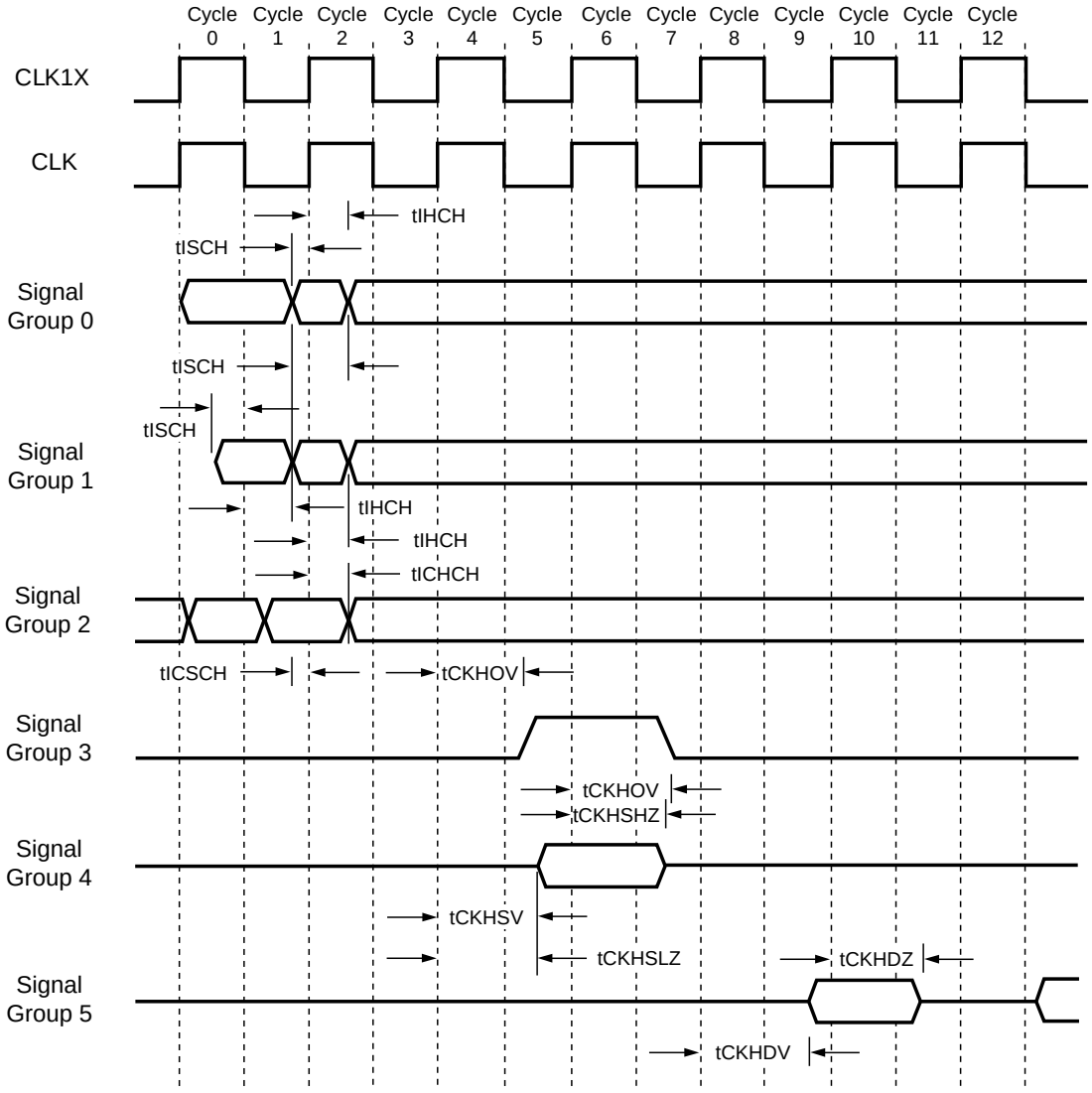
Figure 9. AC Timing Waveforms with CLK1X



Signal Group 0: PHS_L, RST_L
Signal Group 1: DQ, CMD, CMDV
Signal Group 2: LHI, BHI, FULI
Signal Group 3: LHO, BHO, FULO, FULL
Signal Group 4: SADR, CE_L, OE_L, WE_L, ALE_L, SSF, SSV
Signal Group 5: DQ, ACK, EOT

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Table 7. AC Timing Parameters with CLK2X

Row	Sym	M7040N-066 (V_{DDQ} = 3.3V, 2.5V)		M7040N-083 (V_{DDQ} = 3.3V, 2.5V, 1.8V)		M7040N-100 (V_{DDQ} = 3.3V, 2.5V)		Unit	Description(1)
		Min	Max	Min	Max	Min	Max		
1	f_{CLOCK}	40	133	40	166	40	200	MHz	CLK2X frequency
2	t_{CLOK}		0.5		0.5		0.5	ms	PLL lock time
3	t_{CKHI}	3.0		2.4		2.0		ns	CLK2X high pulse(2)
4	t_{CKLO}	3.0		2.4		2.0		ns	CLK2X low pulse(2)
5	t_{ISCH}	2.5		1.8		1.5		ns	Input Setup Time to CLK2X rising edge(2)
6	t_{IHCH}	0.6		0.6		0.5		ns	Input Hold Time to CLK2X rising edge(2)
7	t_{ICSCH}	4.2		3.5		3.0		ns	Cascaded Input Setup Time to CLK2X rising edge(2)
8	t_{ICHCH}	0.6		0.6		0.5		ns	Cascaded Input Hold Time to CLK2X rising edge(2)
9	t_{CKHOV}		8.5		7.0		6.5	ns	Rising edge of CLK2X to LHO, FULO, BHO, FULL valid(3)
10	t_{CKHDV}		9.0		7.5		7.0	ns	Rising edge of CLK2X to DQ valid(3)
11	t_{CKHDZ}		8.5		7.0		6.5	ns	Rising edge of CLK2X to DQ high-Z(4)
12	t_{CKHSV}		9.0		7.5		7.0	ns	Rising edge of CLK2X to SRAM bus valid(3)
13	t_{CKHSHZ}		6.5		6.0		5.5	ns	Rising edge of CLK2X to SRAM bus high-Z(4)
14	t_{CKHSLZ}	7.0		6.5		6.0		ns	Rising edge of CLK2X to SRAM bus low-Z(4)

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{DD} = 1.5V.
2. Values are based on 50% signal levels.
3. Based on an AC load of CL = 30pF (see Figure 5, Figure 6, and Figure 7, page 13).
4. These parameters are sampled and not 100% tested, and are based on an AC load of 5pF.

Table 8. AC Timing Parameters with CLK1X

Row	Sym	M7040N-066 (V_{DDQ} = 3.3V, 2.5V, 1.8V)		M7040N-083 (V_{DDQ} = 3.3V, 2.5V, 1.8V)		M7040N-100 (V_{DDQ} = 3.3V, 2.5V)		Unit	Description[1]
		Min	Max	Min	Max	Min	Max		
1	f_{CLOCK}	20	66	20	83	20	100	MHz	CLK1X frequency
2	t_{CLOK}		0.5		0.5		0.5	ms	PLL lock time
3	t_{CKHI}	6.75		5.4		4.5		ns	CLK1X high pulse[2]
4	t_{CKLO}	6.75		5.4		4.5		ns	CLK1X low pulse[2]
5	t_{ISCH}	2.5		1.8		1.5		ns	Input Setup Time to CLK1X edge[2]
6	t_{IHCH}	0.6		0.6		0.5		ns	Input Hold Time to CLK1X edge[2]
7	t_{ICSCH}	4.2		3.5		3.0		ns	Cascaded Input Setup Time to CLK1X rising edge[2]
8	t_{ICHCH}	0.6		0.5		0.5		ns	Cascaded Input Hold Time to CLK1X rising edge[2]
9	t_{CKHOV}		8.5		7.0		6.5	ns	Rising edge of CLK1X to LHO, FULO, BHO, FULL valid[3]
10	t_{CKHDV}		9.0		7.5		7.0	ns	Rising edge of CLK1X to DQ valid[3]
11	t_{CKHDZ}		8.5		7.0		6.5	ns	Rising edge of CLK1X to DQ high-Z[4]
12	t_{CKHSV}		9.0		7.5		7.0	ns	Rising edge of CLK1X to SRAM bus valid[3]
13	t_{CKHSHZ}		6.5		6.0		5.5	ns	Rising edge of CLK1X to SRAM bus high-Z[4]
14	t_{CKHSLZ}	7.0		6.5		6.0		ns	Rising edge of CLK1X to SRAM bus low-Z[4]

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{DD} = 1.5V.
2. Values are based on 50% signal levels and a 50/50% duty cycle of CLK1X.
3. Based on an AC load of CL = 30pF (see Figure 5, Figure 6, and Figure 7, page 13).
4. These parameters are sampled and not 100% tested, and are based on an AC load of 5pF.

OPERATION

Command Bus and DQ Bus

CMD[10:0] carries the command and its associated parameter. DQ[71:0] is used for data transfer to and from the database entries. These entries comprise a data and a mask field that are organized as data and mask arrays. The DQ Bus carries the search data (of the data and mask arrays and internal registers) during the SEARCH command as well as the address and data during READ and/or WRITE operations. The DQ Bus can also carry the address information for the flow-through accesses to the external SRAMs and/or SSRAMs.

Database Entry (Data Array and Mask Array)

Each database entry comprises a data and a mask field. The resultant value of the entry is “1,” “0,” or “X (don’t care),” depending on the value in the data and mask bits. The on-chip priority encoder selects the first matching entry in the database that is nearest to location “0.”

Arbitration Logic

When multiple Search Engines are cascaded to create large databases, the data being searched is presented to all Search Engines simultaneously in the cascaded system. If multiple matches occur within the cascaded devices, arbitration logic on the Search Engines will enable the winning device (with a matching entry that is closest to address “0” of the cascaded database) to drive the SRAM bus.

Pipeline and SRAM Control

Pipeline latency is added to give enough time to a cascaded system’s arbitration logic to determine the device that will drive the index of the matching entry on the SRAM bus. Pipeline logic adds latency to both the SRAM access cycles and the SSF and SSV signals to align them to the host ASIC receiving the associated data.

Full Logic

Bit[0] in each of the 72-bit entries has a special purpose for the LEARN command (0 = empty, 1 = full). When all the data entries have bit[0] = 1, the database asserts the FULL Flag, indicating all the Search Engines in the depth-cascaded array are full.

Connection Descriptions

CLOCK MODE (CLK_MODE). This signal allows the selection of clock input to the CLK1X/CLK2X pin. If the CLK_MODE pin is low, CLK2X must be supplied on that pin. PHS_L must also be supplied. If the CLK_MODE pin is high, CLK1X must be supplied on the CLK2X/CLK1X pin, and the PHS_L signal is not required. When the CLK_MODE is high, PHS_L is unused and should be externally grounded.

Master Clock (CLK2X/CLK1X). Depending on the CLK_MODE pin, either the CLK2X or the CLK1X must be supplied. M7040N samples control and data signals on both the edges of CLK1X if CLK1X is supplied. M7040N samples all the data and control pins on the positive edge of CLK2X if the CLK2X and PHS_L signals are supplied. All signals are driven out of the device on the rising edge of CLK1X if CLK1X is supplied, and are driven on the rising edge of CLK2X (when PHS_L is low) if CLK2X is supplied.

Phase (PHS_L). This signal runs at half the frequency of CLK2X and generates an internal clock from CLK2X (see Figure 10, page 21).

Test Output (TEST_CO). This is test output and will stay unconnected in the application of the device.

Test Input (TEST). This signal should be connected to ground.

Test Input (TEST_FM). This signal should be connected to ground.

Reset (RST_L). Driving RST_L low initializes the device to a known state.

Test Input (TEST_PB). This signal should be connected to ground.

Configuration. When CFG_L is low, M7040N will operate in backward compatibility mode with M7010 and M7020. When CFG_L is low, the CMD[10:9] should be externally grounded. With CFG_L low, the device will behave identically with M7010 and M7020, and the new feature added to M7040N will be disabled.

When CFG_L is high, the additional command CMD[10:9] can be used and the following additional features will be supported:

1. 16 pairs of Global Masks are supported instead of eight;
2. Parallel WRITE to the data and mask arrays is supported (see Parallel WRITE, page 38); and
3. configuring tables of up to three different widths does not require table identification bits in the data array, thus saving two bits from each 72-bit

Command Bus (CMD[10:0]. [1:0] specifies the command; [10:2] contains the command parameters. The descriptions of individual commands explains the details of the parameters. The encoding of commands based on the [1:0] field are:

– 00: PIO READ

– 01: PIO WRITE

– 10: SEARCH

– 11: LEARN

Command Valid (CMDV). Qualifies the CMD bus as follows:

– 0: No Command

– 1: Command

Address/Data Bus (DQ[71:0]). Carries the Read and WRITE address as well as the data during register, data, and mask array operations. It carries the compare data during search operations. It also carries the SRAM address during SRAM PIO accesses.

READ Acknowledge (ACK). Indicates that valid data is available on the DQ Bus during register, data, and mask array READ operations, or the data is available on the SRAM data bus during SRAM READ operations.

Note: ACK Signals require a weak external pull-down resistor such as 47 or 100 KΩ.

End of Transfer (EOT). Indicates the end of burst transfer during READ or WRITE burst operations.

Note: EOT Signals require a weak external pull-down resistor such as 47 KΩ or 100 KΩ.

SEARCH Successful Flag (SSF). When asserted, this signal indicates that the device is the global winner in a SEARCH operation.

SEARCH Successful Flag Valid (SSV). When asserted, this signal qualifies the SSF signal.

Multiple Hit Flag (MULTI_HIT). When asserted, this signal indicates that there is more than one location having a match on this device.

High Speed (HIGH_SPEED). When this signal is high, the device will run up to 100MHz and perform 100 million searches per second. However, in this mode, a TLSZ value of '00' is not supported in a system of a single device. Furthermore, the device will only support a TLSZ of '00' and '01' if more than one device is cascaded to form database tables.

Clock Tune [3:0] (CLK_TUNE[3:0]). These test pins should be set to logic level 1001.

SRAM Address (SADR[23:0]). This bus contains address lines to access off-chip SRAMs that contain associative data. See Table 52, page 128 for the details of the generated SRAM address. In a database of multiple M7040Ns, each corresponding bit of SADR from all cascaded devices must be connected.

SRAM Chip Enable (CE_L). This is Chip Enable control for external SRAMs. In a database of multiple M7040Ns, CE_L of all cascaded devices must be connected. This signal is then driven by only one of the devices.

SRAM Write Enable (WE_L). This is Write Enable control for external SRAMs. In a database of multiple M7040Ns, WE_L of all cascaded devices must be connected together. This signal is then driven by only one of the devices.

SRAM Output Enable (OE_L). This is Output Enable control for external SRAMs. Only the last device drives this signal (with the LRAM bit set).

Address Latch Enable (ALE_L). When this signal is low, the addresses are valid on the SRAM Address Bus. In a database of multiple M7040Ns, the ALE_L of all cascaded devices must be connected. This signal is then driven by only one of the devices.

Local Hit In (LHI[6:0]). These pins depth-cascade the device to form a larger table size. One signal of this bus is connected to the LHO[1] or LHO[0] of each of the upstream devices in a block. Connect all unused LHI pins to a logic '0.' (For more information, see DEPTH-CASCADING, page 124.)

Local Hit Out (LHO[1:0]). LHO[1] and LHO[0] are the same logical signal. LHO[1] or LHO[0] is connected to one input of the LHI bus of up to four downstream devices (in a block that contains up to eight devices). (For more information, see DEPTH-CASCADING, page 124.)

Block Hit In (BHI[2:0]). Inputs from the previous BHO[2:0] are tied to the BHI[2:0] of the current device (see DEPTH-CASCADING, page 124). In a four-block system, the last block can contain only seven devices because the ID code 11111 is used for broadcast access.

Block Hit Out (BHO[2:0]). These outputs from the last device in a block are connected to the BHI[2:0] inputs of the devices in the downstream blocks (see DEPTH-CASCADING, page 124).

Full In (FULI[6:0]). Each signal in this bus is connected to FULO[0] or FULO[1] of an upstream device to generate the FULL signal for the depth-cascaded block. For more information, see DEPTH-CASCADING, page 124 to Generate Full for a Block Section.

Full Out (FULO[1:0]). FULO[1] and FULO[0] are the same logical signal. One of these two signals must be connected to the FULI of up to four downstream devices in a depth-cascaded table. Bit [0] in the data array indicates if the entry is full (1) or empty (0).This signal is asserted if all of the bits in the data array are '1s.' Refer to Depth-Cascading to Generate a “FULL” Signal, page 124.

Full Flag (FULL). When asserted, this signal indicates that the table consisting of many depth-cascaded devices is full.

Device Identification (ID[4:0]). The binary-encoded device ID for a depth-cascaded system starts at 00000 and goes up to 11110. 11111 is reserved for a special broadcast address that selects all cascaded search engines in the system. On a broadcast read-only, the device with the LDEV bit set to '1' responds.

Chip Core Supply (V_{DD}). This is equal to 1.5V.

Chip I/O Supply (V_{DDQ}). This is equal to either 2.5 or 3.3V.

Test Data In (TDI). This is the Test Access Port’s Test Data In.

Test Clock (TCK). This is the Test Access Port’s Test Clock.

Test Data Out (TDO). This is the Test Access Port’s Test Data Out.

Test Mode Select (TMS). This is the Test Access Port’s Test Mode Select.

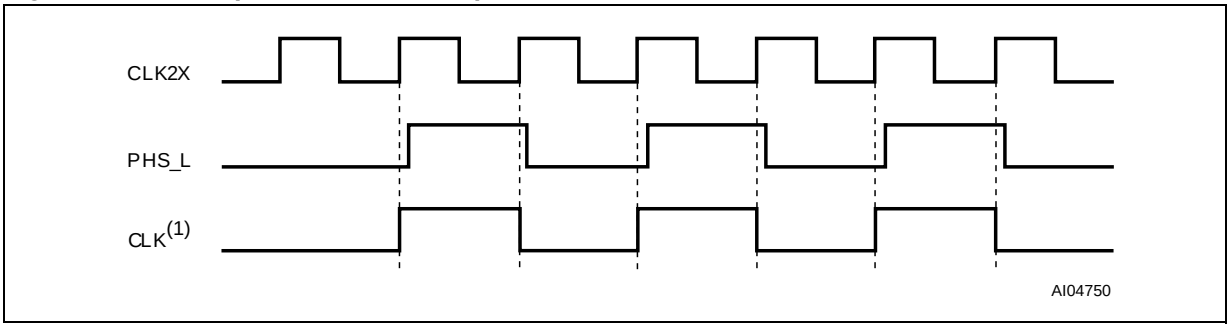
Test Reset (TRST_L). This is the Test Access Port’s Test Reset.

CLOCKS

If the CLK_MODE pin is low, M7040N receives the CLK2X and PHS_L signals. It uses the PHS_L signal to divide CLK2X and generate an internal clock (CLK), as shown in Figure 10. The M7040N uses CLK2X and CLK for internal operations. If the CLK_MODE pin is high, the M7040N receives the CLK1X only. the M7040N uses an internal PLL to double the frequency of CLK1X and then divides that clock by two to generate a CLK for internal operations, as shown in Figure 11.

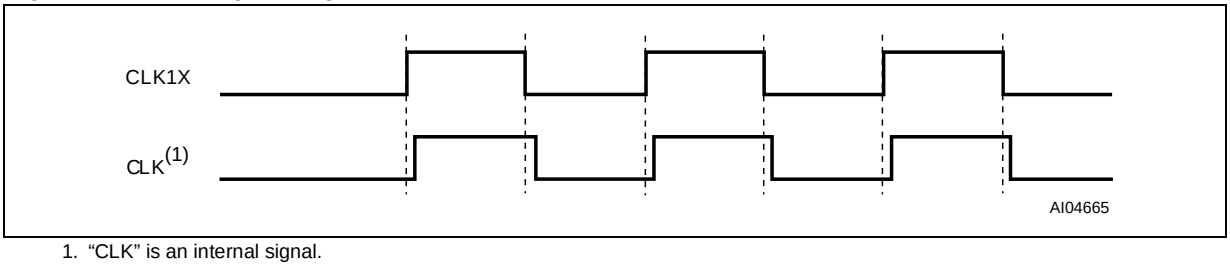
Note: For the purpose of showing timing diagrams, all such diagrams in this document will be shown in CLK2X mode. For a timing diagram in CLK1X mode, the following substitution can be made (see Figure 12).

Figure 10. Clocks (CLK2X and PHS_L)



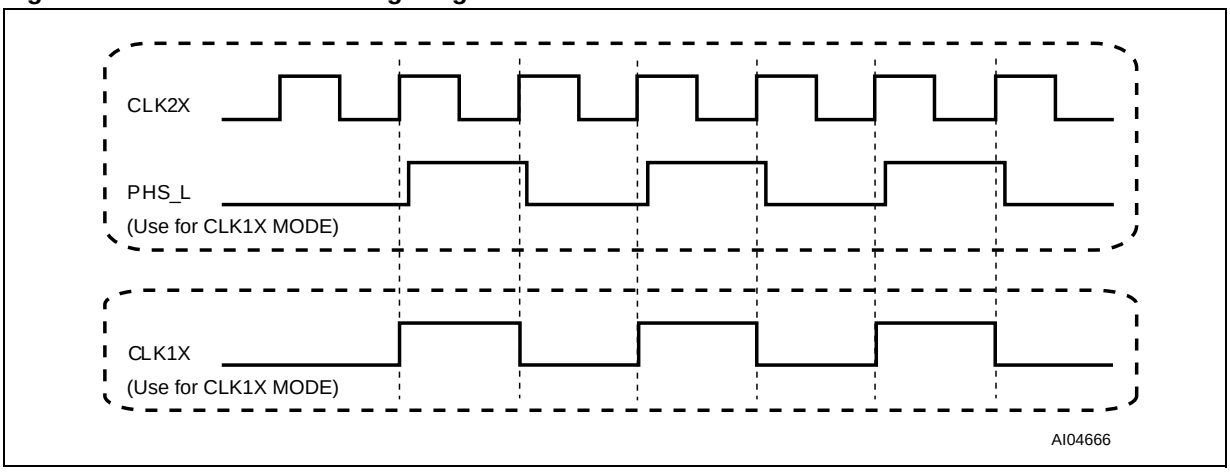
Note: Any reference to “CLK Cycles” means 1 cycle of the signal, “CLK.”
1. “CLK” is an internal signal.

Figure 11. Clocks (CLK1X)



1. “CLK” is an internal signal.

Figure 12. Clocks for All Timing Diagrams



PLL USAGE

When the device first powers up, it takes 0.5 ms to lock the internal phase-lock loop (PLL). During this locking of the PLL, in addition to 32 extra CLK1X cycles in CLK1X mode and 64 extra cycles in CLK2X mode, the RST_L must be held low for proper initialization of the device. Setup and hold requirements will change in CLK1X mode if the duty cycle of the CLK1X is varied. All signals into the device in CLK1X mode are sampled by a clock that is generated by multiplying CLK1X by two. Since PLL has a locking range, the device will only work between the range of frequencies specified in the timing specification section.

REGISTERS

All registers in the M7040N are 72 bits wide. The M7040N contains 16 pairs of comparand storage registers, 16 pairs of global mask registers (GMRs), eight search successful index registers and one each of command, information, burst READ, burst WRITE, and next-free address registers. Table 9 provides an overview of all the M7040N registers. The registers are ordered in ascending address order. Each register group is then described in the following subsections.

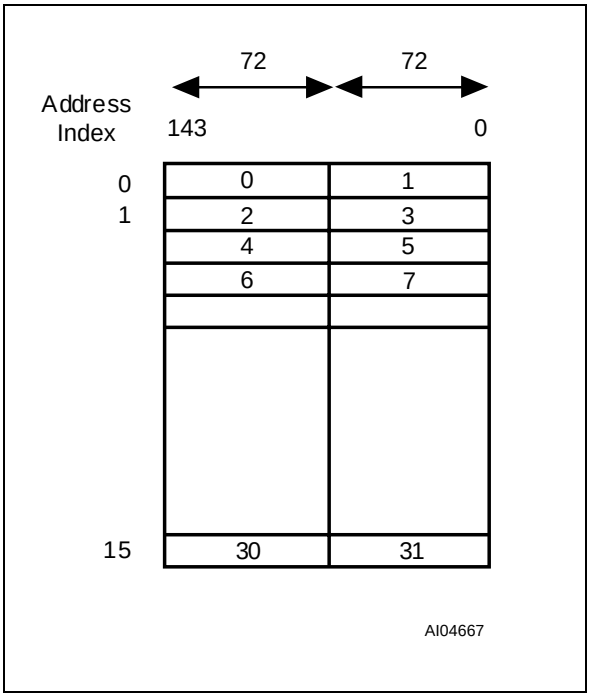
Table 9. Register Overview

Address	Abbreviation	Type	Name
0–31	COMP0–31	R	32 Comparand Registers. Stores comparands from the DQ Bus for learning later.
32–47, 96–111	MASKS	RW	16 Global Mask Registers Pairs.
48–55	SSR0–7	R	8 SEARCH Successful Index Registers.
56	COMMAND	RW	Command Register.
57	INFO	R	Information Register.
58	RBURREG	RW	Burst Read Register.
59	WBURREG	RW	Burst Write Register.
60	NFA	R	Next Free Address Register.
61–63	–	–	Reserved

Comparand Registers

The device contains 32 72-bit comparand registers (16 pairs) dynamically selected in every SEARCH operation to store the comparand presented on the DQ Bus. The LEARN command will later use these registers when executed. The M7040N stores the SEARCH command's Cycle A comparand in the even-numbered register and the Cycle B comparand in the odd-numbered register, as shown in Figure 13.

Figure 13. Comparand Register Selection During SEARCH and LEARN Instructions



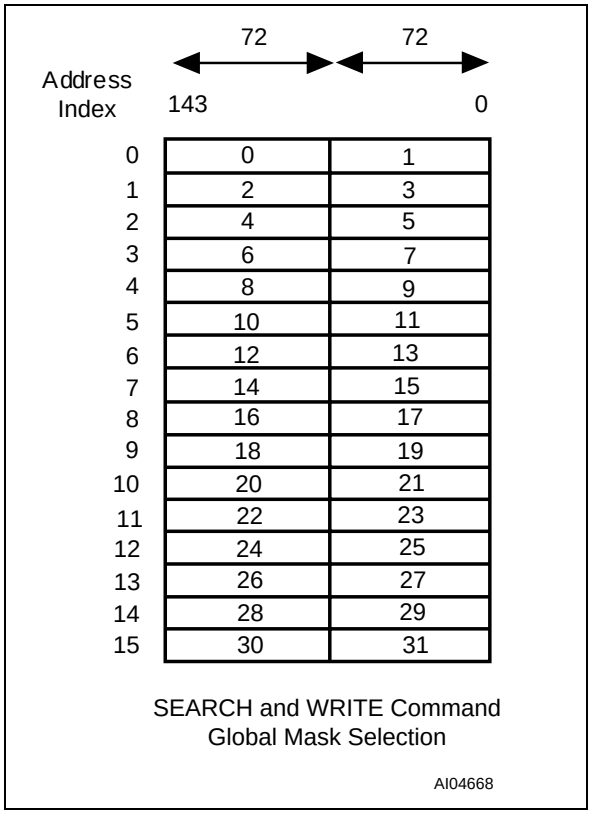
Mask Registers

The device contains 32 72-bit global mask registers (16 pairs) dynamically selected in every SEARCH operation to select the search subfield. The addressing of these registers is explained in Figure 14. The four-bit GMR Index supplied on the command (CMD) bus can apply 16 pairs of global masks during the SEARCH and WRITE operations, as shown below.

Note: In 72-bit SEARCH and WRITE operations, the host ASIC must program both the even and odd mask registers with the same values.

Each mask bit in the GMRs is used during SEARCH and WRITE operations. In SEARCH operations, setting the mask bit to '1' enables compares; setting the mask bit to '0' disables compares (forced match) at the corresponding bit position. In WRITE operations to the data or mask array, setting the mask bit to '1' enables WRITEs; setting the mask bit to '0' disables WRITEs at the corresponding bit position.

Figure 14. Addressing the Global Masks Register Array



SEARCH-Successful Registers (SSR[0:7])

The device contains eight search successful registers (SSRs) to hold the index of the location where a successful search occurred. The format of each register is described in Table 10. The SEARCH command specifies which SSR stores the index of a specific SEARCH command in Cycle B of the SEARCH Instruction. Subsequently, the host ASIC can use this register to access that data array, mask array, or external SRAM using the index as part of the indirect access address (see Table 20, page 34 and Table 23, page 37).

The device with a valid bit set performs a READ or WRITE operation. All other devices suppress the operation.

Table 10. SEARCH-Successful Register (SSR) Description

Field	Range	Initial Value	Description
INDEX	[15:0]	X	**Index.** This is the address of the 72-bit entry where a successful search occurs. The device updates this field only when a search is successful. If a hit occurs in a 144-bit entry-size quadrant, the LSB is '0.' If a hit occurs in a 288-bit entry size quadrant, the two LSBs are '00.' This index updates if the device is either a local or global winner in a SEARCH operation.
–	[30:16]	0	Reserved.
VALID	[31]	0	**Valid.** During SEARCH operation in a depth-cascaded configuration, the device that is a global winner in a match sets this bit to '1.' This bit updates only when the device is a global winner in a SEARCH operation.
–	[71:32]	0	Reserved.

The Command Register

Table 11. Command Register Field Descriptions

Field	Range	Initial Value	Description
SRST	[0]	0	**Software Reset.** If '1,' this bit resets the device, with the same effect as the hardware reset. Internally, it generates a reset pulse lasting for eight CLK cycles. This bit automatically resets to a '0' the reset cycle has completed.
DEVE	[1]	0	**Device Enable.** If '0,' it keeps the SRAM Bus (SADR, WE_L, CE_L, OE_L, and ALE_L), SSF, and SSV signals in 3-state condition and forces the cascade interface output signals LHO[1:0] and BHO[2:0] to '0.' It also keeps the DQ Bus in input mode. The purpose of this bit is to make sure that there are no bus contentions when the devices power up in the system.
TLSZ	[3:2]	01	**Table Size.** The host ASIC must program this field to configure the chips into a table of a certain size. This field affects the pipeline latency of the SEARCH and LEARN operations as well as the READ and WRITE accesses to the SRAM (SADR[23:0], CE_L, OE_L, WE_L, ALE_L, SSV, SSF, and ACK). Once programmed, the search latency stays constant. Latency # CLK Cycles with HIGH_SPEED low 00: 1 device — 4 01: 2-8 devices — 5 10: 9-31 devices — 6 11: Reserved Latency # CLK Cycles with HIGH_SPEED high 00: Not supported 01: 1 devices — 5 10: 2-31 devices — 6 11: Reserved
HLAT	[6:4]	000	**Latency of Hit Signals.** This field adds latency to the SSF and SSV signals during SEARCH, and ACK signal during SRAM READ access by the following number of CLK cycles. 000: 0 — 100: 4 001: 1 — 101: 5 010: 2 — 110: 6 011: 3 — 111: 7
LDEV	[7]	0	**Last device in the cascade.** When set, this is the last device in the depth-cascaded table and is the default driver for the SSF and SSV signals. In the event of a search failure, the device with this bit set drives the hit signals as follows: SSF = 0, SSV = 1 During non-search cycles, the device with this bit set drives the signals as follows: SSF = 0, SSV = 0

Field	Range	Initial Value	Description
LRAM	[8]	0	**Last device on this SRAM Bus.** When set, this device is the last device on this SRAM bus in the depth-cascaded table and is the default driver for the SADR, CE_L, WE_L, and ALE_L signals. In cycles where no M7040N device in a depth-cascaded table drives these signals, this device drives the signals as follows: SADR = FFFFFF, CE_L = 1 WE_L = 1 ALE_L = 1 OE_L is always driven by the device for which this bit is set.
CFG	[24:9]	0000 0000 0000 0000	**Database Configuration.** The device is internally divided into eight quadrants of 8K x 72, each of which can be configured as 8K x 72, 4K x 144, or 2K x 288 as follows: 00: 8K x 72 01: 4K x 144 10: 2K x 288 11: low power, partition not used for SEARCH Bits [10:9] apply to configuring the 1st quadrant in the address space. Bits [12:11] apply to configuring the 2nd quadrant in the address space. Bits [14:13] apply to configuring the 3rd quadrant in the address space. Bits [16:15] apply to configuring the 4th quadrant in the address space. Bits [18:17] apply to configuring the 5th quadrant in the address space. Bits [20:19] apply to configuring the 6th quadrant in the address space. Bits [22:21] apply to configuring the 7th quadrant in the address space. Bits [24:23] apply to configuring the 8th quadrant in the address space.
	[71:25]	0	Reserved.

The Information Register

Table 12. Information Register Field Descriptions

Field	Range	Initial Value	Description
Revision	[3:0]	0001	**Revision Number.** This is the current device revision number. Numbers start from one and increment by one for each revision of the device.
Implementation	[6:4]	001	This is the M7040N implementation number.
Reserved	[7]	0	Reserved.
Device ID	[15:8]	00000100	This is the Device Identification Number.
MFID	[31:16]	0000_0010_0000_1111	**Manufacturer ID.** This field is the same as the manufacturer ID and continuation bits in the TAP controller.
	[71:32]		Reserved.

The Read Burst Address Register (RBURREG)

These READ burst address register fields must be programmed before burst read.

Table 13. Read Burst Register Description

Field	Range	Initial Value	Description
ADR	[15:0]	0	**Address.** This is the starting address of the data array or mask array during a burst READ operation. It automatically increments by 1 for each successive read of the data array or mask array. Once the operation is complete, the contents of this field must be reinitialized for the next operation.
	[18:16]		Reserved.
BLEN	[27:19]	0	**Length of Burst Access.** The device is capable of writing from 4 up to 511 locations in a single burst. The BLEN decrements automatically. Once the operation is complete, the contents of this field must be reinitialized for the next operation.
	[71:28]		Reserved.

The Write Burst Address Register (WBURREG)

These WRITE burst address register fields must be programmed before burst write.

Table 14. Write Burst Register Description

Field	Range	Initial Value	Description
ADR	[15:0]	0	**Address.** This is the starting address of the data array or mask array during a burst WRITE operation. It automatically increments by 1 for each successive write of the data array or mask array. Once the operation is complete, the contents of this field must be reinitialized for the next operation.
	[18:16]		Reserved.
BLEN	[27:19]	0	**Length of Burst Access.** The device is capable of writing from 4 up to 511 locations in a single burst. The BLEN decrements automatically. Once the operation is complete, the contents of this field must be reinitialized for the next operation.
	[71:28]		Reserved.

The NFA Register

Bit [0] of each 72-bit data entry is a special bit designated for use in the operation of the LEARN command. In 72-bit quadrants, the bit[0] indicates whether a location is full (bit set to '1') or empty (bit set to '0'). Every WRITE/LEARN command loads the address of first 72-bit location that contains a '0' in the entry's bit[0]. This is stored in the NFA register (see Table 15). If all the bits in a device are set to '1,' the M7040N asserts FULO[1:0] to '1.'

In 144-bit-configured quadrants, the LSB of this register is always set to '0.' The host ASIC must set bit '0' and bit 72 in a 144-bit word to either '0' or '1' to indicate full/empty status.

Note: Both bits (0 and 72) must be set to '0' or '1' (e.g., '10' or '01' settings are invalid).

Table 15. NFA Register

Address	71 - 16	15 - 0
60	Reserved	Index

SEARCH ENGINE ARCHITECTURE

The M7040N consists of 64K x 72-bit storage cells referred to as data bits. There is a mask cell corresponding to each data cell. Figure 15 shows the three organizations of the device based on the value of the CFG bits in the command register.

During a SEARCH operation, the search data bit (S), data array bit (D), mask array bit (M) and the global mask bit (G) are used in the following manner to generate a match at that bit position (see Table 16, page 29).

The entry with all matched bit positions results in a successful search during a SEARCH operation.

In order for a successful search within a device to make the device the local winner in the SEARCH operation, all 72-bit positions must generate a match for a 72-bit entry in 72-bit-configured quadrants, or all 144-bit positions must generate a match for two consecutive even and odd 72-bit entries in quadrants configured as 144 bits, or all 288-bit positions must generate a match for 4 consecutive entries aligned to 4 entry-page boundaries of 72-bit entries in quadrants configured as 288 bits.

An arbitration mechanism using a cascade bus determines the global winning device among the local winning devices in a SEARCH cycle. The global winning device drives the SRAM Bus, SSV, and the SSF signals. In case of a SEARCH failure, the devices with the LDEV and LRAM bits set drive(s) the SRAM Bus, SSF, and SSV signals

The M7040N device can be configured to contain tables of different widths, even within the same chip. Figure 16, page 29 shows a sample configuration of different widths.

Data and Mask Addressing

Figure 17, page 29 shows the M7040N data array and mask array addressing procedure.

Figure 15. M7040N Database Width Configuration

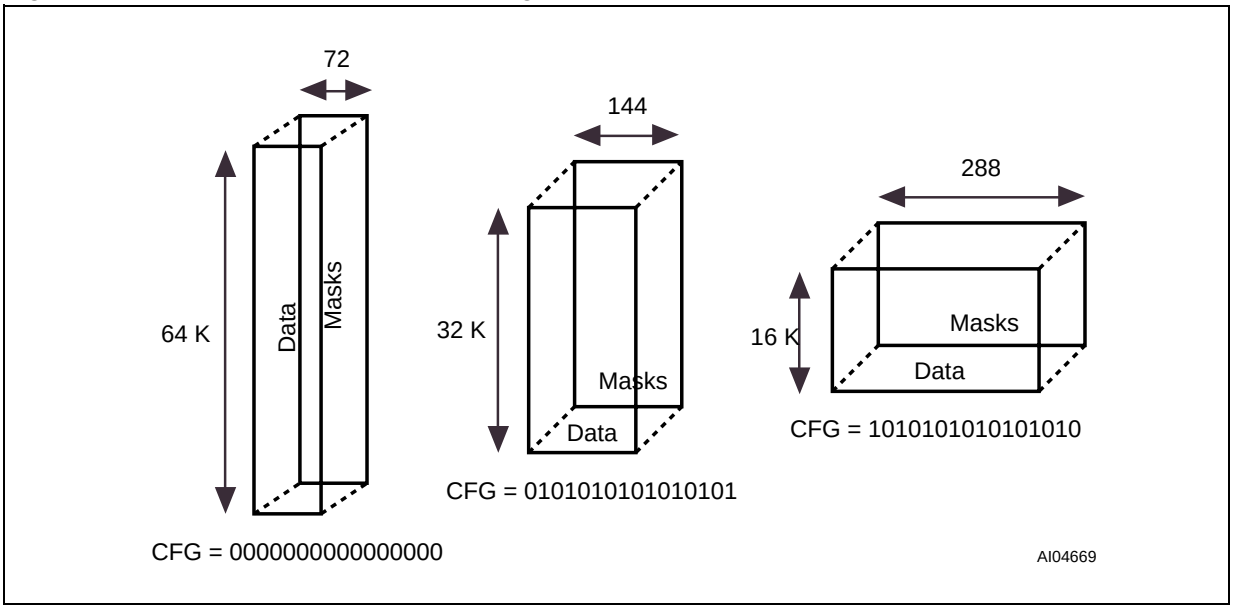


Table 16. Bit Position Match

G	M	S	D	Match
0	X	X	X	1
1	0	X	X	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Figure 16. Multi-width Configuration Example

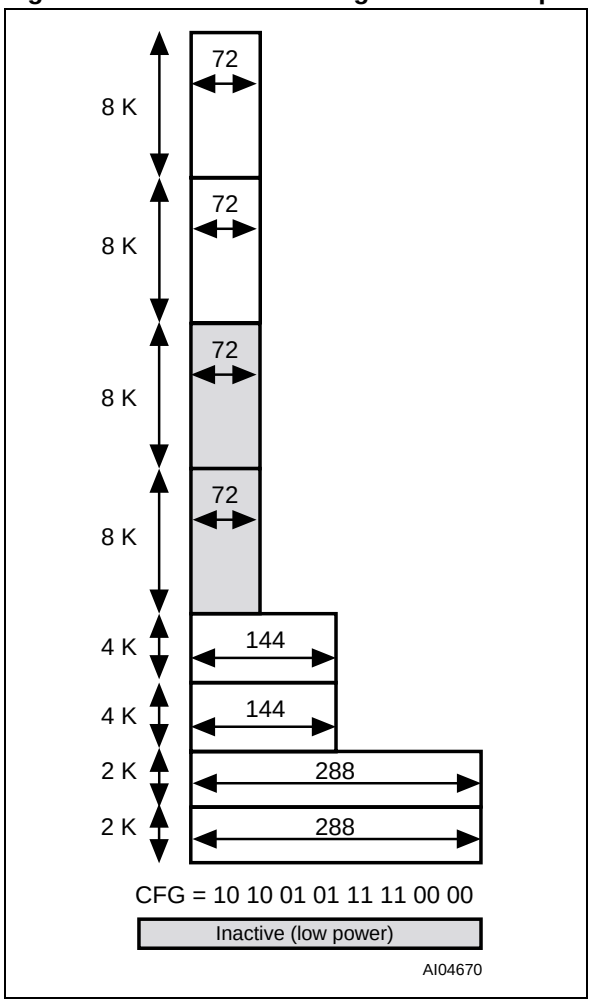
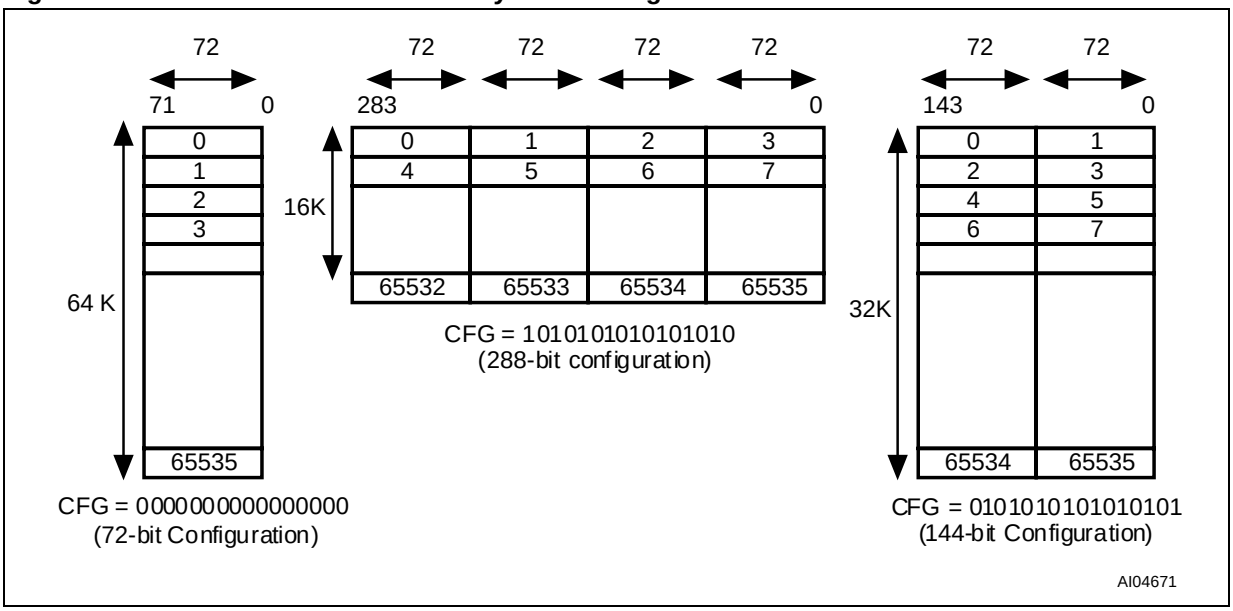


Figure 17. M7040N Data and Mask Array Addressing



COMMAND CODES AND PARAMETERS

A master device, such as an ASIC controller, issues commands to the M7040N using the Command Valid CMDV signal and the CMD Bus. The following subsections describe the functions of the commands.

Command Codes

The M7040N implements four basic commands shown in Table 17. The Command Code must be presented to CMD[1:0] while keeping the command valid (CMDV) signal high for two CLK2X cycles. These two CLK2X cycles are designated as “Cycle A” and “Cycle B” when the CLK_MODE pin is low. In CLK2X mode, the controller ASIC must align the instructions with the PHS_L signal. The command code must be presented to CMD[1:0] while keeping the CMDV signal high for one CLK1X cycle when the CLK_MODE pin is high. In CLK1X mode the high phase of the CLK1X is designated as Cycle A and the low phase of the CLK1X is designated as Cycle B. The CMD[10:2] field passes the parameters of the command in Cycles A and B.

Commands and Command Parameters

Table 18, page 31 lists the CMD bus fields that contain the M7040N command parameters as well as their respective cycles.

Table 17. Command Codes

CMD Code	Command	Description
00	READ	Reads one of the following: data array, mask array, device registers, or external SRAM.
01	WRITE	Writes one of the following: data array, mask array, device registers, or external SRAM.
10	SEARCH	Searches the data array for a desired pattern using the specified register from the global mask register array and local mask associated with each data cell.
11	LEARN	The device has internal storage for up to 16 comparands that it can learn. The device controller can insert these entries at the next free address (as specified by the NFA register) using the LEARN Instruction.

Table 18. Command Parameters

Cmd[1, 2]	Cyc	10	9	8	7	6	5	4	3	2	1	0
READ	A	X	X	SADR [23]	SADR [22]	SADR [21]	0	0	0	0 = Single 1 = Burst	0	0
	B	X	X	0	0	0	0	0	0	0 = Single 1 = Burst	0	0
WRITE	A	Global Mask Register Index [3]	0 Normal WRITE 1 Parallel WRITE	SADR [23]	SADR [22]	SADR [21]	Global Mask Register Index [2:0]			0 = Single 1 = Burst	0	1
	B	Global Mask Register Index [3]	0 Normal WRITE 1 Parallel WRITE	0	0	0	Global Mask Register Index [2:0]			0 = Single 1 = Burst	0	1
SEARCH	A	Global Mask Register Index [3]	72-bit: 0 144-bit: 1 288-bit:X	SADR [23]	SADR [22]	SADR [21]	Global Mask Register Index [2:0]			72-bit or 144-bit: 0 288-bit: 1 in 1st Cycle 0 in 2nd Cycle	1	0
	B	X		Successful SEARCH Register Index[2:0]			Comparand Register Index				1	0
LEARN[3]	A	X	X	SADR [23]	SADR [22]	SADR [21]	Comparand Register Index				1	1
	B	X	X	0	0	Mode 0: 72-bit 1: 144-bit	Comparand Register Index				1	1

Note: 1. Use only CMD[8:0] and connect the CMD[10:9] to ground with CFG_L low.
2. For a description of CMD[9] and CMD[2] see subsections on search 288-bit configured tables and mixed-size searches with CFG_L high.
3. The 288-bit-configured devices or 288-bit-configured quadrants within devices do not support the LEARN Instruction.

READ COMMAND

The READ can be a single read of a data array, a mask array, an SRAM, or a register location (CMD[2] = 0). It can be a burst READ (CMD[2] = 1) or mask array locations using an internal auto-incrementing address register (RBURADR). Table 19, page 34 describes each type of READ command.

A single-location READ operation lasts six cycles, as shown in Figure 18, page 33. The burst READ adds two cycles for each successive READ. The SADR[23:21] bits supplied in the READ Instruction Cycle A drive SADR[23:21] signals during the READ of an SRAM location.

The single READ operation takes six CLK cycles, in the following sequence:

– **Cycle 1:** The host ASIC applies the READ Instruction on the CMD[1:0] (CMD[2] = 0), using CMDV = 1, and the DQ Bus supplies the address, as shown in Table 20, page 34 and Table 21, page 35. The host ASIC selects the M7040N for which ID[4:0] matches the DQ[25:21] lines. If the DQ[25:21] = 11111, the host ASIC selects the M7040N with the LDEV Bit set. The host ASIC also supplies SADR[23:21] on CMD[8:6] in Cycle A of the READ Instruction if the READ is directed to the external SRAM.
– **Cycle 2:** The host ASIC floats DQ[71:0] to 3-state condition.
– **Cycle 3:** The host ASIC keeps DQ[71:0] in 3-state condition.
– **Cycle 4:** The selected device starts to drive the DQ[71:0] Bus and drives the ACK signal from Z to low.
– **Cycle 5:** The selected device drives the read data from the addressed location on the DQ[71:0] Bus and drives the ACK signal high.
– **Cycle 6:** The selected device floats DQ[71:0] to 3-state condition and drives the ACK signal low.

At the termination of Cycle 6, the selected device releases the ACK line to 3-state condition. The READ Instruction is complete, and a new operation can begin.

Note: The latency of the SRAM READ will be different than the one described above (see SRAM PIO Access, page 128). Table 20, page 34 lists and describes the format of the READ address for a data array, mask array, or SRAM.

In a burst READ operation, the READ lasts 4 + 2n CLK-cycles (where “n” stands for the number of accesses in the burst specified by the BLEN field of the RBURREG). Table 21, page 35 describes the READ address format for the internal registers. Figure 19, page 33 illustrates the timing diagram for the burst READ of the data or mask array. This operation assumes that the host ASIC has programmed the RBURREG with the starting address (ADR) and the length of transfer (BLEN) before initiating the burst READ command.

– **Cycle 1:** The host ASIC applies the READ Instruction on the CMD[1:0] (CMD[2] = 1), using CMDV=1 and the address supplied on the DQ Bus, as shown in Table 22, page 35. The host ASIC selects the M7040N for which ID[4:0] matches the DQ[25:21] lines. If the DQ[25:21] = 11111, the host ASIC selects the M7040N with the LDEV Bit set.
– **Cycle 2:** The host ASIC floats DQ[71:0] to the 3-state condition.
– **Cycle 3:** The host ASIC keeps DQ[71:0] in the 3-state condition.
– **Cycle 4:** The selected device starts to drive the DQ[71:0] Bus and drives ACK and EOT from Z to low.
– **Cycle 5:** The selected device drives the READ data from the addressed location on the DQ[71:0] Bus and drives the ACK signal high.

  Note: Cycles four and five repeat for each additional access until all the accesses specified in the burst length (BLEN) field of RBURREG are complete. On the last transfer, the M7040N drives the EOT signal high.
– **Cycle (4 + 2n):** The selected device drives the DQ[71:0] to 3-state condition and drives the ACK and the EOT signals low.

At the termination of Cycle 4 + 2n, the selected device floats the ACK line to 3-state condition. The burst READ Instruction is complete, and a new operation can begin (see Table 22, page 35 for burst READ address formats).

Figure 18. Single Location READ Cycle Timing

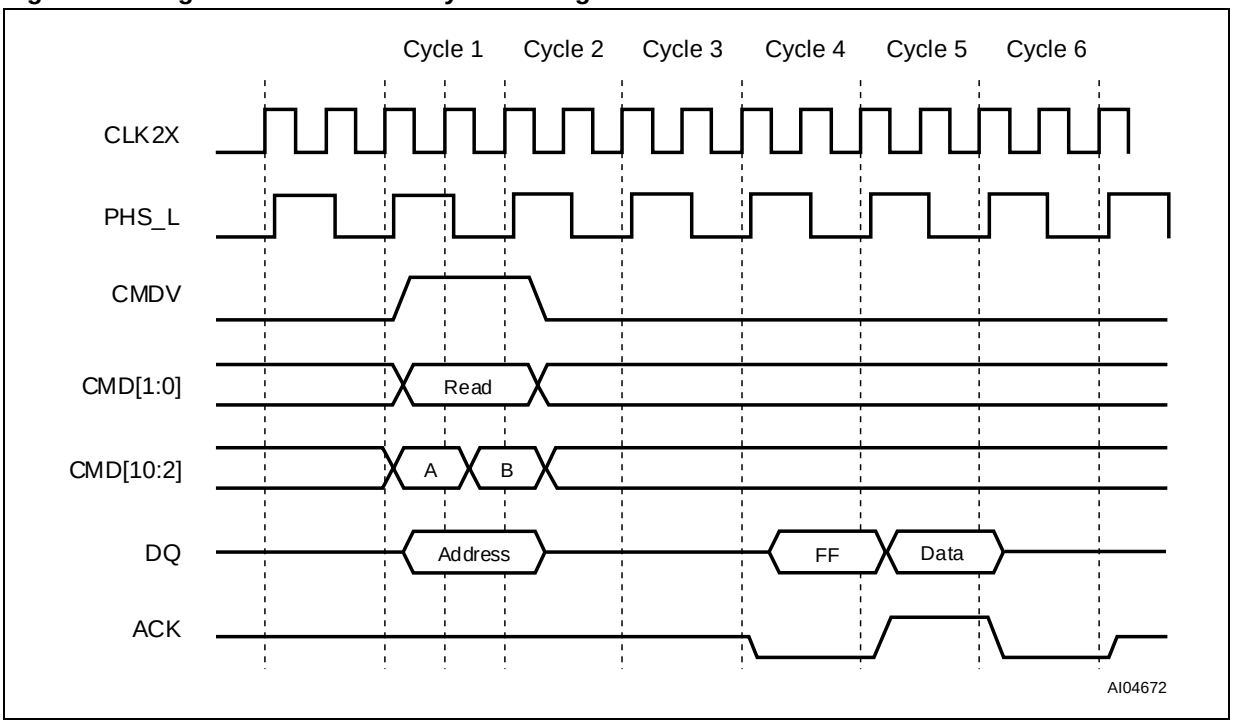


Figure 19. Burst READ of the Data and Mask Arrays (BLEN = 4)

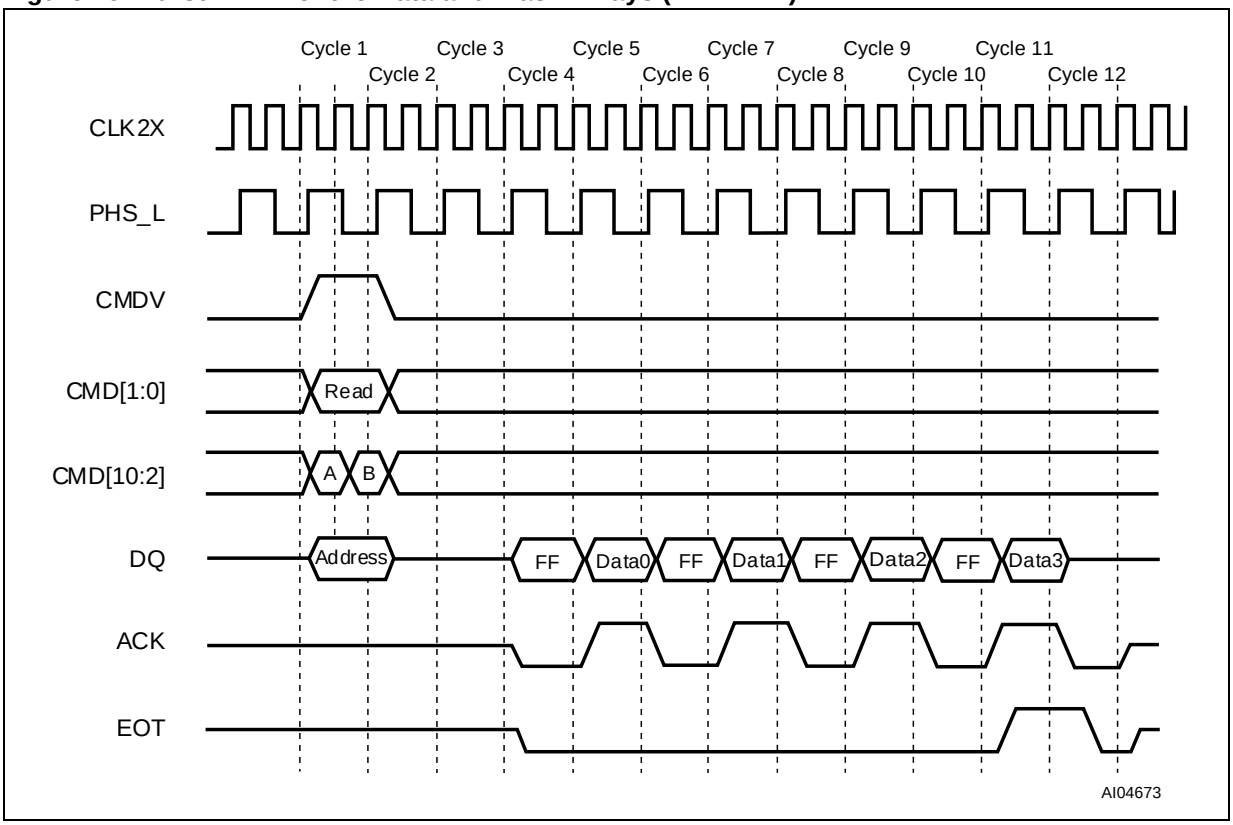


Table 19. READ Command Parameters

CMD Parameter CMD[2]	Read Command	Description
0	Single Read	Reads a single location of the data array, mask array, external SRAM, or device registers. All access information is applied on the DQ Bus.
1	Burst Read	Reads a block of locations from the data array or mask array as a burst. The internal register (RBURADR) specifies the starting address and the length of the data transfer from the data array or mask array, and it auto-increments the address for each access. All other access information is applied on the DQ Bus. **Note:** The device registers and external SRAM can only be read in single-read mode.

Table 20. Data and Mask Array, SRAM Read Address Format

DQ [71:30]	DQ [29]	DQ [28:26]	DQ [25:21]	DQ [20:19]	DQ [18:16]	DQ [15:0]
Reserved	0: Direct 1: Indirect	Successful SEARCH Register Index (Applicable if DQ[29] is indirect)	ID	00: Data Array	Reserved	If DQ[29] is '0,' this field carries address of data array location. If DQ[29] is '1,' the successful search register ID (SSRI) specified on DQ[28:26] supplies the address of the data array location: {SSR[15:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}(1)
Reserved	0: Direct 1: Indirect	Successful SEARCH Register Index (Applicable if DQ[29] is indirect)	ID	01: Mask Array	Reserved	If DQ[29] is '0,' this field carries address of mask array location. If DQ[29] is '1,' the successful search register ID (SSRI) specified on DQ[28:26] supplies the address of the mask array location: {SSR[15:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}(1)
Reserved	0: Direct 1: Indirect	Successful SEARCH Register Index (Applicable if DQ[29] is indirect)	ID	10: External SRAM	Reserved	If DQ[29] is '0,' this field carries address of SRAM location. If DQ[29] is '1,' the successful search register ID (SSRI) specified on DQ[28:26] supplies the address of the SRAM location: {SSR[15:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}(1)

Note: 1. "|" stands for Logical OR operation. "{ }" stands for concatenation operator.

Table 21. READ Address Format for Internal Registers

DQ[71:26]	DQ[25:21]	DQ[20:19]	DQ[18:7]	DQ[6:0]
Reserved	ID	11: Register	Reserved	Register Address

Table 22. READ Address Format for Data and Mask Arrays

DQ[71:26]	DQ[25:21]	DQ[20:19]	DQ[18:16]	DQ[15:0]
Reserved	ID	00: Data Array	Reserved	Do not care. These 16 bits come from the internal register (RBURADR) which increments for each access.
Reserved	ID	01: Mask Array	Reserved	Do not care. These 16 bits come from the internal register (RBURADR) which increments for each access.

WRITE COMMAND

The WRITE can be a single write of a data array, mask array, register, or external SRAM location (CMD[2] = 0). It can be a burst WRITE (CMD[2] = 1) using an internal auto-incrementing address register (WBURADR) of the data array or mask array locations. A single-location WRITE is a three-cycle operation, shown in Figure 20, page 36. The burst WRITE adds one extra cycle for each successive WRITE.

The WRITE operation sequence is as follows:

– **Cycle 1A:** The host ASIC applies the WRITE Instruction on the CMD[1:0] (CMD[2] = 0), using CMDV=1 and the address supplied on the DQ Bus, as shown in Table 23, page 37. The host ASIC also supplies the index to the global mask register to mask the write to the data array or mask array location in {CMD[10], CMD[5:3]}. For SRAM WRITEs, the host ASIC must supply the SADR[23:21] on CMD[8:6]. The host ASIC sets CMD[9] to '0' for the normal WRITE.

– **Cycle 1B:** The host ASIC continues to apply the WRITE Instruction to the CMD[1:0] (CMD[2] = 0), using CMDV = 1 and the address supplied on the DQ Bus. The host ASIC continues to supply the global mask register index to mask the WRITE to the data or mask array locations in {CMD[10], CMD[5:3]}. The host ASIC selects the device where ID[4:0] matches the DQ[25:21] lines, or it selects all the devices when DQ[25:21] = 11111.

– **Cycle 2:** The host ASIC drives the DQ[71:0] with the data to be written to the data array, mask array, external SRAM, or register location of the selected device.

– **Cycle 3:** Idle cycle. At the termination of this cycle, another operation can begin.

Note: The latency of the SRAM WRITE will be different than the one described above (see SRAM PIO Access, page 128).

The burst WRITE operation lasts for n + 2 CLK cycles (where n signifies the number of accesses in the burst as specified in the BLEN field of the WBURREG register, please see Figure 21, page 37).

This operation assumes that the host ASIC has programmed the WBURREG with the starting address (ADR) and the length of transfer (BLEN) before initiating the burst write command (see Table 25, page 38 for format). The sequence is as follows:

– **Cycle 1A:** The host ASIC applies the WRITE Instruction on the CMD[1:0] (CMD[2] = 1), using CMDV = 1 and the address supplied on the DQ Bus, as shown in Table 25, page 38. The host ASIC also supplies the index to the global mask register to mask the write to the data or mask array locations in {CMD[10], CMD[5:3]}. The host ASIC sets ASIC sets CMD[9] to '0' for the normal WRITE.

– **Cycle 1B:** The host ASIC continues to apply the WRITE Instruction on the CMD[1:0] (CMD[2] = 0), using CMDV = 1 and the address supplied on the DQ Bus. The host ASIC continues to supply the global mask register index to mask the WRITE to the data or mask array locations in {CMD[10], CMD[5:3]}. The host ASIC selects the device where ID[4:0] matches the DQ[25:21] lines, or it selects all the devices when DQ[25:21] = 11111.

– **Cycle 2:** The host ASIC drives the DQ[71:0] with the data to be written to the data array or mask array location of the selected device. The M7040N writes the data from the DQ[71:0] Bus only to the subfield that has the corresponding mask bit set to '1' in the global mask register specified by the index {CMD[10], CMD[5:3]} and supplied in Cycle 1.
– **Cycles 3 to n + 1:** The host ASIC drives the DQ[71:0] with the data to be written to the next data array or mask array location (addressed by the auto-increment ADR field of the WBURREG register) of the selected device. The M7040N writes the data on the DQ[71:0] Bus only to the subfield that has the corresponding mask bit set to '1' in the global mask register specified by the index {CMD[10], CMD[5:3]} and supplied in Cycle 1. The M7040N drives the EOT signal low from Cycle 3 to Cycle n; the M7040N drives the EOT signal high in Cycle n + 1 (n is specified in the BLEN field of the WBURREG).
– **Cycle n + 2:** The M7040N drives the EOT signal low. At the termination of the Cycle n + 2, the M7040N floats the EOT signal to a 3-state, and a new instruction can begin.

Figure 20. Single Location WRITE Cycle Timing

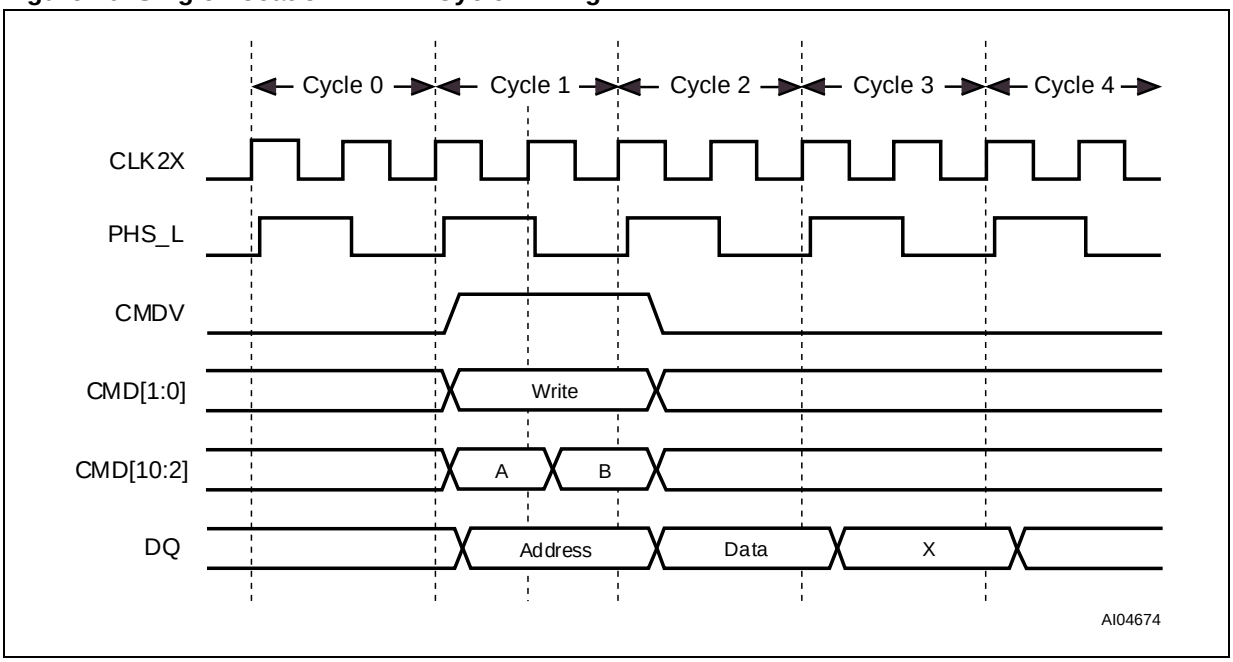


Figure 21. Burst WRITE of the Data and Mask Arrays (BLEN = 4)

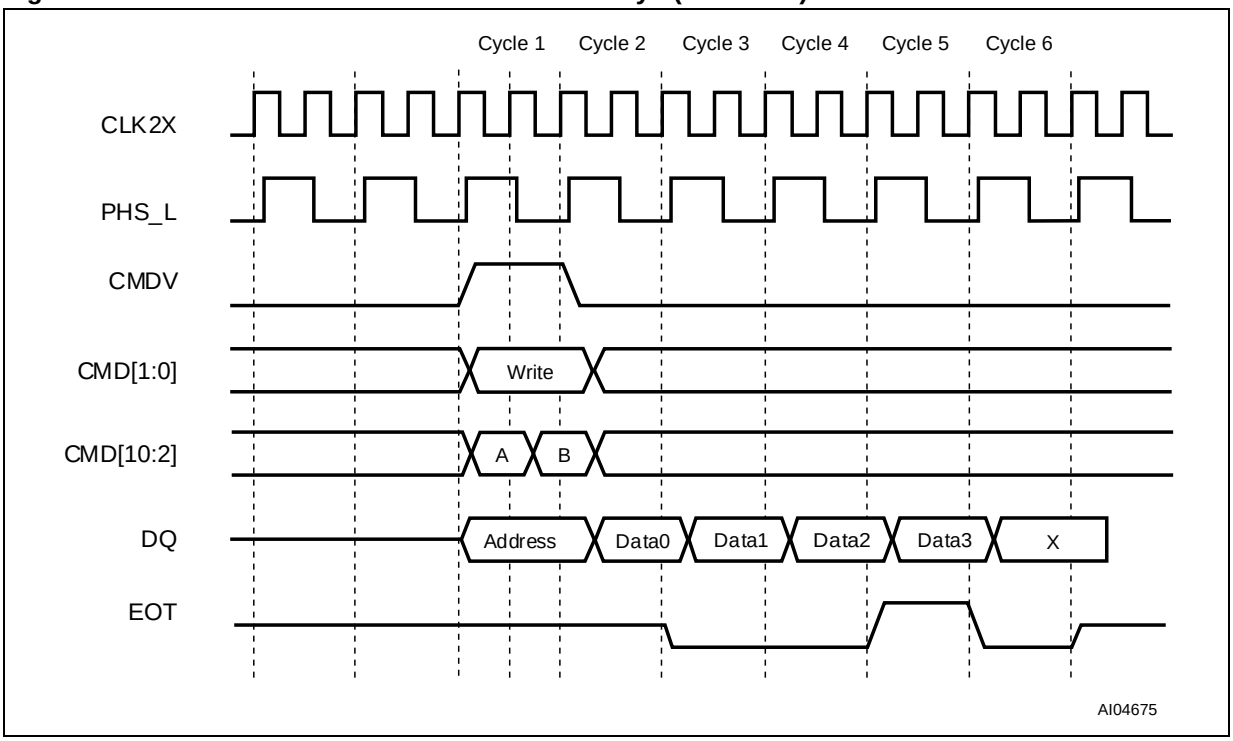


Table 23. (Single) WRITE Address Format for Data and Mask Arrays or SRAM

DQ [71:30]	DQ [29]	DQ [28:26]	DQ [25:21]	DQ [20:19]	DQ [18:16]	DQ [15:0]
Reserved	0: Direct 1: Indirect	Successful SEARCH Register Index (Applicable if DQ[29] is indirect)	ID	00: Data Array	Reserved	If DQ[29] is '0,' this field carries the address of the data array location. If DQ[29] is '1,' the successful search register specified by DQ[28:26] supplies the address of the data array location: {SSR[15:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}(1)
Reserved	0: Direct 1: Indirect	Successful SEARCH Register Index (Applicable if DQ[29] is indirect)	ID	01: Mask Array	Reserved	If DQ[29] is '0,' this field carries address of the mask array location. If DQ[29] is '1,' the successful search register specified by DQ[28:26] supplies the address of the mask array location: {SSR[15:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}(1)
Reserved	0: Direct 1: Indirect	Successful SEARCH Register Index (Applicable if DQ[29] is indirect)	ID	10: External SRAM	Reserved	If DQ[29] is '0,' this field carries address of the data SRAM location. If DQ[29] is '1,' the successful search register specified by DQ[28:26] supplies the address of the SRAM location: {SSR[15:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}(1)

Note: 1. "|" stands for Logical OR operation. "{ }" stands for concatenation operator.

Table 24. WRITE Address Format for Internal Registers

DQ[71:26]	DQ[25:21]	DQ[20:19]	DQ[18:7]	DQ[6:0]
Reserved	ID	11: Register	Reserved	Register address

Table 25. WRITE Address Format for Data and Mask Array (Burst Write)

DQ [71:26]	DQ [25:21]	DQ [20:19]	DQ [18:16]	DQ [15:0]
Reserved	ID	00: Data array	Reserved	Don't care. These 16 bits come from the internal register (WBURADR), which increments with each access.
Reserved	ID	01: Mask array	Reserved	Don't care. These 16 bits come from the internal register (WBURADR), which increments with each access.

Parallel WRITE

In order to write the data and mask arrays faster for initialization, testing, or diagnostics, many locations can be written simultaneously in the M7040N device. When CMD[9] is set in Cycles A and B of the WRITE command during a WRITE to the data or mask arrays, the address present on DQ[10:1] that specifies 64 locations in a device is used and 64 72-bit locations are simultaneously written in either the data or mask array.

SEARCH COMMAND

The M7040N (Silicon) Search Engine can be configured in four ways:

1. 72-bit
2. 144-bit (page)
3. 288-bit (page)
4. Mixed-sizes on tables configured with different widths using an M7040N with CFG_L low or CFG_L high (page)

72-bit Configuration with Single Device

The hardware diagram of the search subsystem of a single device is shown in Figure 22. Figure 23, page 40 shows the timing diagram for a SEARCH operation in the 72-bit configuration (CFG = 0000000000000000) for one set of parameters. This illustration assumes that the host ASIC has programmed TLSZ to '00,' HLAT to '000,' LRAM to '1,' and LDEV to '1' in the command register.

The following is the sequence of operations for a single 72-bit SEARCH command.

– **Cycle A:** The host ASIC drives CMDV high and applies the SEARCH command code ('10') on CMD[1:0] signals. {CMD[10], CMD[5:3] must be driven with the index to the global mask register pair for use in the SEARCH operation. CMD[8:6] signals must be driven with the same bits that will be driven on SADR[23:21] by this device if it has a hit. DQ[71:0] must be driven with the 72-bit data to be compared. The CMD[2] signal must be driven to Logic '0.'

– **Cycle B:** The host ASIC continues to drive CMDV high and applies the SEARCH command ('10') on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 144-bit word presented on the DQ Bus during Cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 24). The DQ[71:0] continues to carry the 72-bit data to be compared.

  Note: In the 72-bit configuration, the host ASIC must supply the same data on DQ[71:0] during both Cycles A and B. The even and odd pair of GMRs selected for the comparison must be programmed with the same value.

The logical 72-bit SEARCH operation is shown in Figure 24, page 41. The entire table consisting of 72-bit entries is compared to a 72-bit word K (presented on the DQ Bus in both Cycles A and B of the command) using the GMR and the local mask bits. The effective GMR is the 72-bit word specified by the identical value in both even and odd GMR pairs selected by the GMR Index in the command's Cycle A. The 72-bit word K (presented on the DQ Bus in both Cycles A and B of the command) is also stored in both even and odd comparand register pairs selected by the Comparand Register Index in the command's Cycle B. In a x72 configuration, only the even comparand register can be subsequently used by the LEARN command. The word K (presented on the DQ Bus in both Cycles A and B of the command) is compared with each entry in the table starting at location "0."

The first matching entry's location address, "L," is the winning address that is driven as part of the SRAM address on the SADR[23:0] lines (see SRAM ADDRESSING, page 128).

The SEARCH command is a pipelined operation and executes a SEARCH at half the rate of the frequency of CLK2X for 72-bit searches in x72-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 72-bit SEARCH command cycle (two CLK2X cycles) is shown in Table 26, page 41.

The latency of a SEARCH from command to SRAM access cycle is 4 for a single device in the table and TLSZ = 00. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in Table 27, page 41.

Figure 22. Hardware Diagram for a Table with One Device

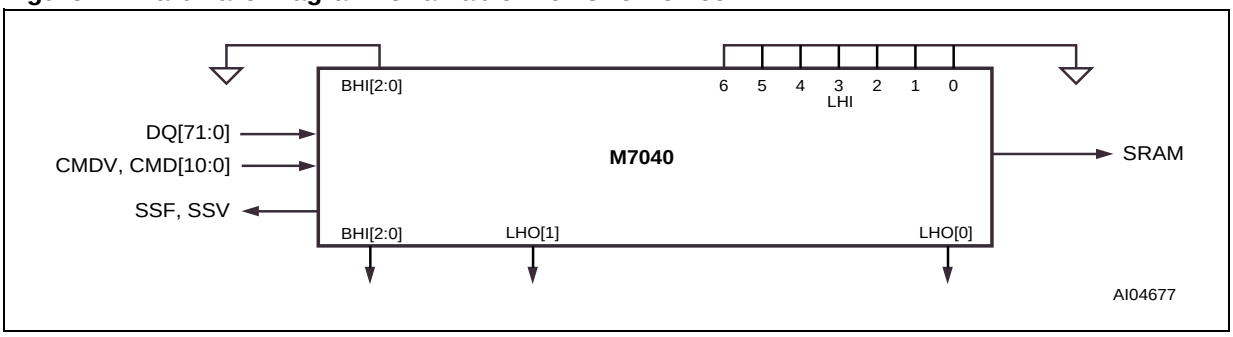


Figure 23. 72-Bit Configuration SEARCH Timing Diagram for One Device

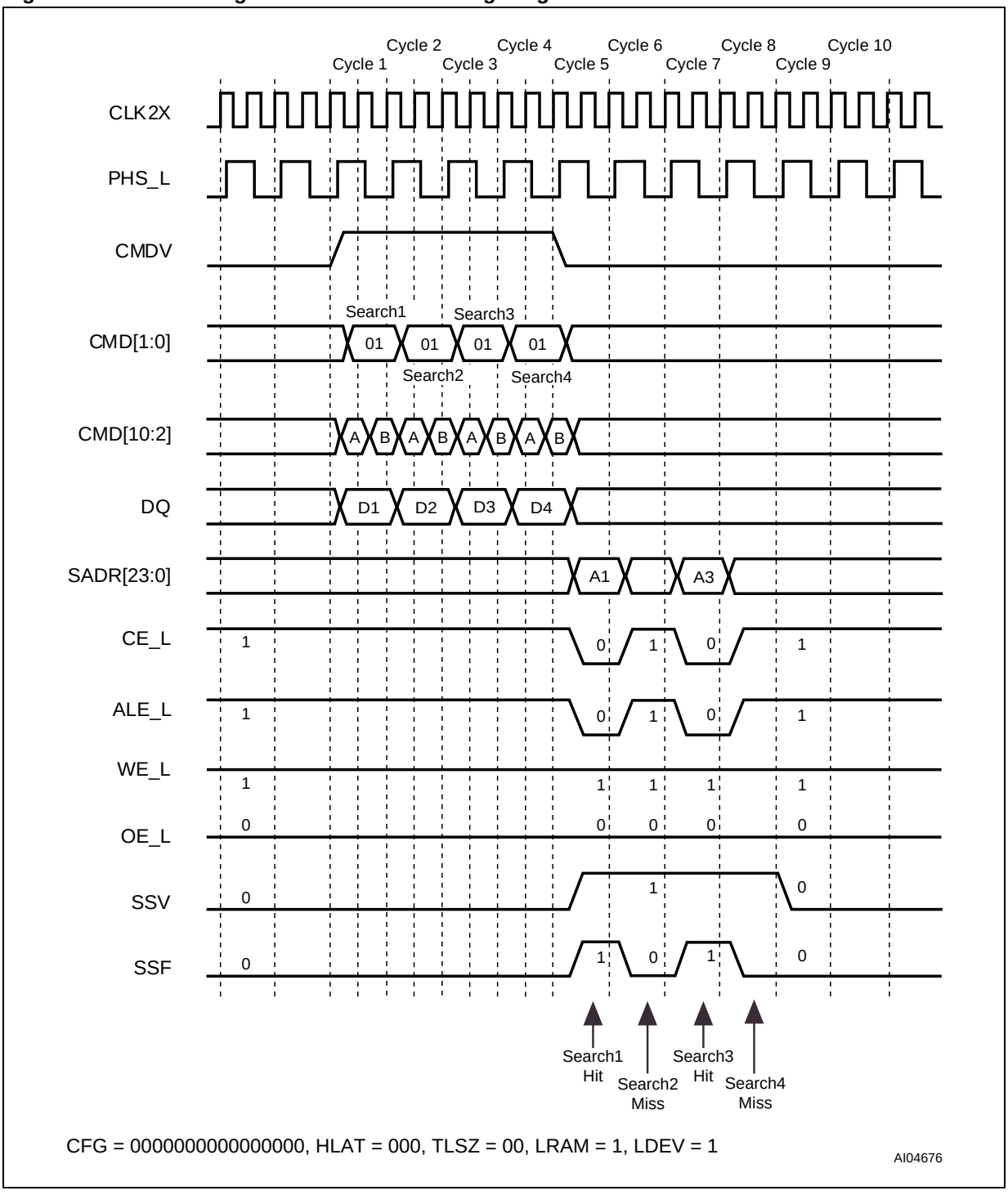


Figure 24. x72 Table with One Device

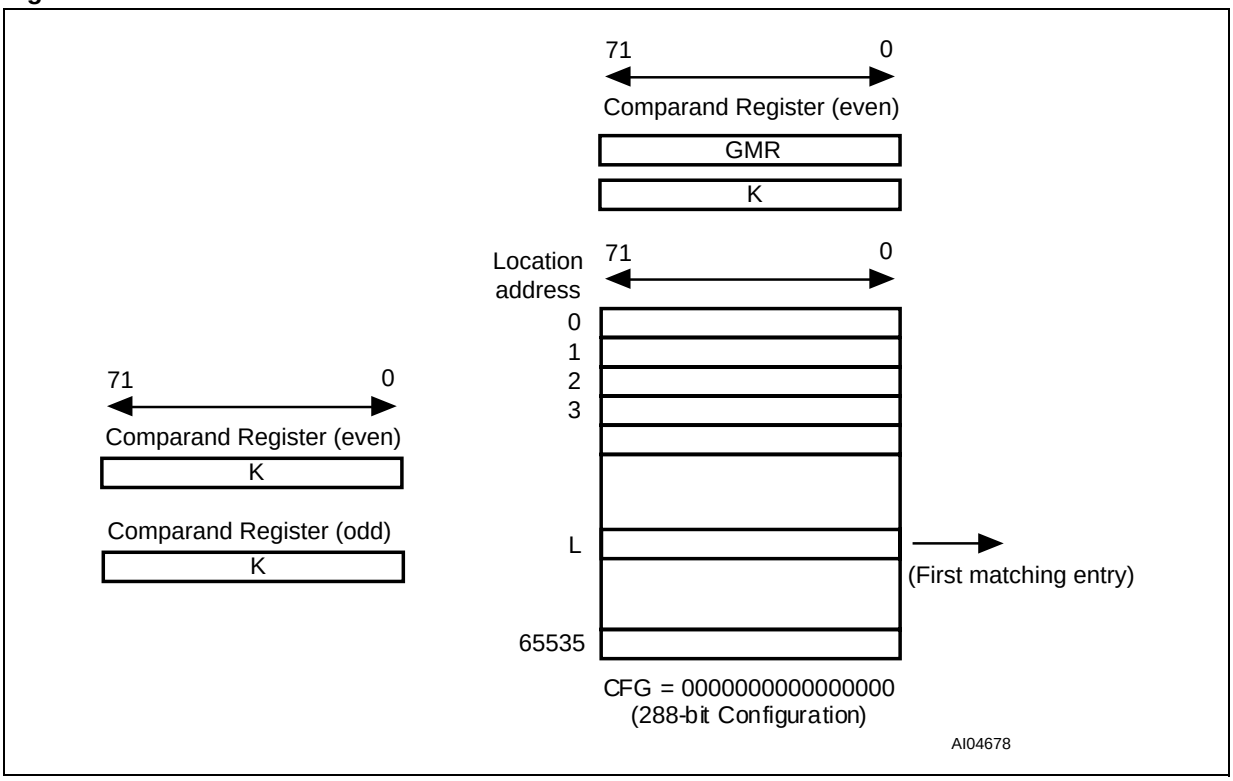


Table 26. Latency of SEARCH from Instruction to SRAM Access Cycle, 72-bit

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	64K x 72-bit	4
2–8 (TLSZ = 01)	512K x 72-bit	5
2–31 (TLSZ = 10)	1984K x 72-bit	6

Table 27. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

72-bit SEARCH on Tables Configured as x72 Using up to Eight M7040N Devices

The hardware diagram of the search subsystem of eight devices is shown in Figure 25, page 43. The following are the parameters programmed into the eight devices:

– First seven devices (device 0–6):
CFG = 0000000000000000, TLSZ = 01,
HLAT = 010, LRAM = 0, and LDEV = 0.

– Eighth device (device 7):
CFG = 0000000000000000, TLSZ = 01,
HLAT = 010, LRAM = 1, and LDEV = 1.

Note: All eight devices must be programmed with the same values for TLSZ and HLAT. Only the last device in the table (Device 7 in this case) must be programmed with LRAM = 1 and LDEV = 1. All other upstream devices (Devices 0 through 6 in this case) must be programmed with LRAM = 0 and LDEV = 0.

Figure 27, page 45 shows the timing diagram for a SEARCH command in the 72-bit-configured table of eight devices for Device 0. Figure 28, page 46 shows the timing diagram for a SEARCH command in the 72-bit-configured table of eight devices for Device 1. Figure 29, page 47 shows the timing diagram for a SEARCH command in the 72-bit-configured table of eight devices for Device 7 (the last device in this specific table). For these timing diagrams four 72-bit searches are performed sequentially. HIT/MISS assumptions were made as shown below in Table 28.

The sequence of operation for a 72-bit SEARCH command is as follows:]

– **Cycle A:** The host ASIC drives CMDV high and applies the SEARCH command code ('10') on CMD[1:0] signals. {CMD[10], CMD[5:3] must be driven with the index to the global mask register pair for use in the SEARCH operation. CMD[8:6] signals must be driven with the same bits that will be driven on SADR[23:21] by this device if it has a hit. DQ[71:0] must be driven with the 72-bit data to be compared. The CMD[2] signal must be driven to Logic '0.'

– **Cycle B:** The host ASIC continues to drive CMDV high and applies the SEARCH command ('10') on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 144-bit word presented on the DQ Bus during Cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 24). The DQ[71:0] continues to carry the 72-bit data to be compared.

Note: For 72-bit searches, the host ASIC must supply the same data on DQ[71:0] during both Cycles A and B. The even and odd pair of GMRs selected for the comparison must be programmed with the same value.

The logical 72-bit SEARCH operation is shown in Figure 26, page 44. The entire table with eight devices of 72-bit entries is compared to a 72-bit word K (presented on the DQ Bus in both Cycles A and B of the command) using the GMR and the local mask bits. The effective GMR is the 72-bit word specified by the identical value in both even and odd GMR pairs in each of the eight devices and selected by the GMR Index in the command's Cycle A. The 72-bit word K (presented on the DQ Bus in both Cycles A and B of the command) is also stored in both even and odd comparand register pairs (selected by the Comparand Register Index in command Cycle B) in each of the eight devices. In the x72 configuration, only the even comparand register can subsequently be used by the LEARN command in one of the devices (only the first non-full device). The word K (presented on the DQ Bus in both Cycles A and B of the command) is compared with each entry in the table starting at location "0." The first matching entry's location address, "L," is the winning address that is driven as part of the SRAM address on the SADR[23:0] lines (see SRAM ADDRESSING, page 128). The global winning device will drive the bus in a specific cycle. On a global miss cycle the device with LRAM = 1 (default driving device for the SRAM Bus) and LDEV = 1 (default driving device for SSF and SSV signals) will be the default driver for such missed cycles.

The SEARCH command is a pipelined operation and executes a search at half the rate of the frequency of CLK2X for 72-bit searches in x72-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 72-bit SEARCH command cycle (two CLK2X cycles) is shown in Table 29, page 48

The latency of the search from command to SRAM access cycle is 5 for up to eight devices in the table (TLSZ = 01). SSV and SSF also shift further to the right for different values of HLAT, as specified in Table 30, page 48.

Table 28. Hit/Miss Assumption

Search Number	1	2	3	4
Device 0	Hit	Miss	Hit	Hit
Device 1	Miss	Hit	Hit	Miss
Device 2-6	Miss	Miss	Miss	Miss
Device 7	Miss	Miss	Hit	Hit

Figure 25. Hardware Diagram for a Table with Eight Devices

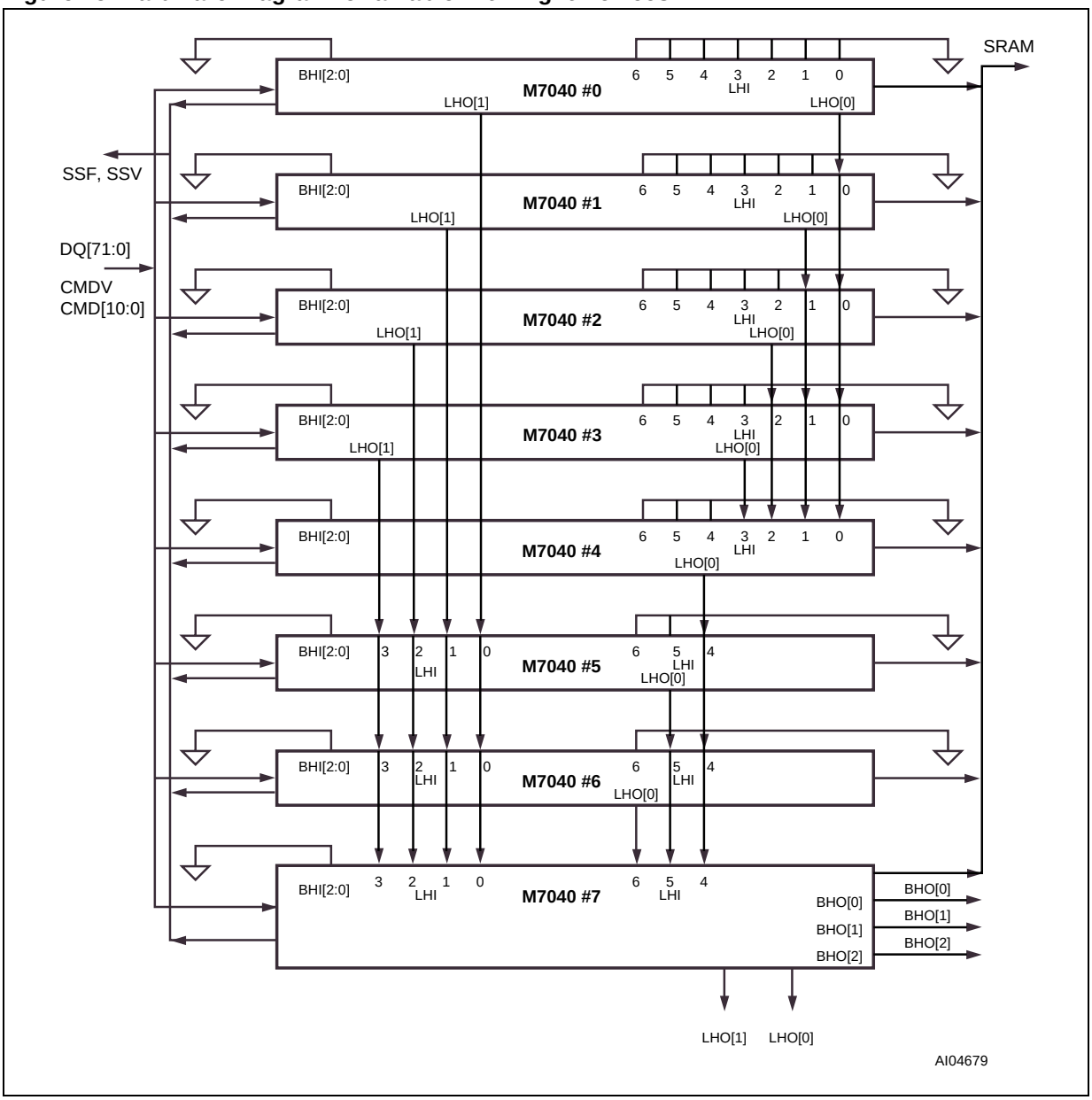
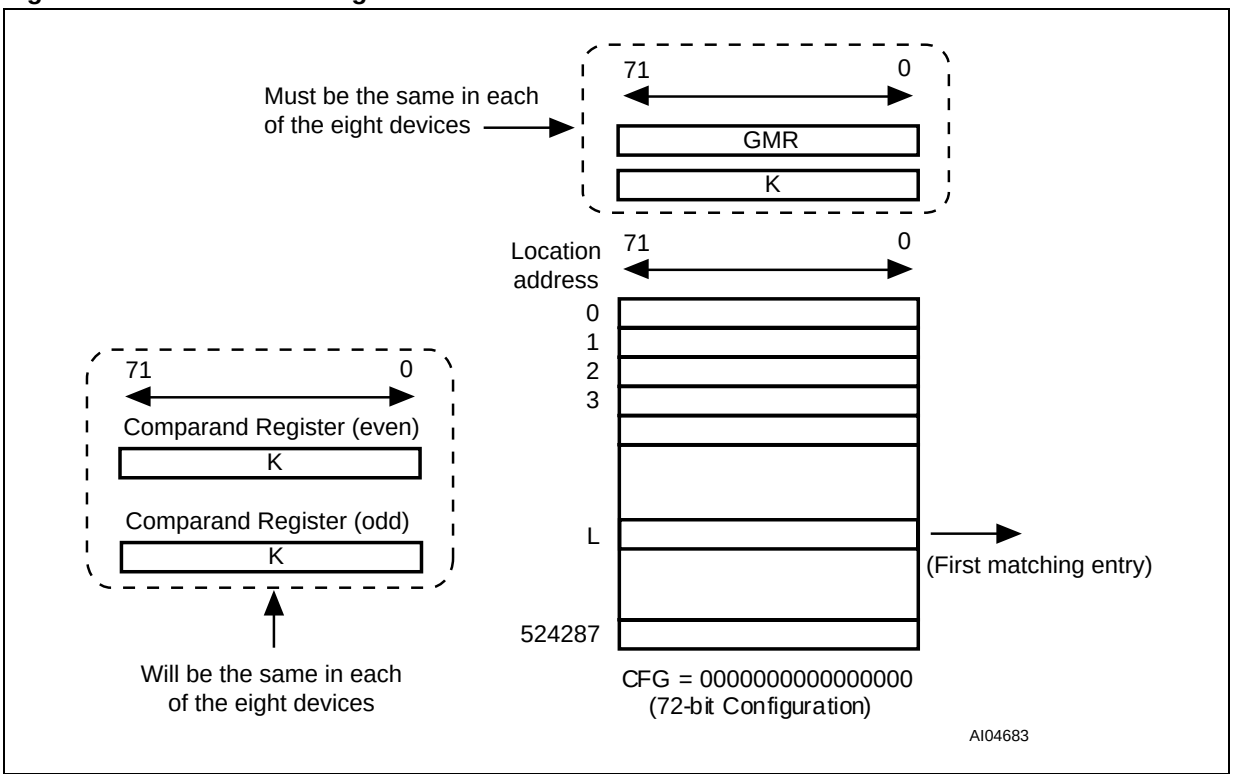
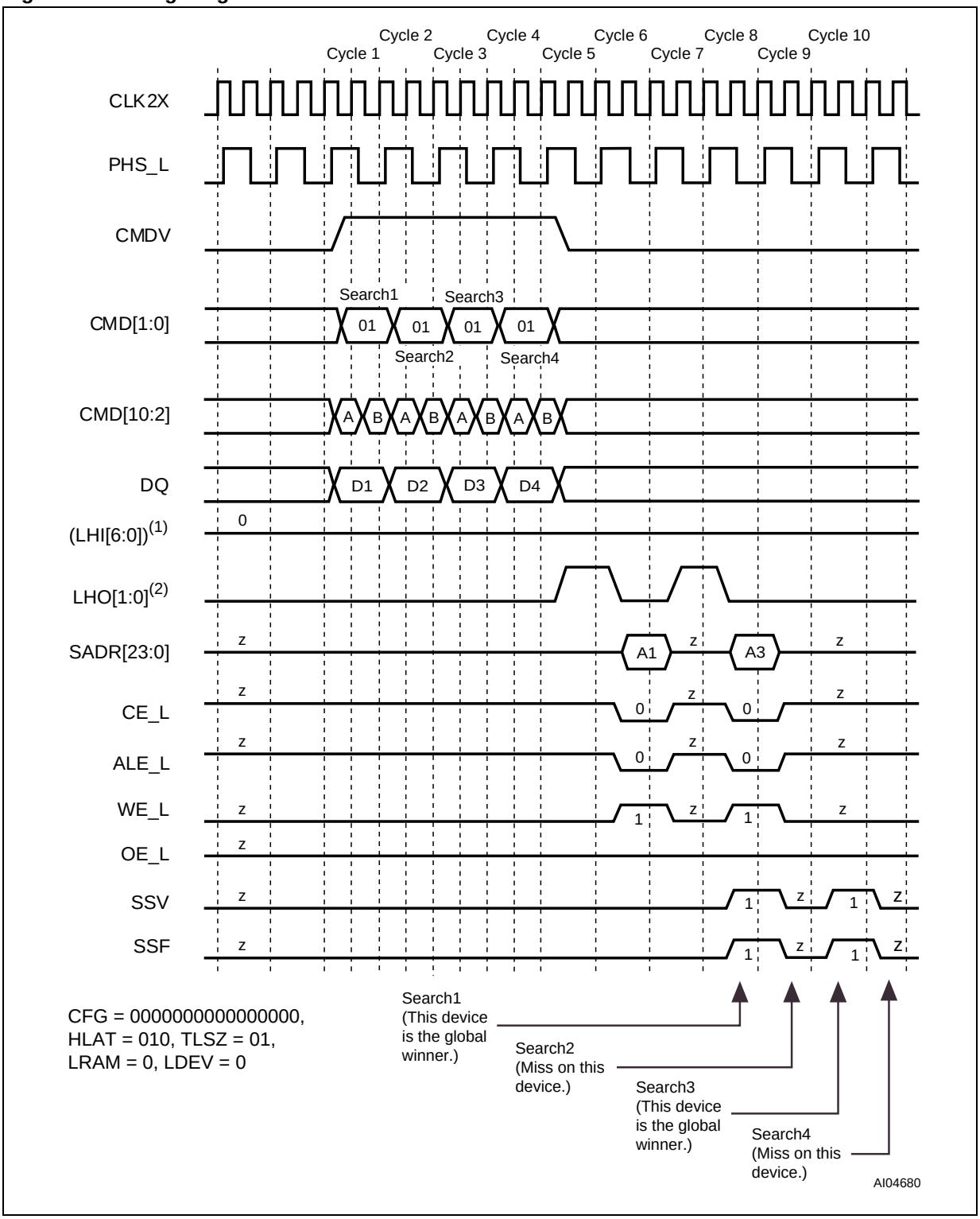


Figure 26. x72 Table with Eight Devices



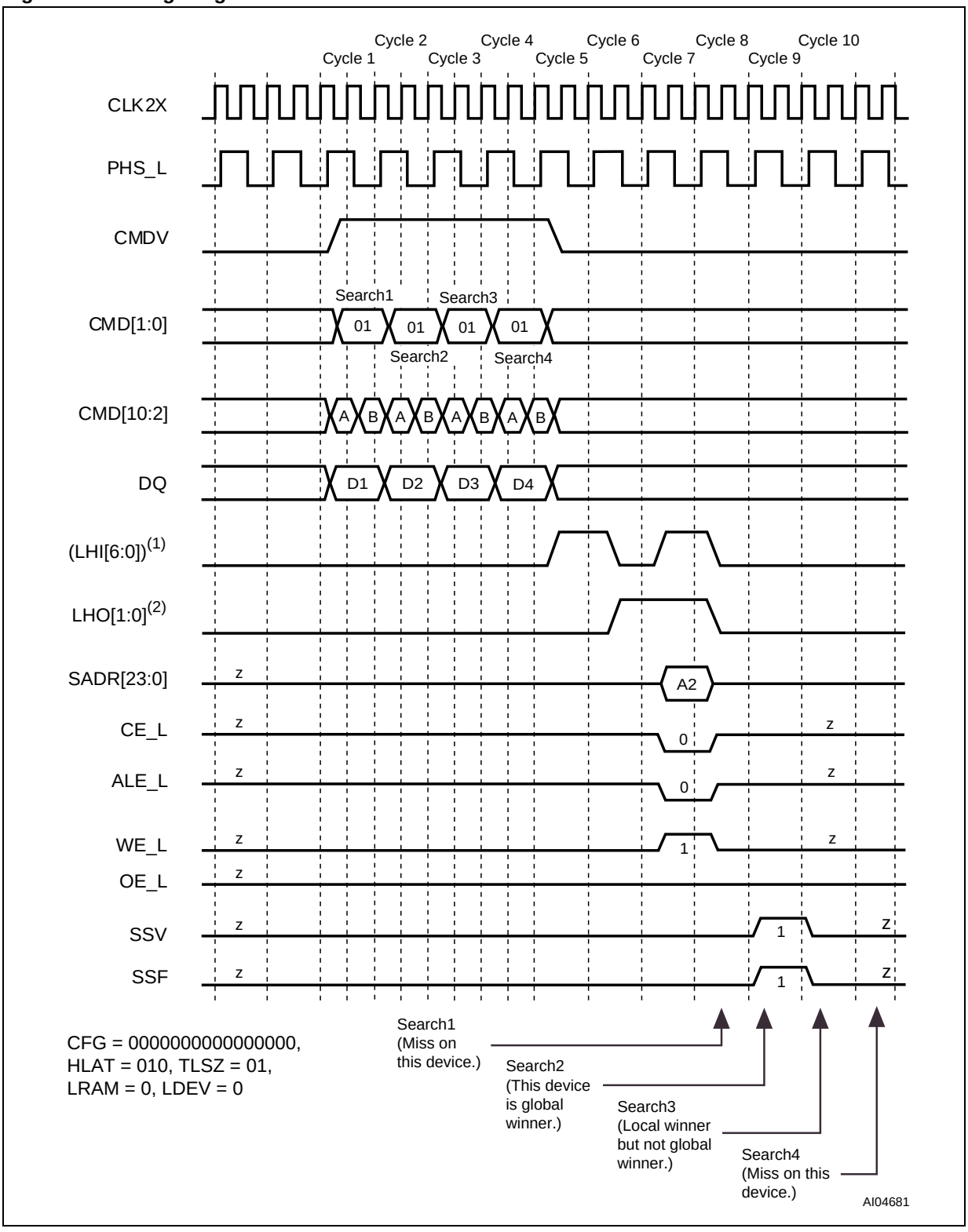
Timing Diagrams for x72 Using up to Eight M7040N Devices

Figure 27. Timing Diagram for 72-bit SEARCH For Device 0



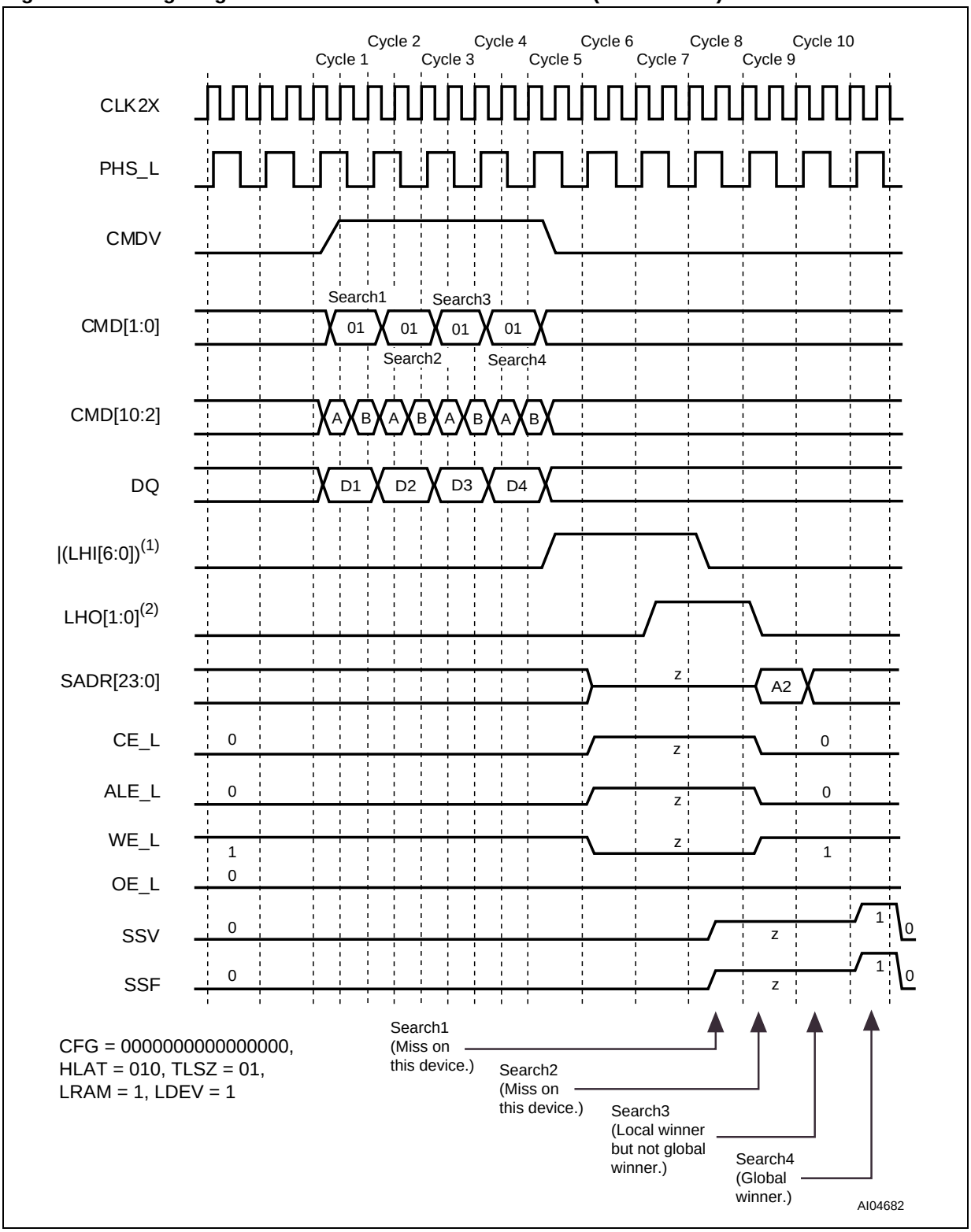
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.

Figure 28. Timing Diagram for 72-bit SEARCH For Device 1



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.

Figure 29. Timing Diagram for 72-bit SEARCH For Device 7 (Last Device)



Note: 1. |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.

Table 29. Latency of SEARCH from Instruction to SRAM Access Cycle

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	64K x 72-bit	4
1–8 (TLSZ = 01)	512K x 72-bit	5
1–31 (TLSZ = 10)	1984K x 72-bit	6

Table 30. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

72-bit Search on Tables Configured as x72 Using Up To 31 M7040N Devices

The hardware diagram of the search subsystem of 31 devices is shown in Figure 30, page 50. Each of the four blocks in the diagram represents eight M7040N devices (except the last, which has seven devices). The diagram for a block of eight devices is shown in Figure 31, page 51. The following are the parameters programmed into the 31 devices:

– First thirty devices (devices 0–29):
CFG = 0000000000000000, TLSZ = 10,
HLAT = 001, LRAM = 0, and LDEV = 0.

– Thirty-first device (device 30):
CFG = 0000000000000000, TLSZ = 10,
HLAT = 001, LRAM = 1, and LDEV = 1.

Note: All 31 devices must be programmed with the same values for TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (Device 30 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (Devices 0 through 29 in this case).

The timing diagrams referred to in this paragraph reference the HIT/MISS assumptions defined in Table 31, page 49. For the purpose of illustrating the timings, it is further assumed that there is only one device with a matching entry in each of the blocks. Figure 33, page 53 shows the timing diagram for a SEARCH command in the 72-bit-configured table of 31 devices for each of the eight devices in Block Number 0. Figure 34, page 54 shows a timing diagram for a SEARCH command in the 72-bit-configured table of 31 devices for the all the devices in Block Number 1 (above the winning device in that block). Figure 35, page 55 shows the timing diagram for the globally winning device (defined as the final winner within its own and all blocks) in Block Number 1. Figure 36, page 56 shows the timing diagram for all the devices below the globally winning device in Block Number 1. Figure 37, page 57, Figure 38, page 58, and Figure 39, page 59 show the timing diagrams of the devices above the globally winning device, the globally winning device, and the devices below the globally winning device, respectively, for Block Number 2. Figure 40, page 60, Figure 41, page 61, Figure 42, page 62, and Figure 43, page 63 show the timing diagrams of the devices above globally winning device, the globally winning device, and the devices below the globally winning device except the last device (Device 30), respectively, for Block Number 3.

The following is the sequence of operation for a single 72-bit SEARCH command (also refer to Command Codes, page 30).

– **Cycle A:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair for use in this SEARCH operation. CMD[8:6] signals must be driven with the same bits that will be driven on SADR[23:21] by this device if it has a hit. DQ[71:0] must be driven with the 72-bit data to be compared. The CMD[2] signal must be driven to a logic '0.'

– **Cycle B:** The host ASIC continues to drive the CMDV high and applies SEARCH command ('10') on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 144-bit word presented on the DQ Bus during Cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 24). The DQ[71:0] continues to carry the 72-bit data to be compared.

  Note: For 72-bit searches, the host ASIC must supply the same 72-bit data on DQ[71:0] during both Cycles A and B. The even and odd pair of GMRs selected for the comparison must be programmed with the same value.

The logical 72-bit SEARCH operation is shown in Figure 32, page 52. The entire table (31 devices of 72-bit entries) is compared to a 72-bit word K (presented on the DQ Bus in both Cycles A and B of the command) using the GMR and the local mask bits. The effective GMR is the 72-bit word specified by the identical value in both even and odd GMR pairs in each of the eight devices and selected by the GMR Index in the command's Cycle A. The 72-bit word K (presented on the DQ Bus in both Cycles A and B of the command) is also stored in both even and odd comparand register pairs in each of the eight devices and selected by the Comparand Register Index in command's Cycle B. In the x72 configuration, the even comparand register can be subsequently used by the LEARN command only in the first non-full device. The word K (presented on the DQ Bus in both Cycles A and B of the command) is compared with each entry in the table starting at location "0." The first matching entry's location address, "L," is the winning address that is driven as part of the SRAM address on the SADR[23:0] lines (see SRAM ADDRESSING, page 128). The global winning device will drive the bus in a specific cycle. On global miss cycles the device with LRAM = 1 and LDEV = 1 will be the default driver for such missed cycles.

The SEARCH command is a pipelined operation and executes a search at half the rate of the frequency of CLK2X for 72-bit searches in x72-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 72-bit SEARCH command cycle (two CLK2X cycles) is shown in Table 32, page 64.

For up to 31 devices in the table (TLSZ = 10), search latency from command to SRAM access cycle is 6. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in Table 33, page 64.

The 72-bit SEARCH operation is pipelined and executes as follows:

– Four cycles from the SEARCH command, each of the devices knows the outcome internal to it for that operation;

– In the fifth cycle after the SEARCH command, the devices in a block arbitrate for a winner amongst them (a "block" being defined as less than or equal to eight devices resolving the winner within them using the LHI[6:0] and LHO[1:0] signalling mechanism);

– In the sixth cycle after the SEARCH command, the blocks (of devices) resolve the winning block through the BHI[2:0] and BHO[2:0] signalling mechanism. The winning device within the winning block is the global winning device for a SEARCH operation.

Table 31. Hit/Miss Assumption

Search Number	1	2	3	4
Block 0	Miss	Miss	Miss	Miss
Block 1	Miss	Miss	Hit	Miss
Block 2	Miss	Hit	Hit	Miss
Block 3	Hit	Hit	Miss	Miss

Figure 30. Hardware Diagram for a Table with 31 Devices

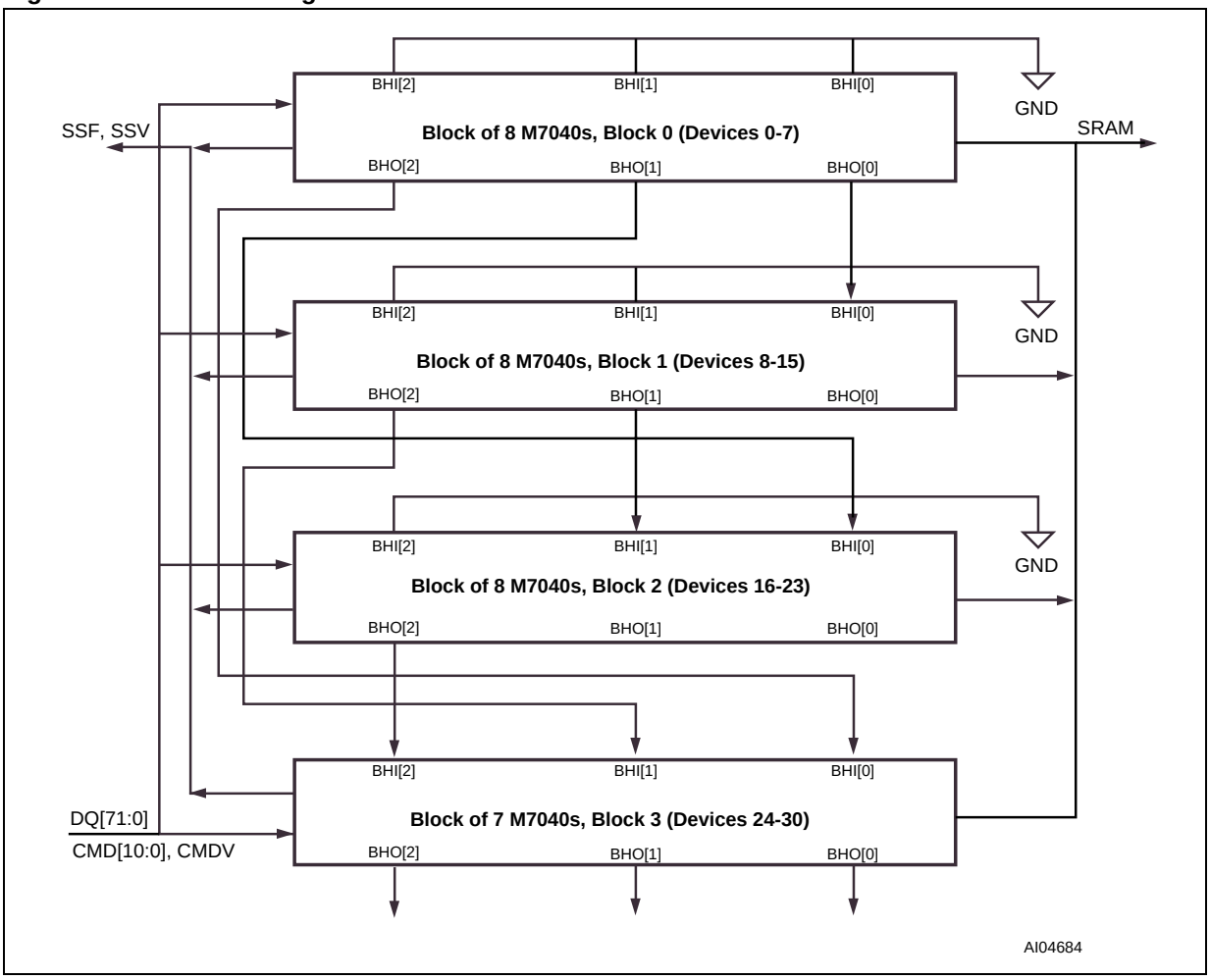


Figure 31. Hardware Diagram for a Block of Up To Eight Devices

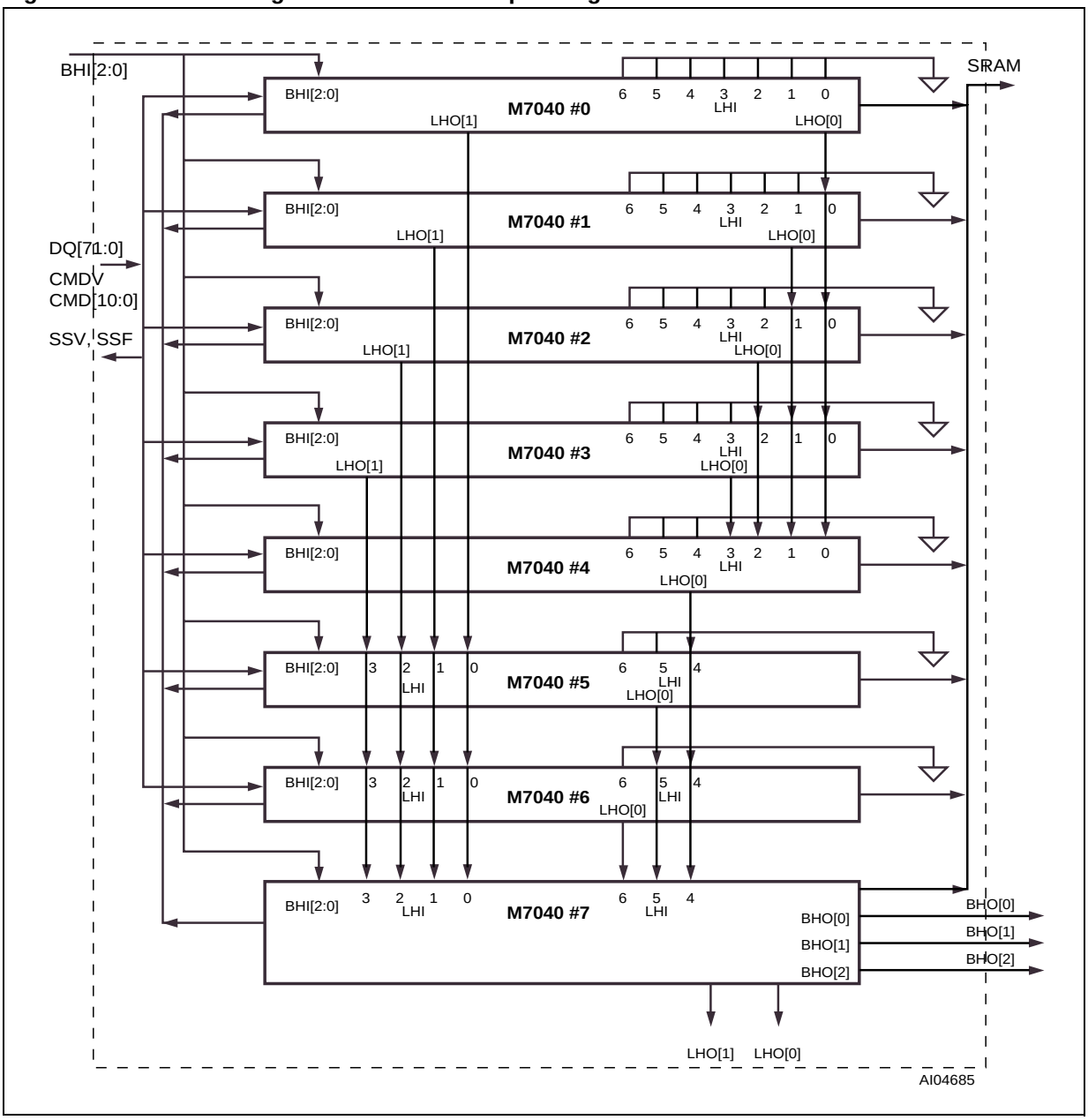
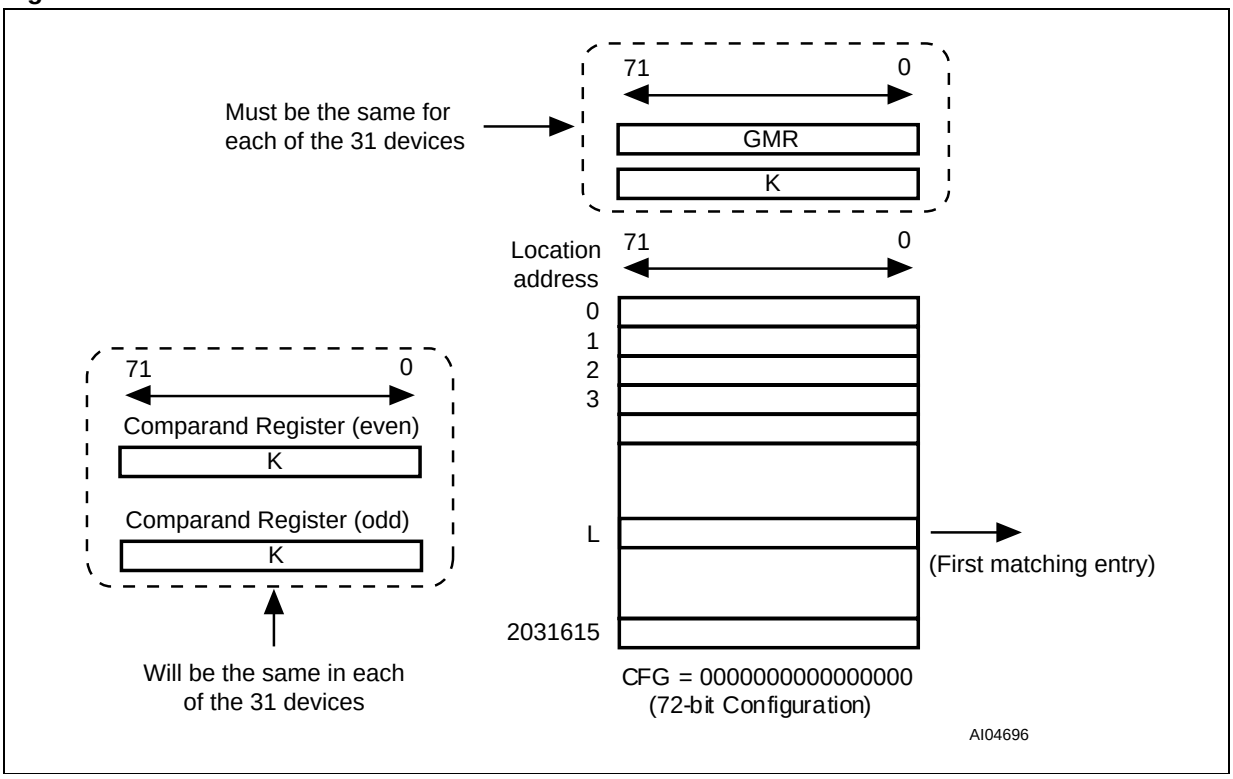
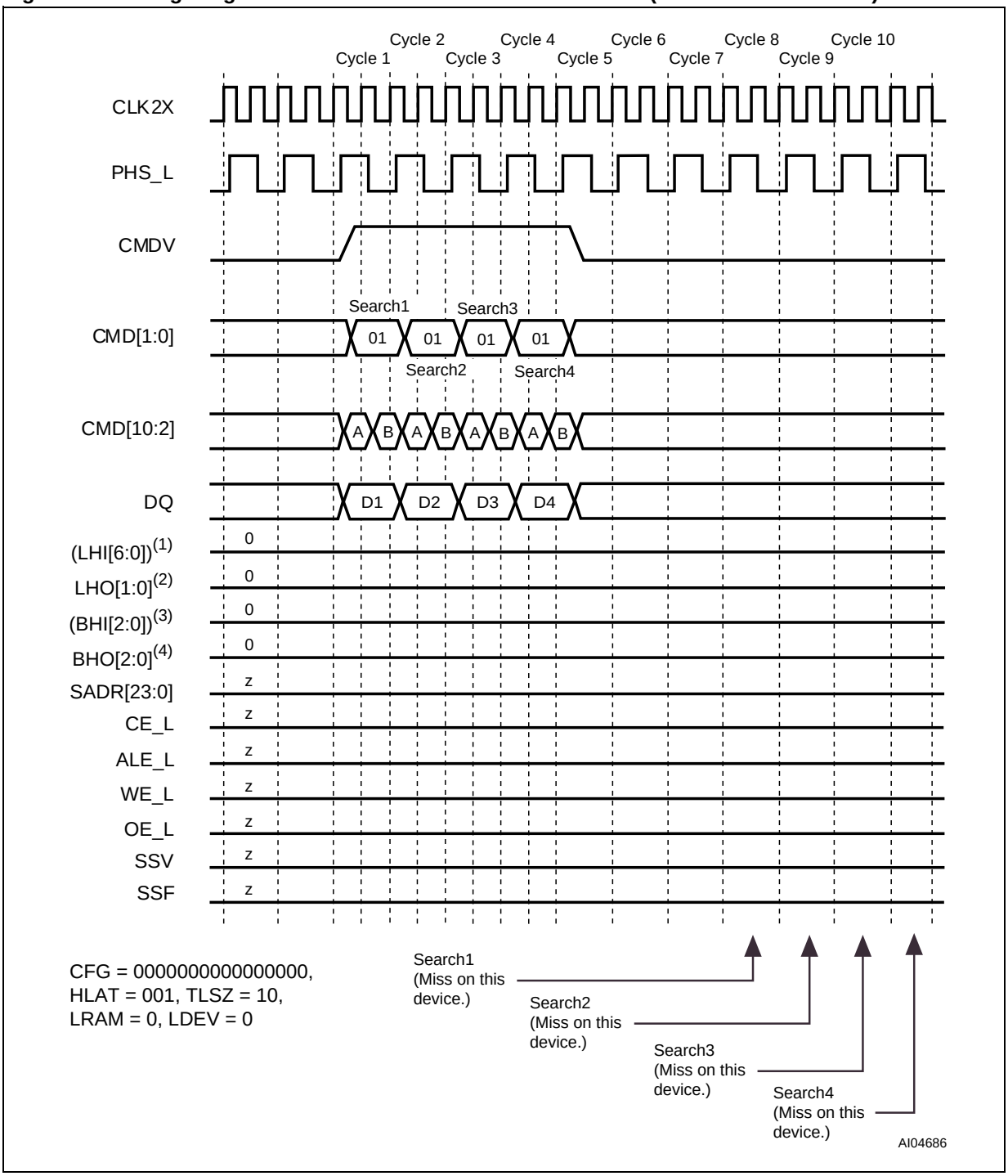


Figure 32. x72 Table with 31 Devices



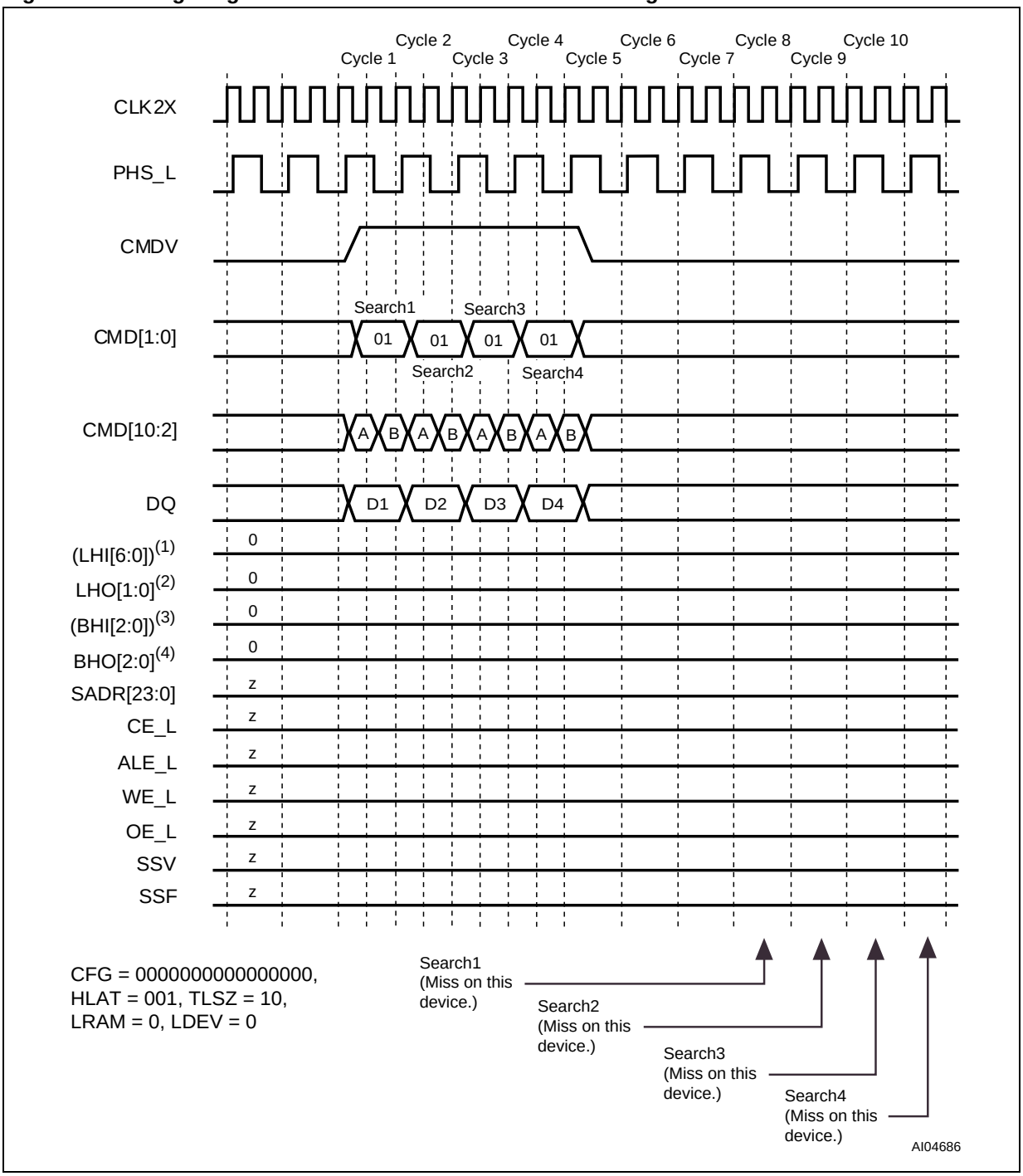
Timing Diagrams for x72 Using Up To 31 M7040N Devices

Figure 33. Timing Diagram for Each Device in Block Number 0 (Miss on Each Device)



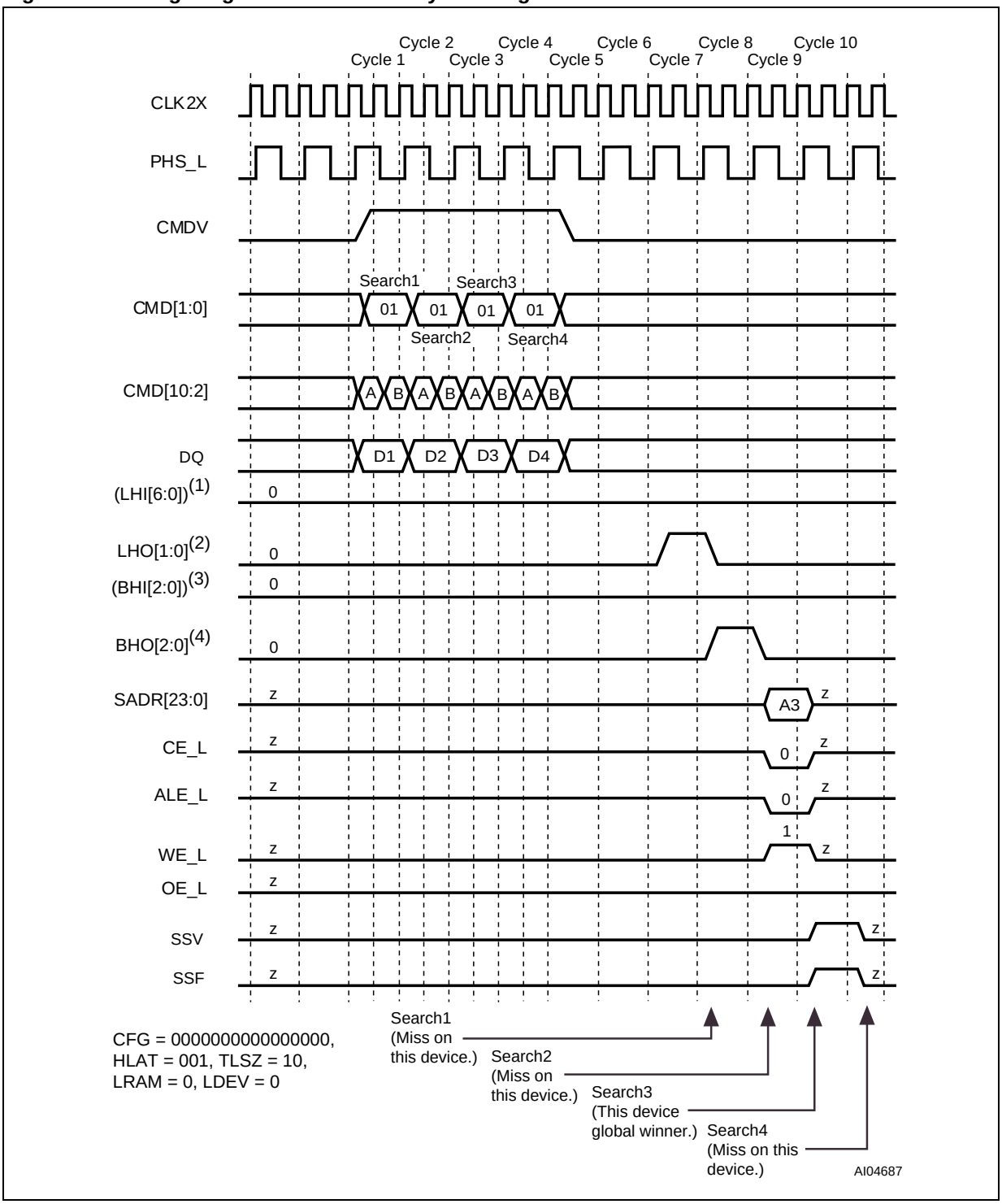
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 34. Timing Diagram for Each Device Above the Winning Device in Block Number 1



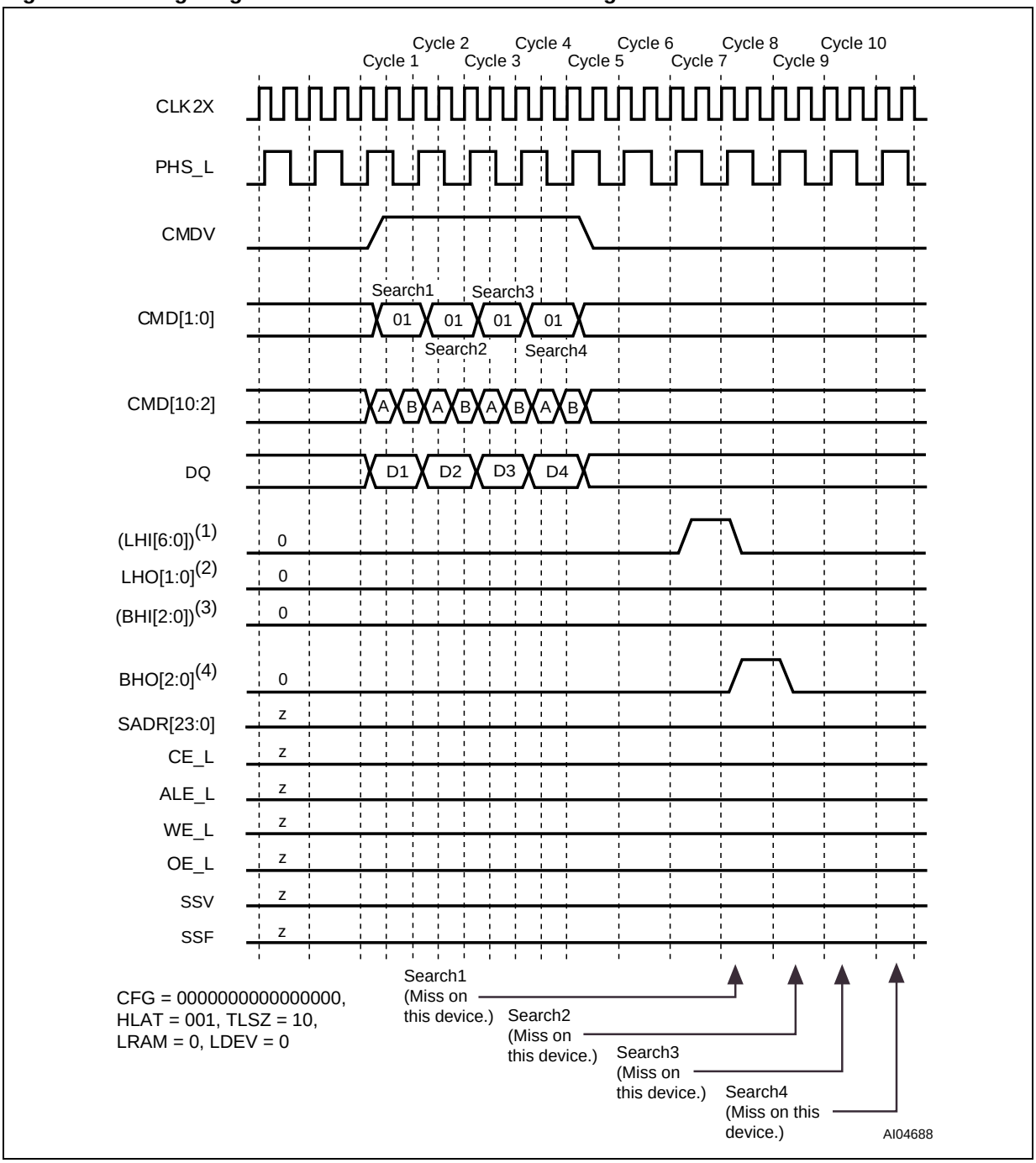
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 35. Timing Diagram for the Globally Winning Device in Block Number 1



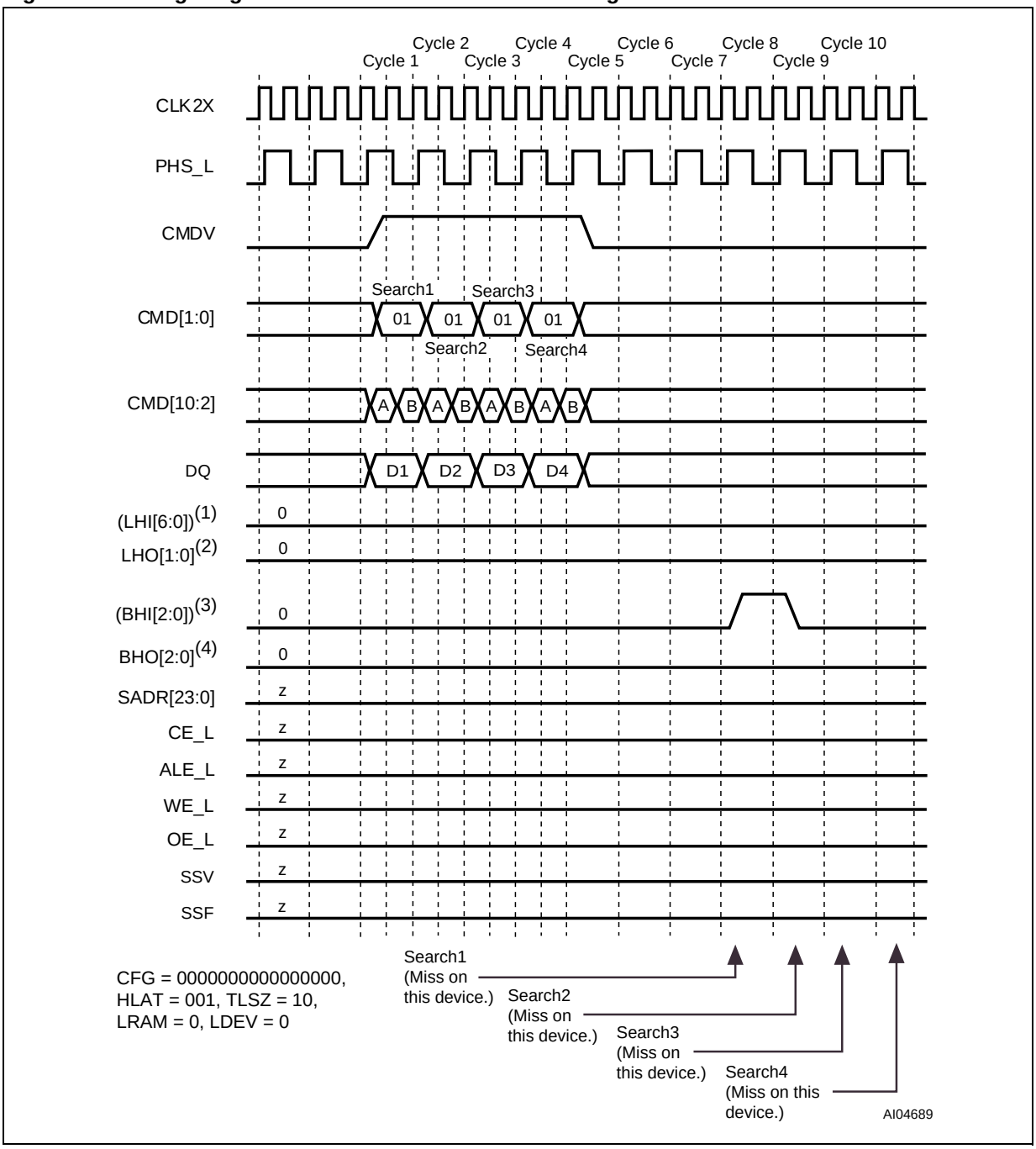
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 36. Timing Diagram for Devices Below the Winning Device in Block Number 1



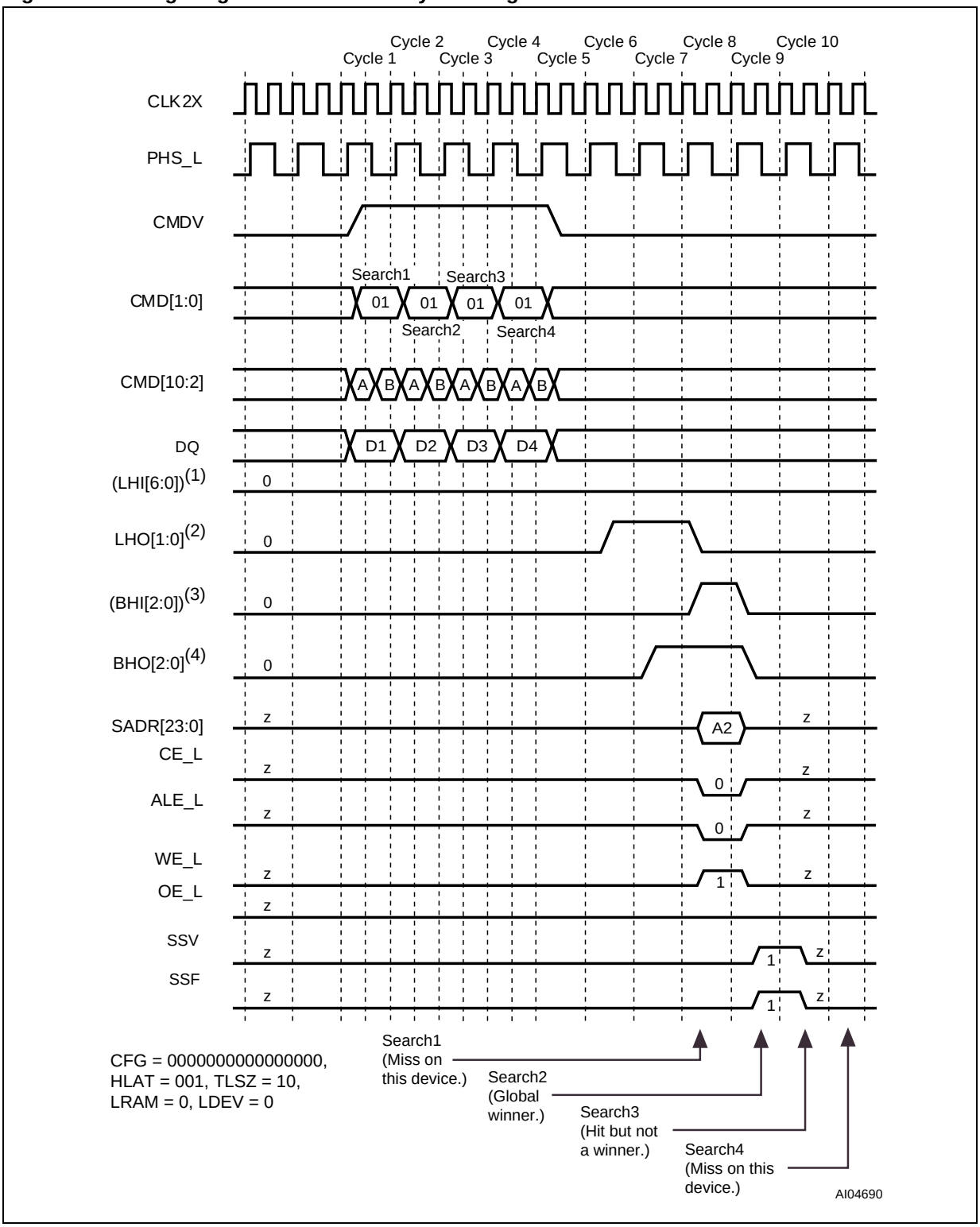
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 37. Timing Diagram for Devices Above the Winning Device in Block Number 2



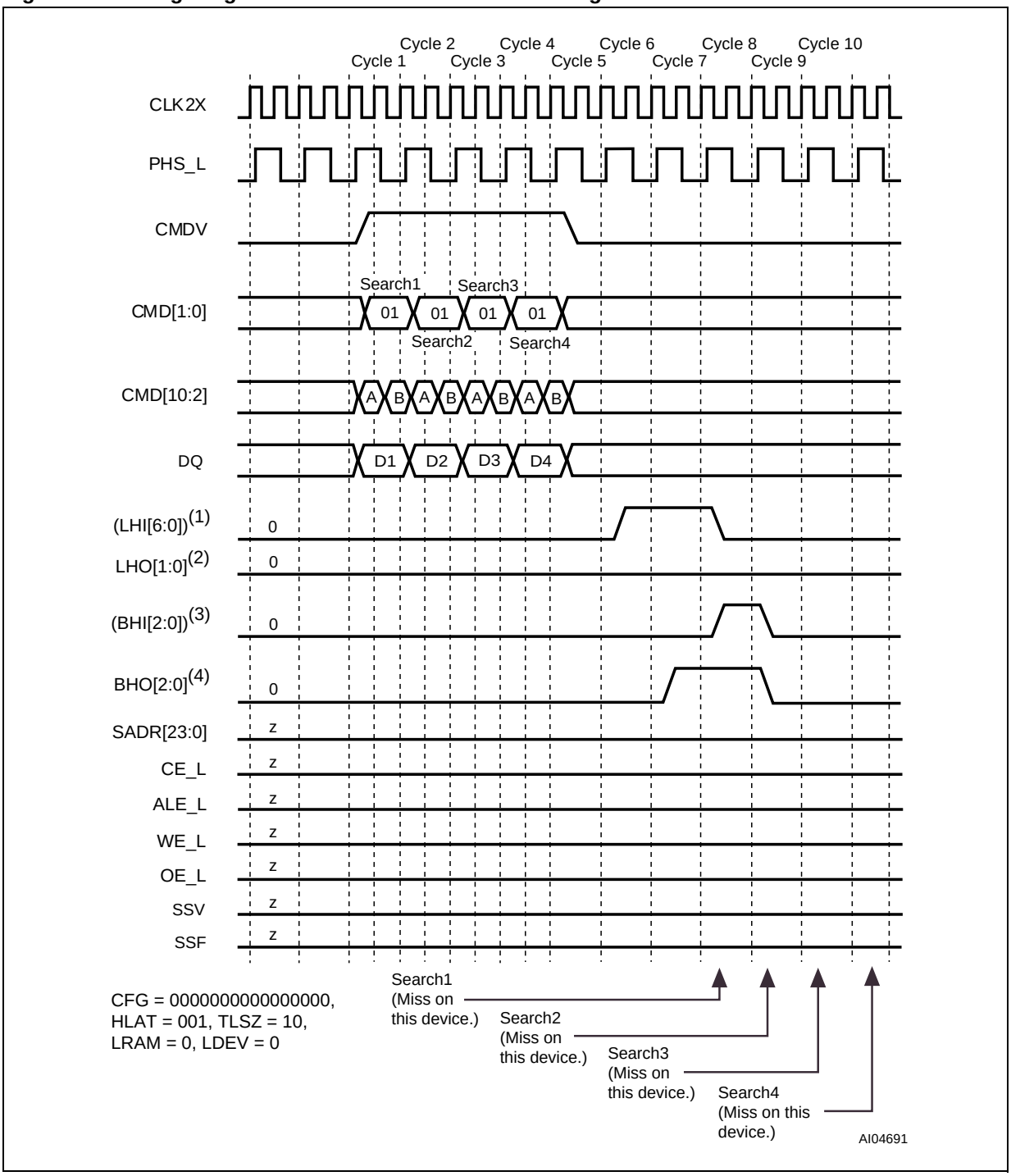
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 38. Timing Diagram for the Globally Winning Device in Block Number 2



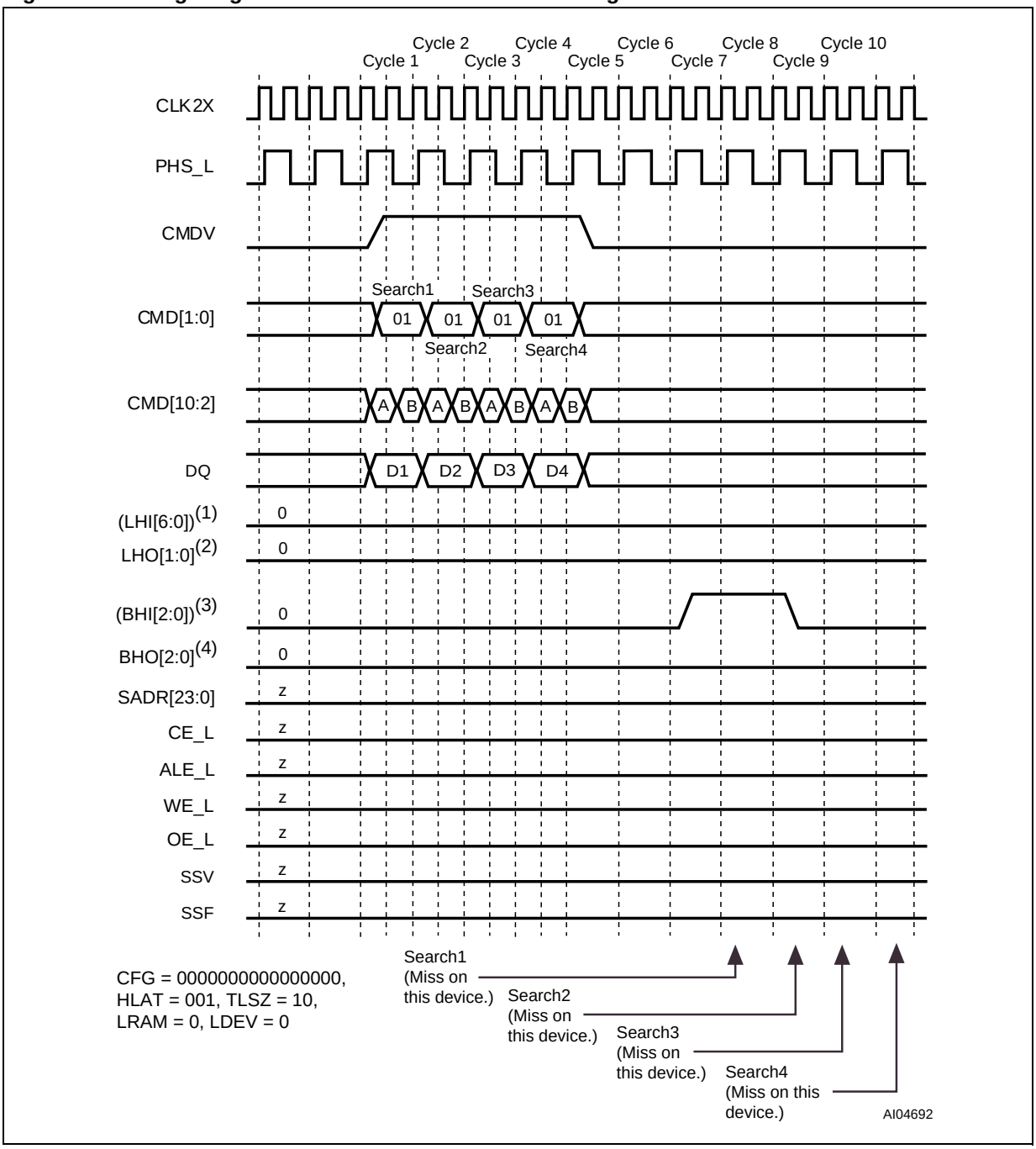
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 39. Timing Diagram for Devices Below the Winning Device in Block Number 2



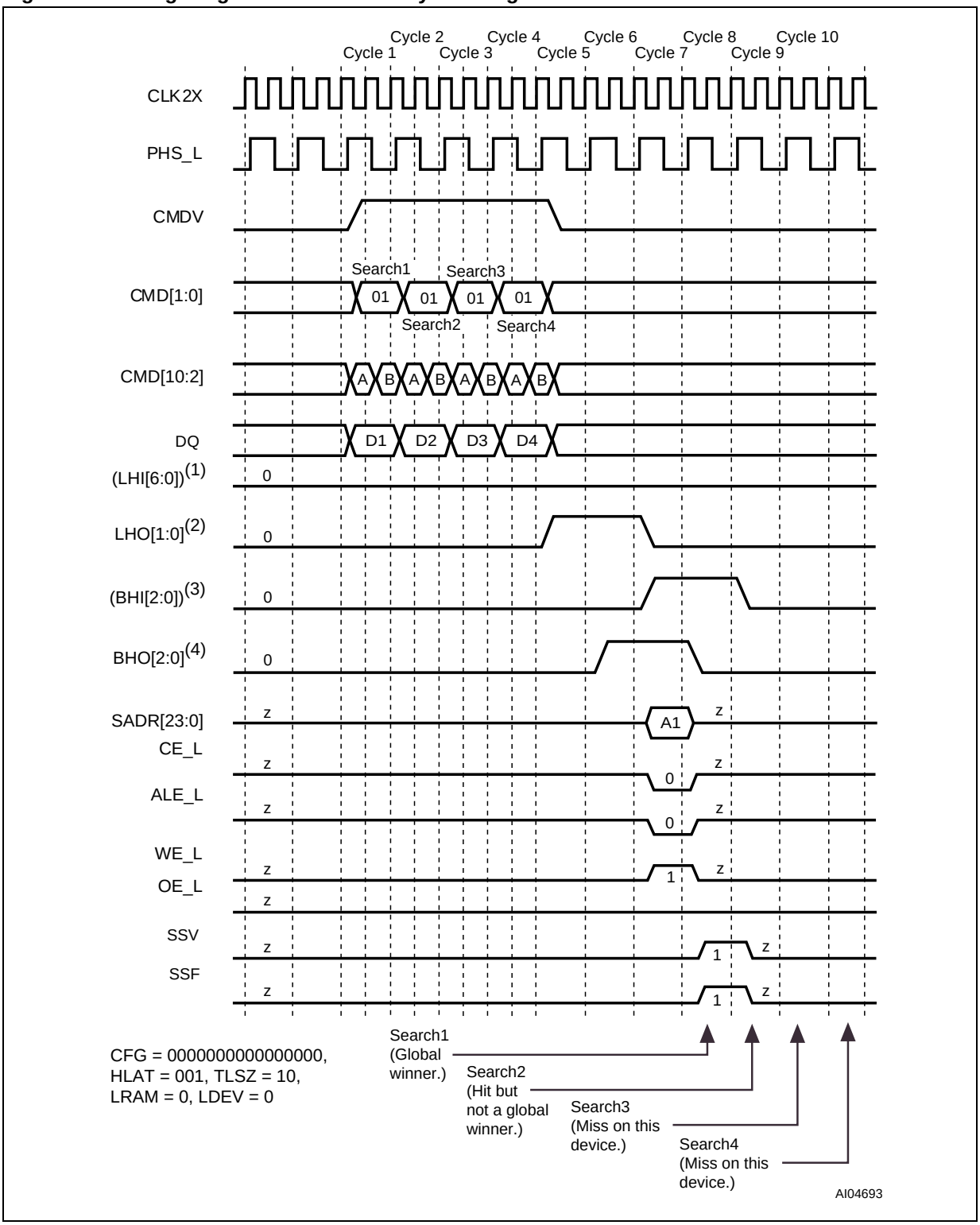
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 40. Timing Diagram for Devices Above the Winning Device in Block Number 3



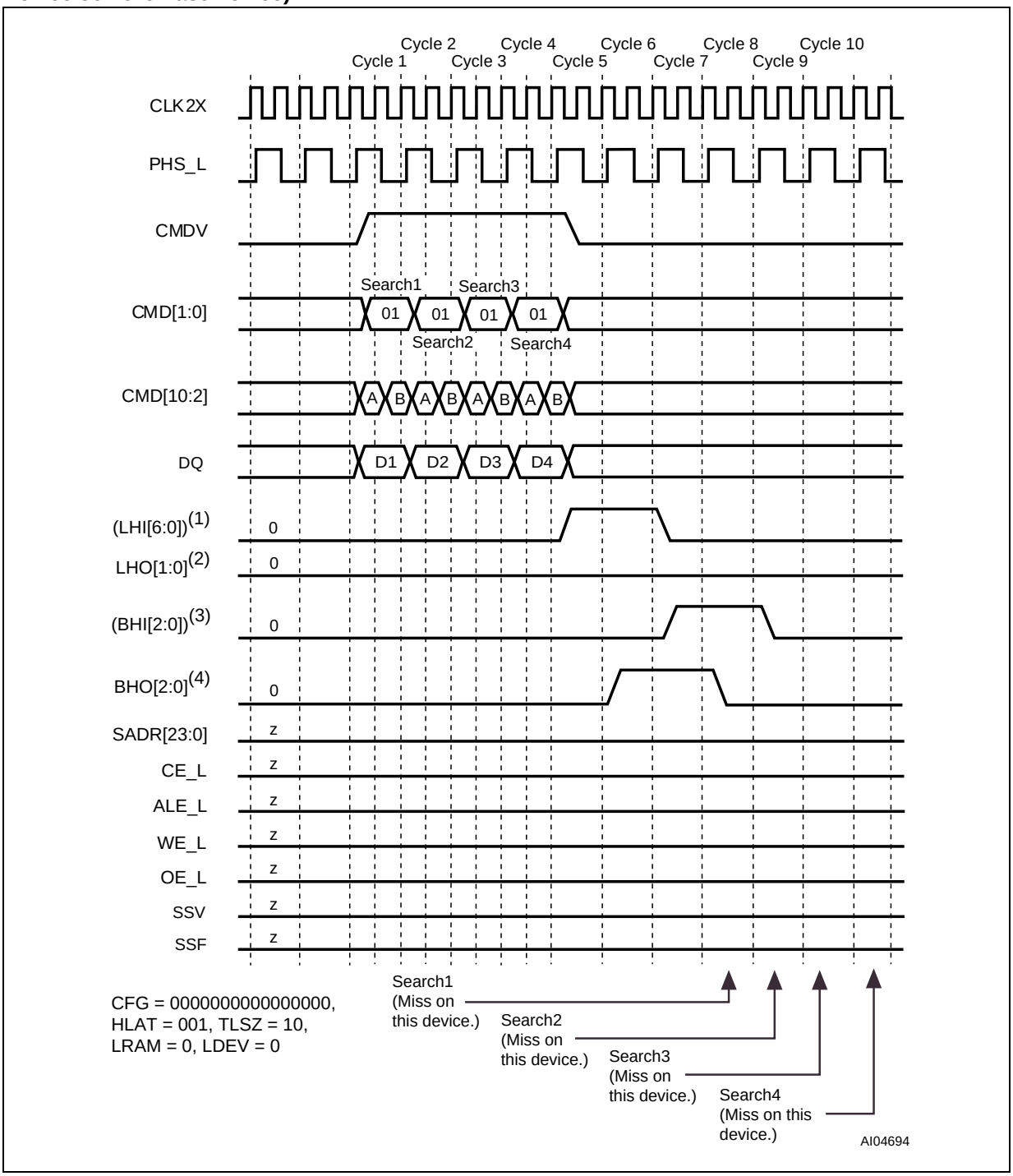
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 41. Timing Diagram for the Globally Winning Device in Block Number 3



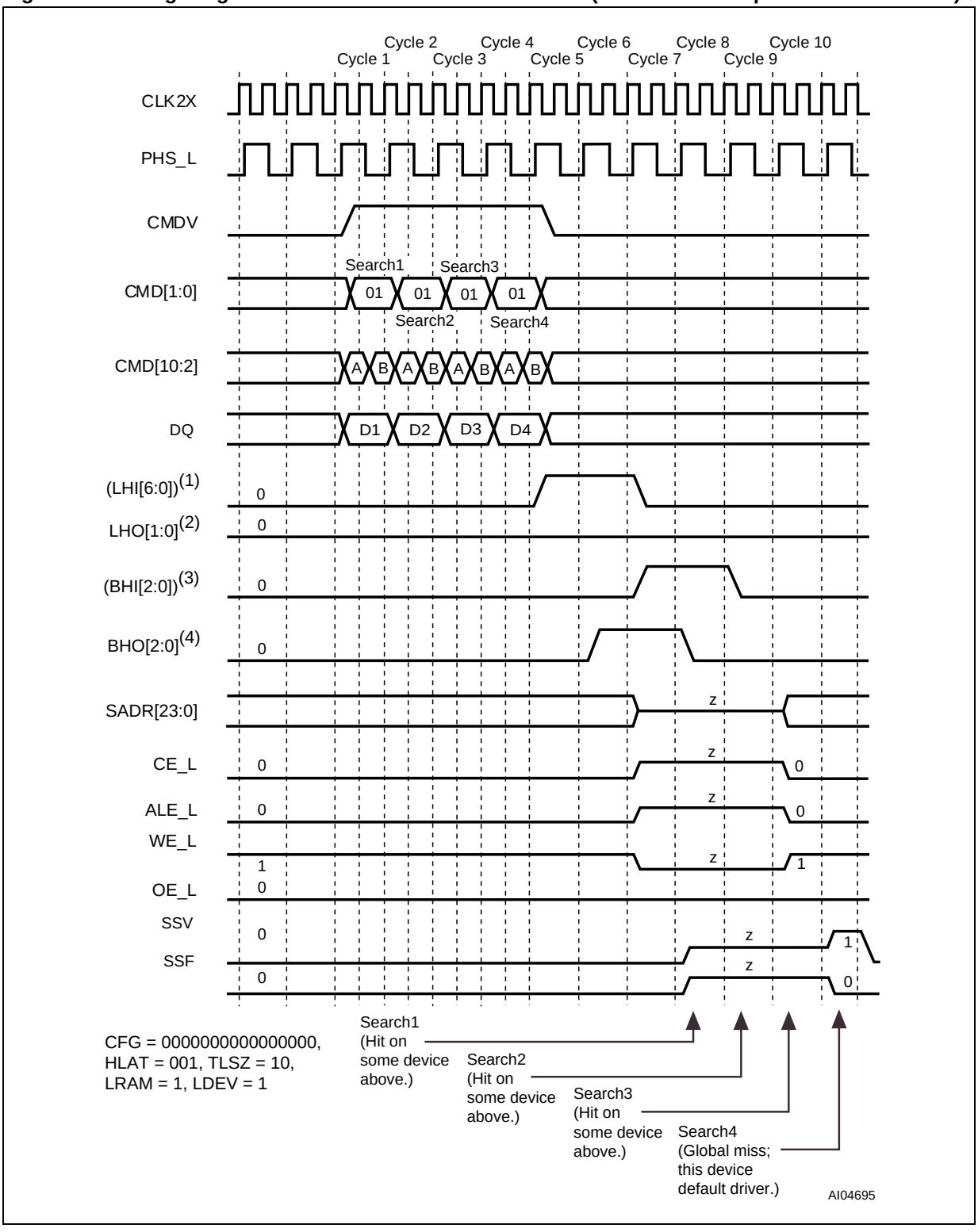
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 42. Timing Diagram for Devices Below the Winning Device in Block Number 3 (except Device 30 - the Last Device)



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 43. Timing Diagram for Device 6 in Block Number 3 (Device 30 in Depth-Cascaded Table)



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Table 32. Latency of SEARCH from Instruction to SRAM Access Cycle

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	64K x 72-bit	4
1–8 (TLSZ = 01)	512K x 72-bit	5
1–31 (TLSZ = 10)	1984K x 72-bit	6

Table 33. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

144-bit Configuration with Single Device

The hardware diagram for this search subsystem is shown in Figure 44.

Figure 45, page 66 shows the timing diagram for a SEARCH command in the 144-bit-configured table (CFG = 0101010101010101) consisting of a single device for one set of parameters. This illustration assumes that the host ASIC has programmed TLSZ to '00,' HLAT to '001,' LRAM to '1,' and LDEV to '1.'

The following is the operation sequence for a single 144-bit SEARCH command (refer to COMMAND CODES AND PARAMETERS, page 30).

– **Cycle A:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') to CMD[1:0] signals. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair for use in this SEARCH operation. CMD[8:6] signals must be driven with the same bits that will be driven on SADR[23:21] by this device if it has a hit. DQ[71:0] must be driven with the 72-bit data ([143:72]) to be compared against all even locations. The CMD[2] signal must be driven to logic '0.'

– **Cycle B:** The host ASIC continues to drive the CMDV high and applies the command code of SEARCH command ('10') on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 144-bit word presented on the DQ Bus during Cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 24). The DQ[71:0] is driven with 72-bit data ([71:0]), compared to all odd locations.

Note: For 144-bit searches, the host ASIC must supply two distinct 72-bit data words on DQ[71:0] during Cycles A and B. The even-numbered GMR of the pair specified by the GMR Index is used for masking the word in Cycle A. The odd-numbered GMR of the pair specified by the GMR Index is used for masking the word in Cycle B.

The logical 144-bit search operation is shown in Figure 46, page 67. The entire table of 144-bit entries is compared to a 144-bit word K (presented on the DQ Bus in Cycles A and B of the command) using the GMR and the local mask bits. The GMR is the 144-bit word specified by the even and odd global mask pair selected by the GMR Index in the command's Cycle A. The 144-bit word K (presented on the DQ Bus in Cycles A and B of the command) is also stored in both even and odd comparand register pairs selected by the Comparand Register Index in the command's Cycle B. The two comparand registers can subsequently be used by the LEARN command with the even comparand register stored in an even location, and the odd comparand register stored in an adjacent odd location. The word K (presented on the DQ Bus in Cycles A and B of the command) is compared with each entry in the table starting at location "0." The first matching entry's location address, "L," is the winning address that is driven as part of the SRAM address on the SADR[23:0] lines (see SRAM ADDRESSING, page 128).

Note: The matching address is always going to an even address for a 144-bit SEARCH.

The SEARCH command is a pipelined operation that executes searches at half the rate of the frequency of CLK2X for 144-bit searches in x144-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 144-bit SEARCH command cycle (two CLK2X cycles) is shown in Table 34, page 67.

For a single device in the table with TLSZ = 00, the latency of the SEARCH from command to SRAM access cycle is 4. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in Table 35, page 67.

Figure 44. Hardware Diagram for a Table with 1 Device

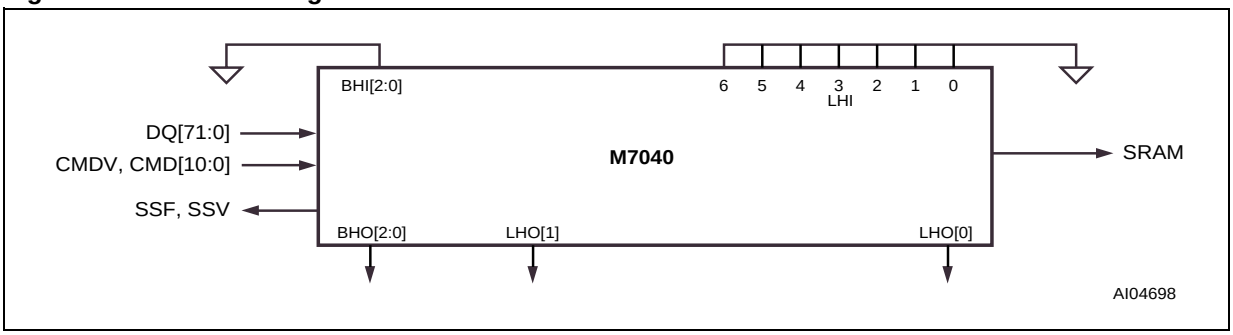


Figure 45. Timing Diagram for a 144-bit SEARCH for 1 Device

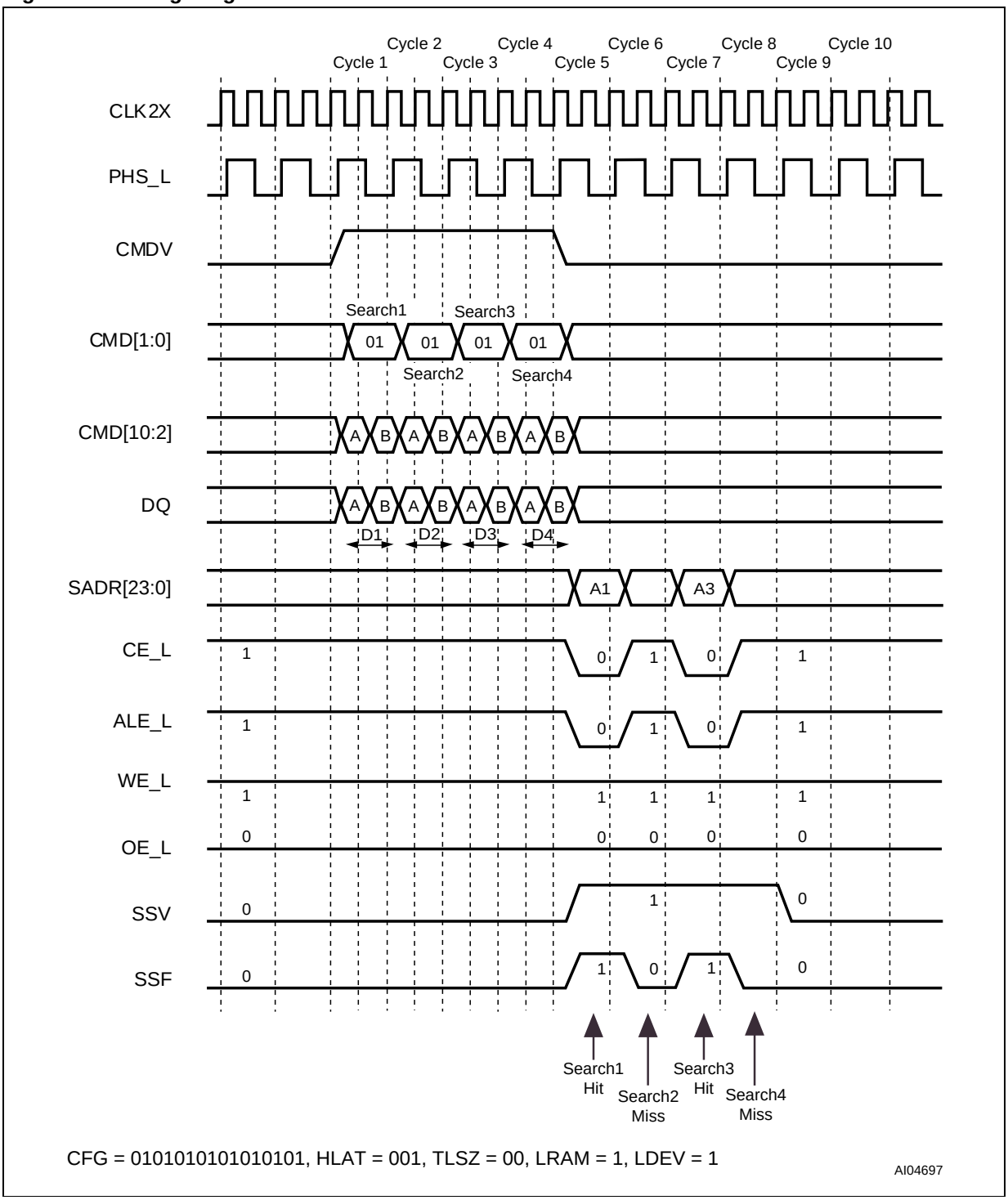


Figure 46. x144 Table with One Device

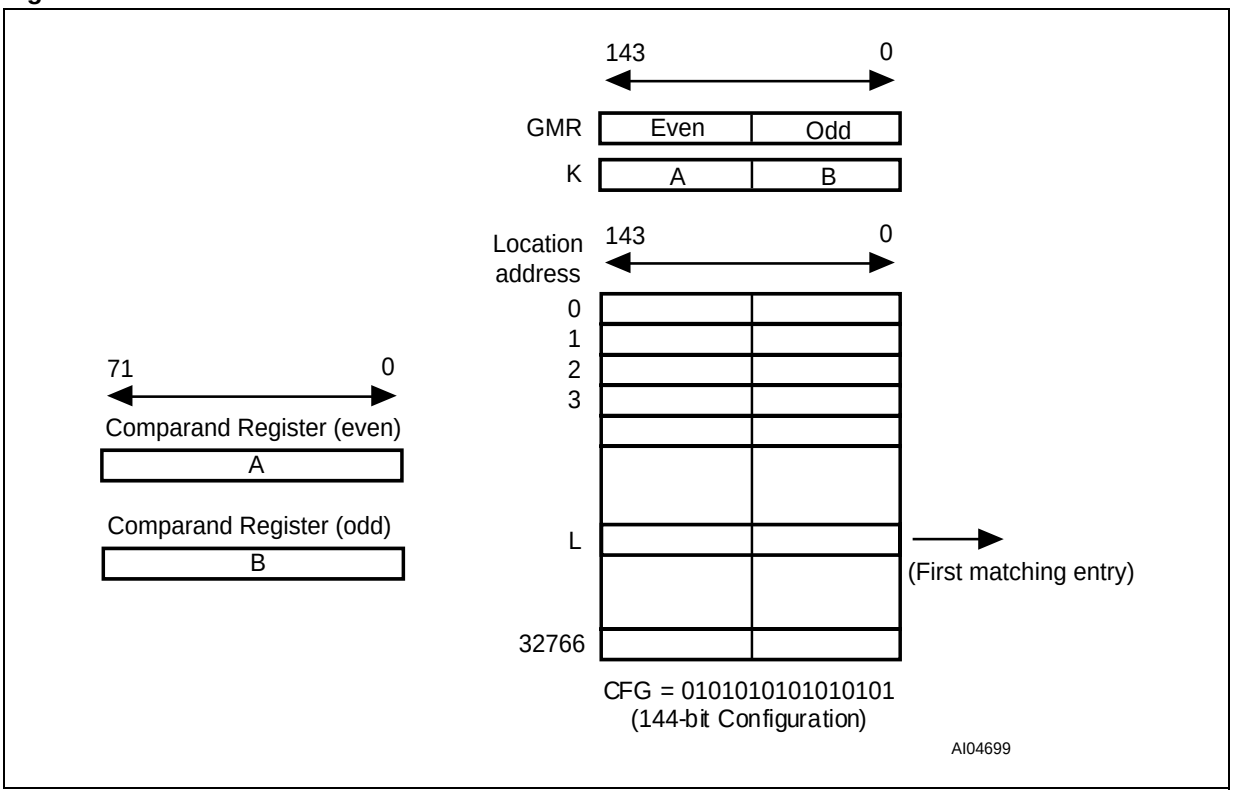


Table 34. Latency of SEARCH from Instruction to SRAM Access Cycle, 144-bit

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	32K x 144-bit	4
1–8 (TLSZ = 01)	256K x 144-bit	5
1–31 (TLSZ = 10)	992K x 144-bit	6

Table 35. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

144-bit Search on Tables Configured as x144 Using Up to Eight M7040N Devices

The hardware diagram of the search subsystem of eight devices is shown in Figure 47, page 69. The following are parameters programmed into the eight devices:

- First seven devices (devices 0–6):
  CFG = 0101010101010101, TLSZ = 01,
  HLAT = 010, LRAM = 0, and LDEV = 0.
- Eighth device (device 7):
  CFG = 0101010101010101, TLSZ = 01,
  HLAT = 010, LRAM = 1, and LDEV = 1.

Note: All eight devices must be programmed with the same value of TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (Device 7 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (Devices 0 through 6 in this case).

Figure 49, page 71 shows the timing diagram for a SEARCH command in the 144-bit-configured table of eight devices for Device 0. Figure 50, page 72 shows the timing diagram for a SEARCH command in the 144-bit-configured table consisting of eight devices for Device 1. Figure 51, page 73 shows the timing diagram for a SEARCH command in the 144-bit configured table consisting of eight devices for Device 7 (the last device in this specific table). For these timing diagrams, four 144-bit searches are performed sequentially, and the following HIT/MISS assumptions were made (see Table 36)

The following is the sequence of operation for a single 144-bit SEARCH command (see COMMAND CODES AND PARAMETERS, page 30).

- **Cycle A:** The host ASIC drives CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair for use in this SEARCH operation. CMD[8:6] signals must be driven with the same bits that will be driven by this device on SADR[23:21] if it has a hit. DQ[71:0] must be driven with the 72-bit data ([143:72]) in order to be compared against all even locations. The CMD[2] signal must be driven to a logic '0.'
- **Cycle B:** The host ASIC continues to drive CMDV high and to apply the command code for SEARCH command ('10') on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 144-bit word presented on the DQ Bus during Cycles A and B. CMD[8:6] signals must be driven with the SSR Index that will be used for storing the address of the matching entry and the Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 24). The DQ[71:0] is driven with 72-bit data ([71:0]) compared against all odd locations.

The logical 144-bit search operation is shown in Figure 48, page 70. The entire table (eight devices of 144-bit entries) is compared to a 144-bit word K (presented on the DQ Bus in Cycles A and B of the command) using the GMR and local mask bits. The GMR is the 144-bit word specified by the even and odd global mask pair selected by the GMR Index in the command's Cycle A.

The 144-bit word K (presented on the DQ Bus in Cycles A and B of the command) is also stored in the even and odd comparand registers specified by the Comparand Register Index in the command's Cycle B. In x144 configurations, the even and odd comparand registers can subsequently be used by the LEARN command in only one of the devices (the first non-full device). The word K (presented on the DQ Bus in Cycles A and B of the command) is compared to each entry in the table starting at location "0." The first matching entry's location, "L," is the winning address that is driven as part of the SRAM address on the SADR[23:0] lines (see SRAM ADDRESSING, page 128). The global winning device will drive the bus in a specific cycle. On global miss cycles the device with LRAM = 1 (the default driving device for the SRAM Bus) and LDEV = 1 (the default driving device for SSF and SSV signals) will be the default driver for such missed cycles.

Note: During 144-bit searches of 144-bit-configured tables, the search hit will always be at an even address.

The SEARCH command is a pipelined operation and executes a search at half the rate of the frequency of CLK2X for 144-bit searches in x144-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 144-bit SEARCH command cycle (two CLK2X cycles) is shown in Table 37, page 74.

For one to eight devices in the table and TLSZ = 01, the latency of a SEARCH from command to SRAM access cycle is 5. In addition, SSV and SSF shift further to the right for different values of HLAT as specified in Table 38, page 74.

Table 36. Hit/Miss Assumption

Search Number	1	2	3	4
Device 0	Hit	Miss	Hit	Miss
Device 1	Miss	Hit	Hit	Miss
Device 2-6	Miss	Miss	Miss	Miss
Device 7	Miss	Miss	Hit	Hit

Figure 47. Hardware Diagram for a Table with Eight Devices

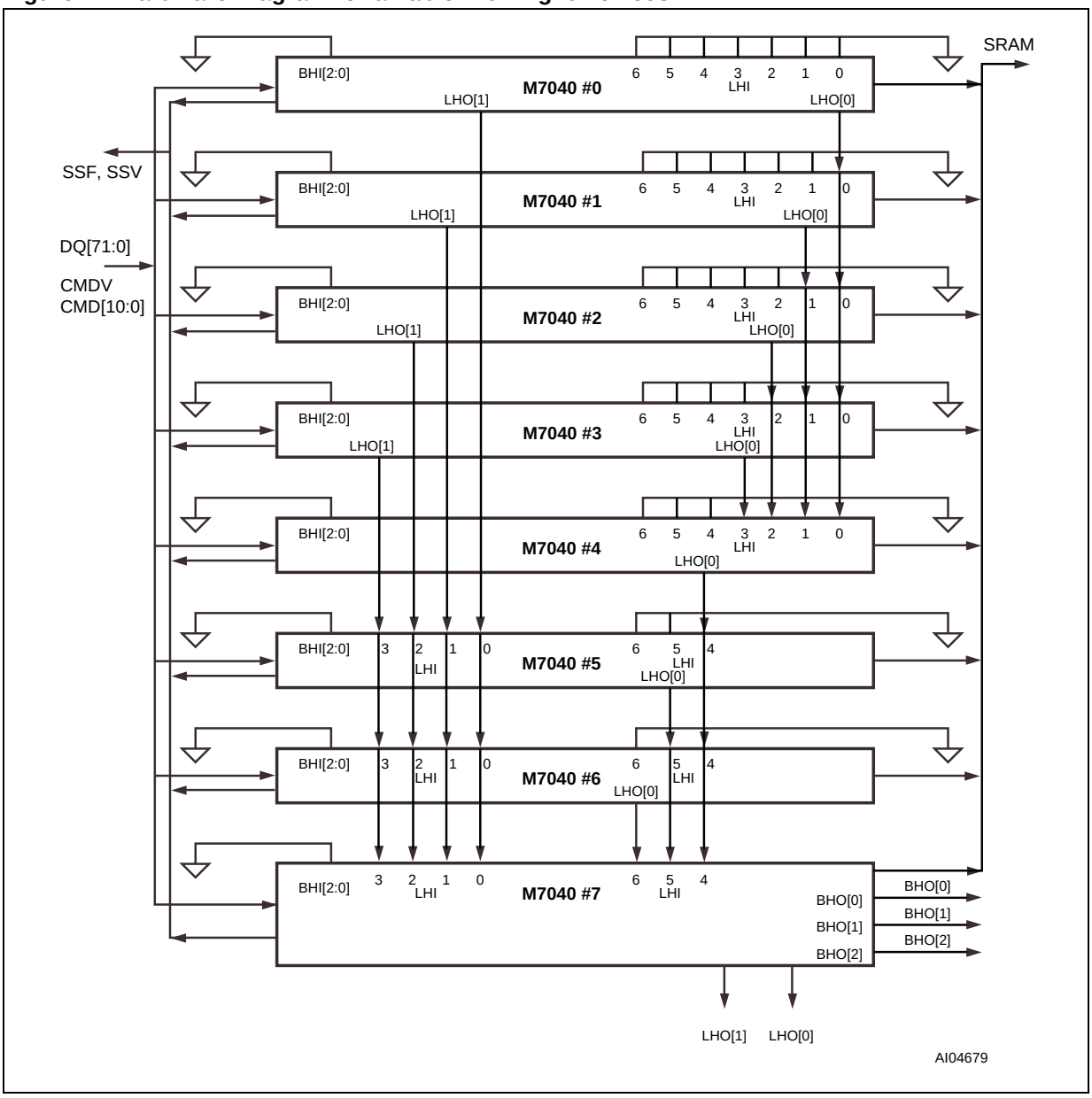
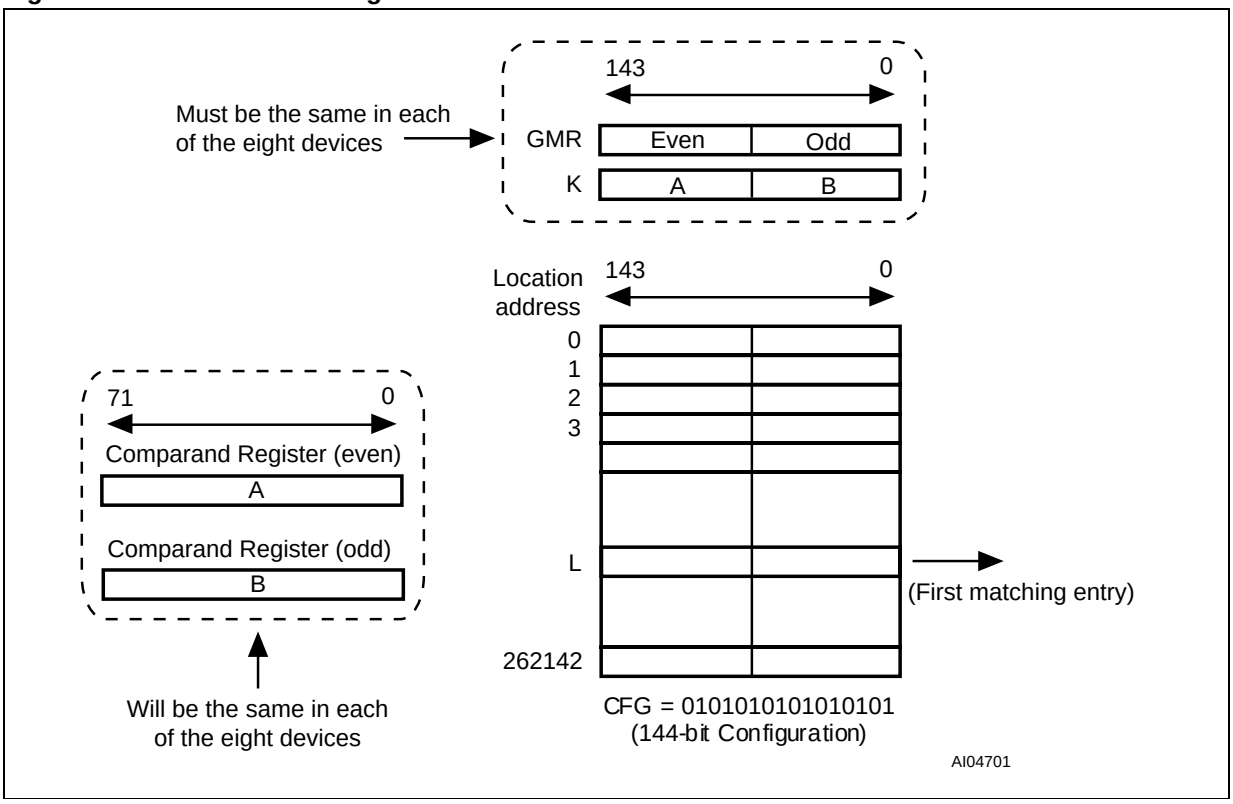
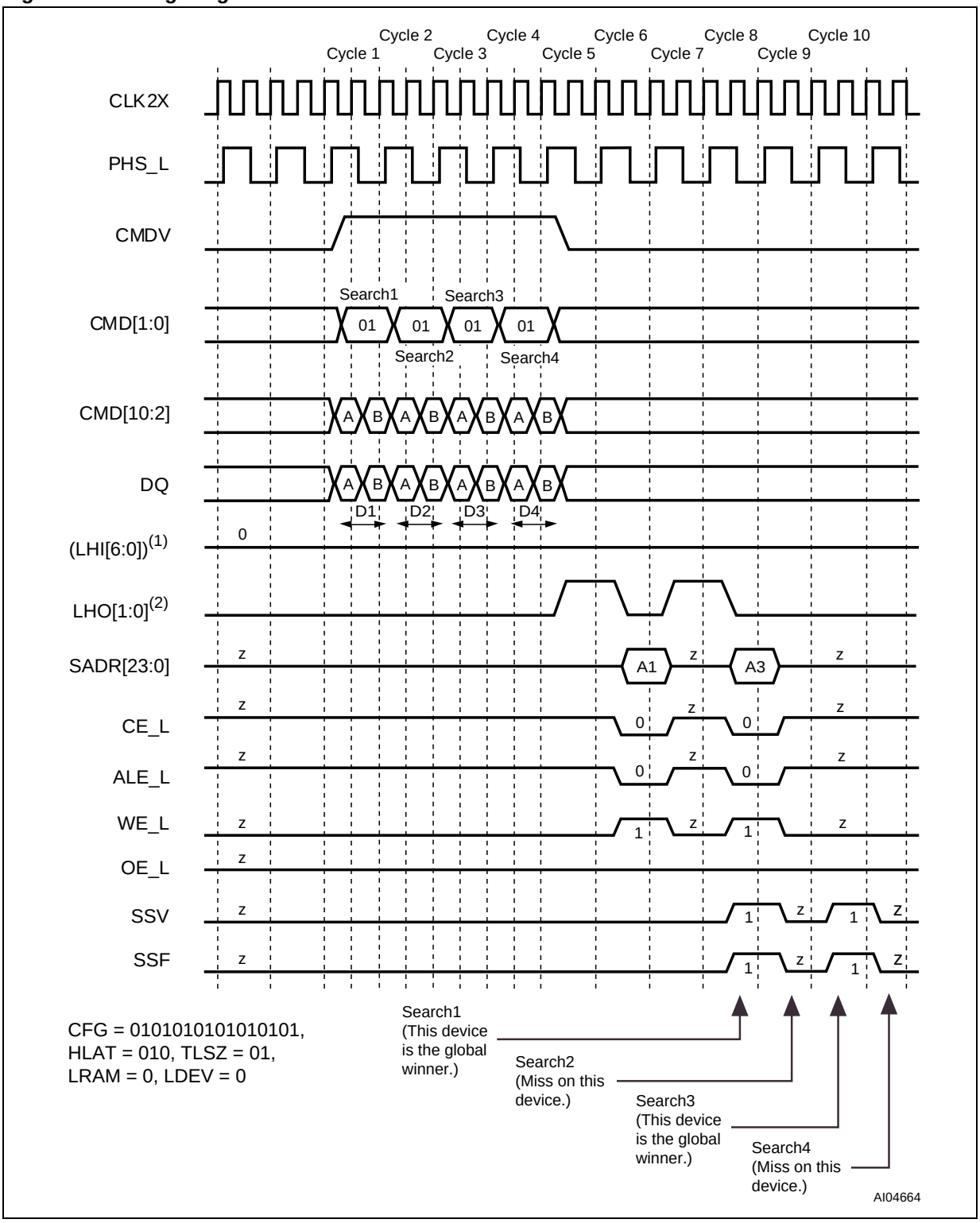


Figure 48. x144 Table with Eight Devices



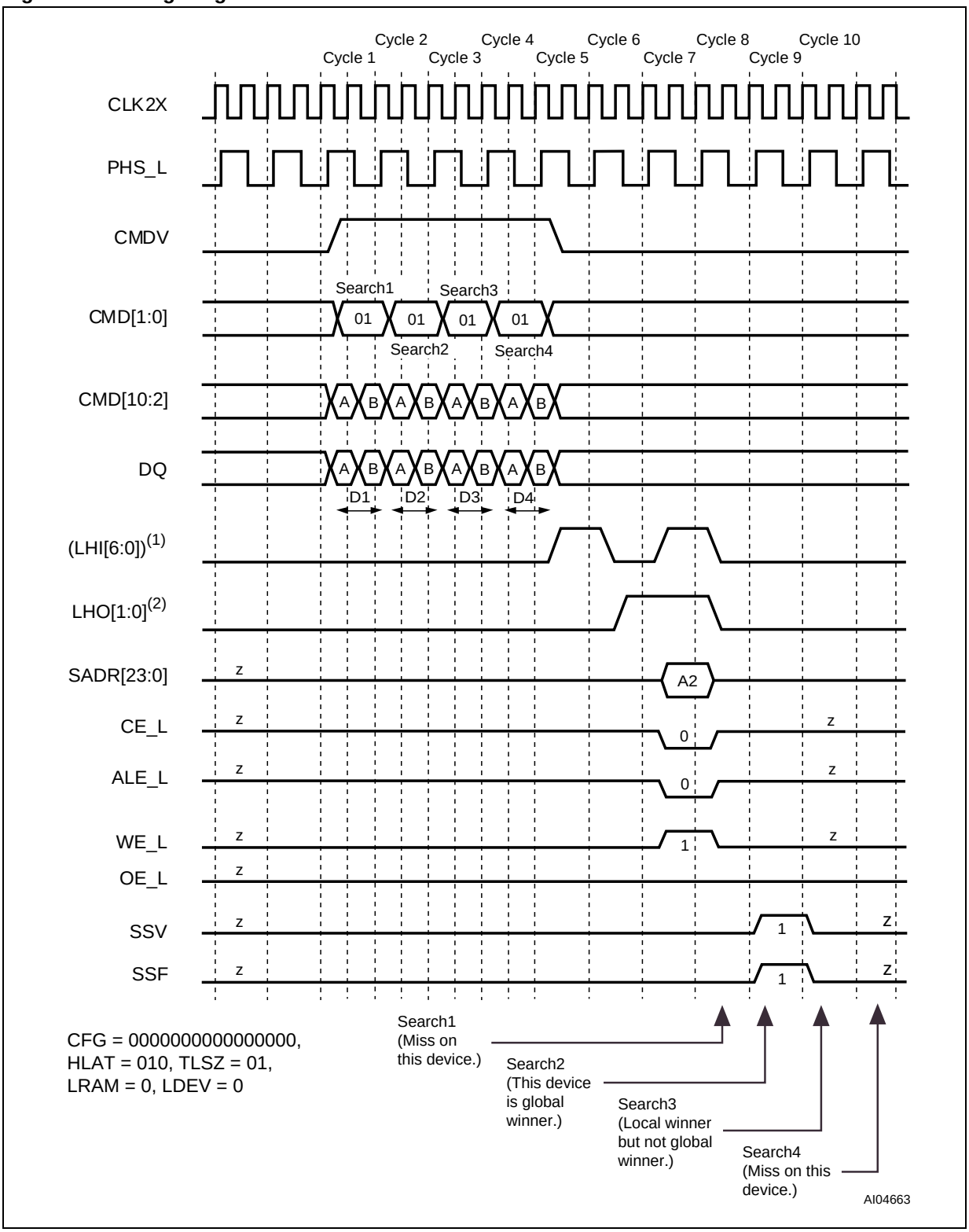
Timing Diagrams for x144 Using Up to Eight M7040N Devices

Figure 49. Timing Diagram for 144-bit SEARCH for Device Number 0



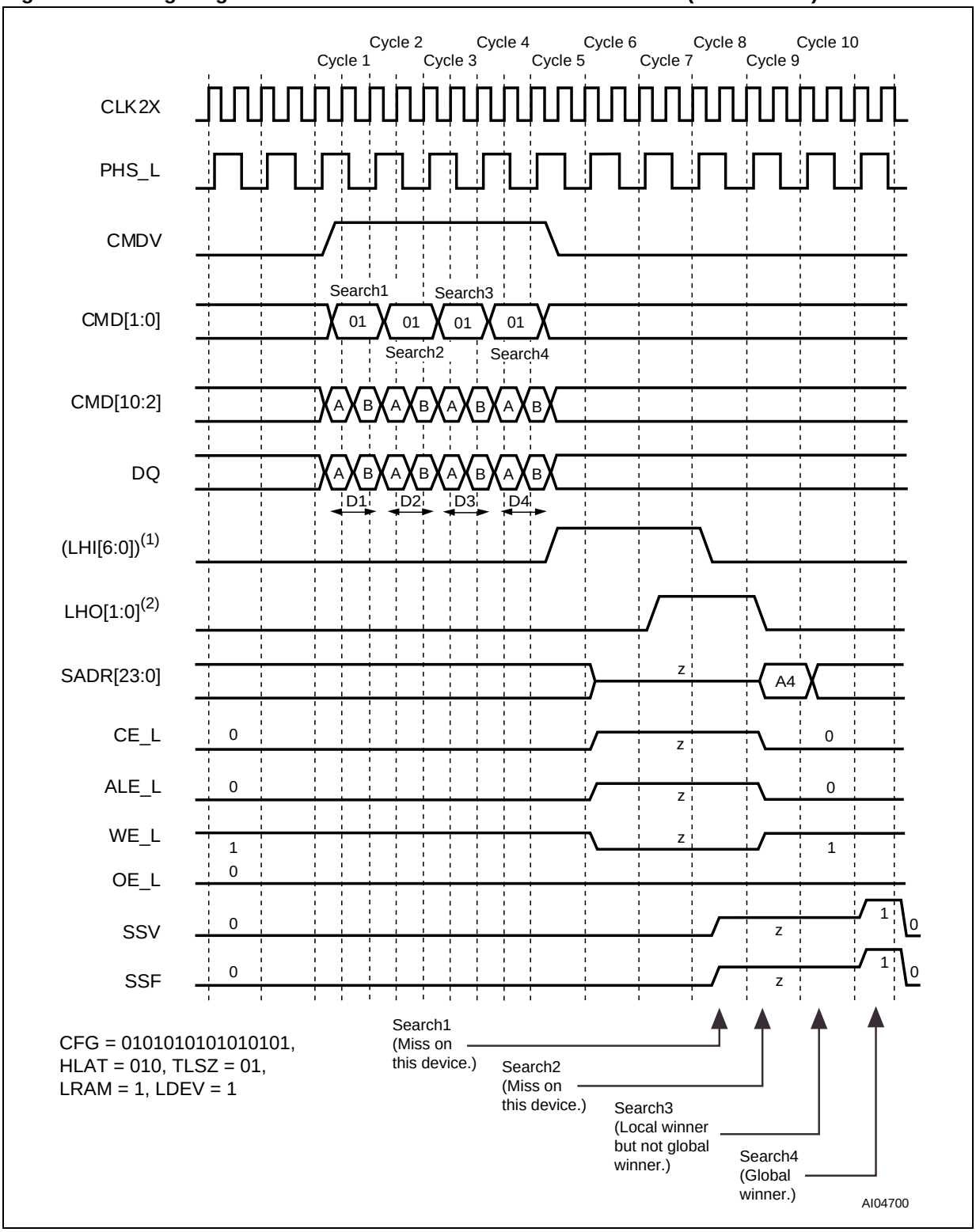
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.

Figure 50. Timing Diagram for 144-bit SEARCH for Device Number 1



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.

Figure 51. Timing Diagram for 144-bit SEARCH for Device Number 7 (Last Device)



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.

Table 37. Latency of SEARCH from Instruction to SRAM Access Cycle, 144-bit

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	32K x 144-bit	4
1–8 (TLSZ = 01)	256K x 144-bit	5
1–31 (TLSZ = 10)	992K x 144-bit	6

Table 38. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

144-bit Search on Tables Configured as x144 Using Up to 31 M7040N Devices

The hardware diagram of the search subsystem of 31 devices is shown in Figure 52, page 76. Each of the four blocks in the diagram represents a block of eight M7040N devices (except the last, which has seven devices).The diagram for a block of eight devices is shown in Figure 53, page 77. Following are the parameters programmed into the 31 devices.

First thirty devices (devices 0–29):
CFG = 0101010101010101, TLSZ = 10,
HLAT = 001, LRAM = 0, and LDEV = 0.

Thirty-first device (device 30):
CFG = 0101010101010101, TLSZ = 10,
HLAT = 001, LRAM = 1, and LDEV = 1.

Note: All 31 devices must be programmed with the same value of TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (Device 30 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (Devices 0 through 29 in this case).

The timing diagrams referred to in this paragraph reference the HIT/MISS assumptions defined in Table 39, page 75. For the purpose of illustrating timings, it is further assumed that the there is only one device with a matching entry in each of the blocks. Figure 55, page 79 shows the timing diagram for a SEARCH command in the 144-bit-configured table (31 devices) for each of the eight devices in Block 0. Figure 56, page 80 shows the timing diagram for SEARCH command in the 72-bit-configured table (31 devices) for all the devices in Block 1 above the winning device in that block. Figure 57, page 81 shows the timing diagram for the globally winning device (the final winner within its own block and all blocks) in Block 1. Figure 58, page 82 shows the timing diagram for all the devices below the globally winning device in Block 1. Figure 59, page 83, Figure 60, page 84, and Figure 61, page 85 respectively show the timing diagrams of the devices above globally winning device, the globally winning device and devices below the globally winning device for Block 2. Figure 62, page 86, Figure 63, page 87, Figure 64, page 88, and Figure 65, page 89 respectively show the timing diagrams of the devices above the globally winning device, the globally winning device, and devices below the globally winning device except the last device (Device 30), and the last device (Device 30) for Block 3.

The following is the sequence of operation for a single 144-bit SEARCH command (see COMMAND CODES AND PARAMETERS, page 30).

– **Cycle A:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair for use in this SEARCH operation. CMD[8:6] signals must be driven with the bits that will be driven on SADR[23:21] by this device if it has a hit. DQ[71:0] must be driven with the 72-bit data ([143:72]) in order to be compared against all even locations. The CMD[2] signal must be driven to logic '0.'

– **Cycle B:** The host ASIC continues to drive the CMDV high and to apply SEARCH command code ('10') on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 144-bit word presented on the DQ Bus during Cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 24). The DQ[71:0] is driven with 72-bit data ([71:0]) to be compared against all odd locations.

The logical 144-bit search operation is as shown in Figure 54, page 78. The entire table of 31 devices (consisting of 144-bit entries) is compared against a 144-bit word K that is presented on the DQ Bus in Cycles A and B of the command using the GMR and local mask bits. The GMR is the 144-bit word specified by the even and odd global mask pair selected by the GMR Index in the command's Cycle A.

The 144-bit word K that is presented on the DQ Bus in Cycles A and B of the command is also stored in the even and odd comparand registers specified by the Comparand Register Index in the command's Cycle B. In x144 configurations, the even and odd comparand registers can subsequently be used by the LEARN command in only the first non-full device.

Note: The LEARN command is supported for only one of the blocks consisting of up to eight devices in a depth-cascaded table of more than one block.

The word K that is presented on the DQ Bus in Cycles A and B of the command is compared with each entry in the table starting at location "0." The first matching entry's location address, "L," is the winning address that is driven as part of the SRAM address on the SADR[23:0] lines (see SRAM ADDRESSING, page 128). The global winning device will drive the bus in a specific cycle. On global miss cycles the device with LRAM = 1 (the default driving device for the SRAM bus) and LDEV = 1 (the default driving device for SSF and SSV signals) will be the default driver for such missed cycles.

Note: During 144-bit searches of 144-bit-configured tables, the search hit will always be at an even address.

The SEARCH command is a pipelined operation. It executes a search at half the rate of the frequency of CLK2X for 144-bit searches in x144-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 144-bit SEARCH command cycle (two CLK2X cycles) is shown in Table 40, page 90.

The latency of a search from command to the SRAM access cycle is 6 for 1–31 devices in the table and where TLSZ = 10. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in Table 41, page 90.

The 144-bit SEARCH operation is pipelined and executes as follows:

– Four cycles from the SEARCH command, each of the devices knows the outcome internal to it for that operation.

– In the fifth cycle after the SEARCH command, the devices in a block (being less than or equal to eight devices resolving the winner within them using the LHI[6:0] and LHO[1:0] signalling mechanism) arbitrate for a winner amongst them.

– In the sixth cycle after the SEARCH command, the blocks (of devices) resolve the winning block through the BHI[2:0] and BHO[2:0] signalling mechanism. The winning device in the winning block is the global winning device for a SEARCH operation.

Table 39. Hit/Miss Assumption

Search Number	1	2	3	4
Block 0	Miss	Miss	Miss	Miss
Block 1	Miss	Miss	Hit	Miss
Block 2	Miss	Hit	Hit	Miss
Block 3	Hit	Hit	Miss	Miss

Figure 52. Hardware Diagram for a Table with 31 Devices

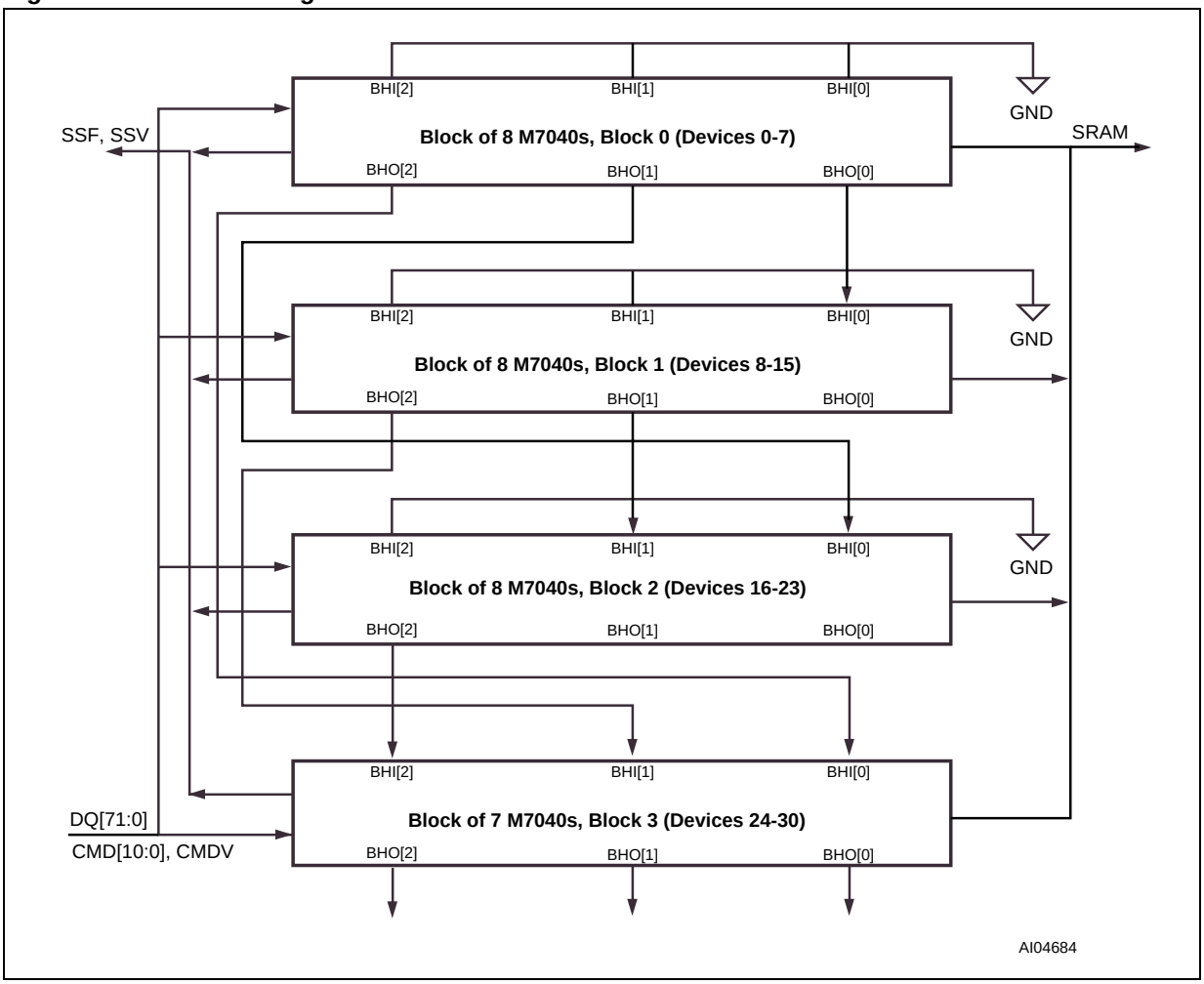


Figure 53. Hardware Diagram for a Block of Up to Eight Devices

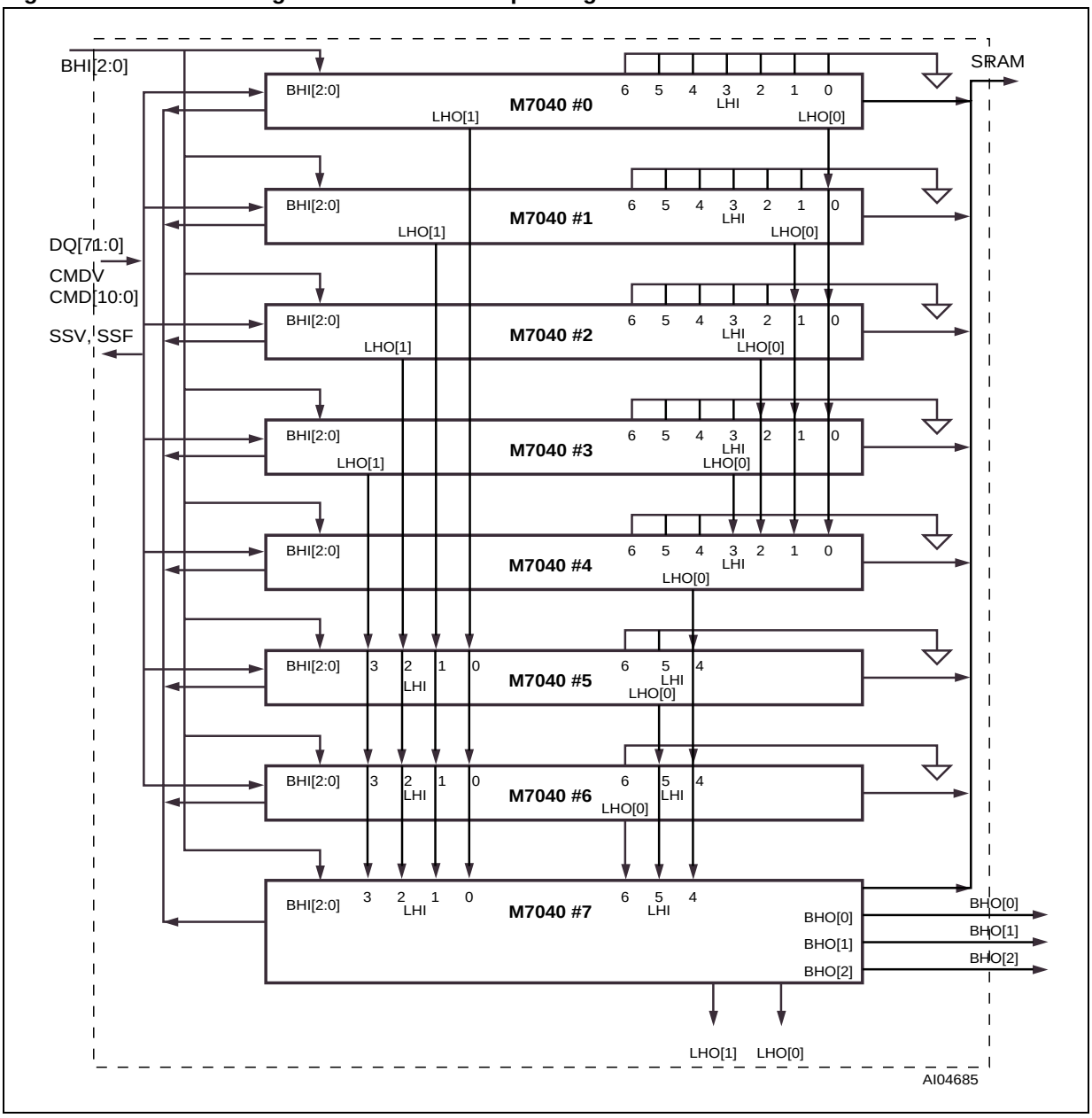
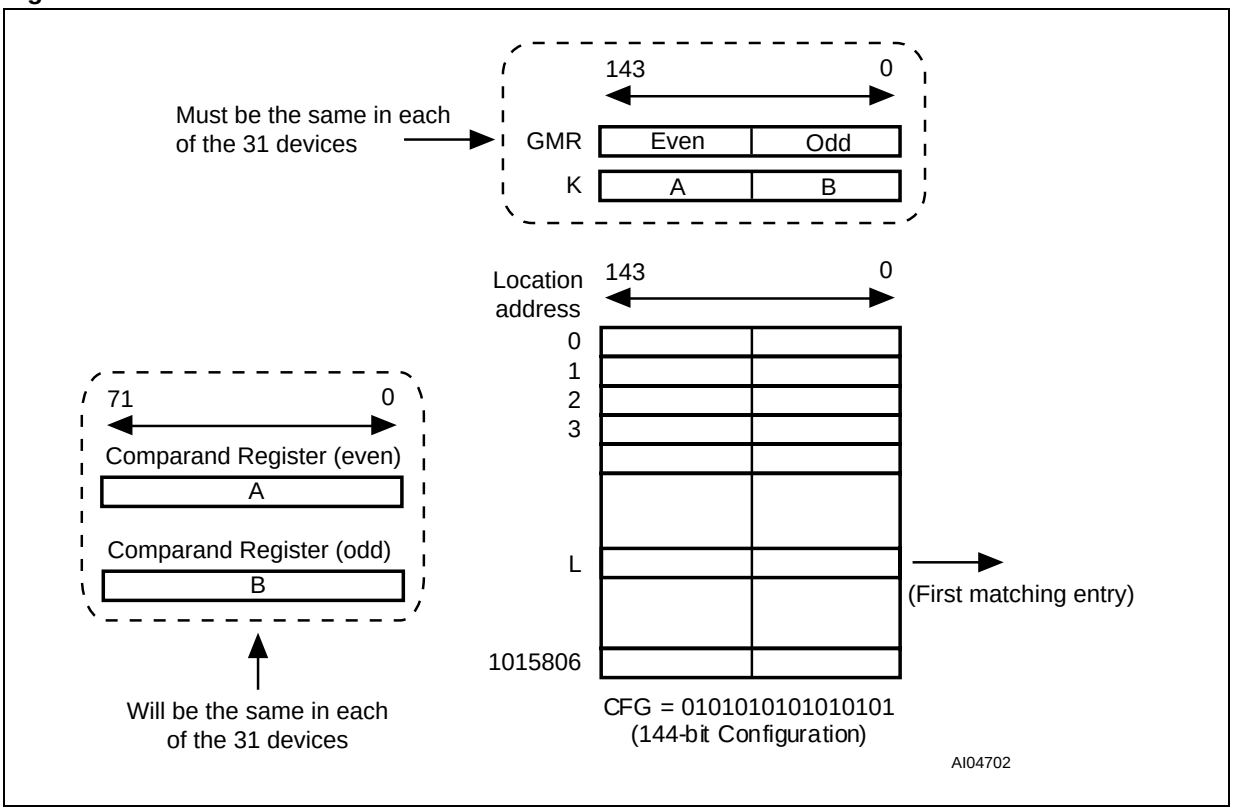
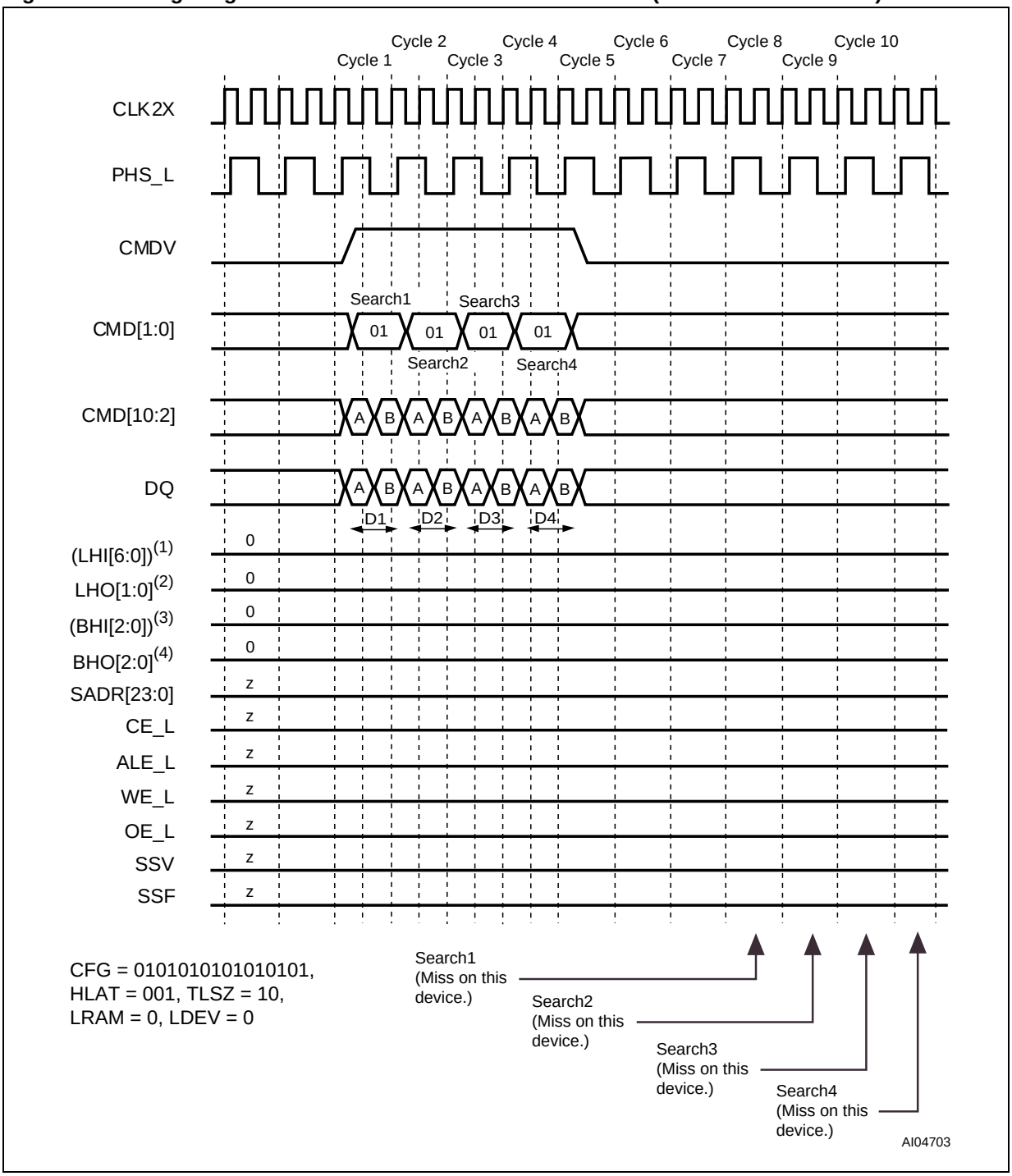


Figure 54. x144 Table with 31 Devices



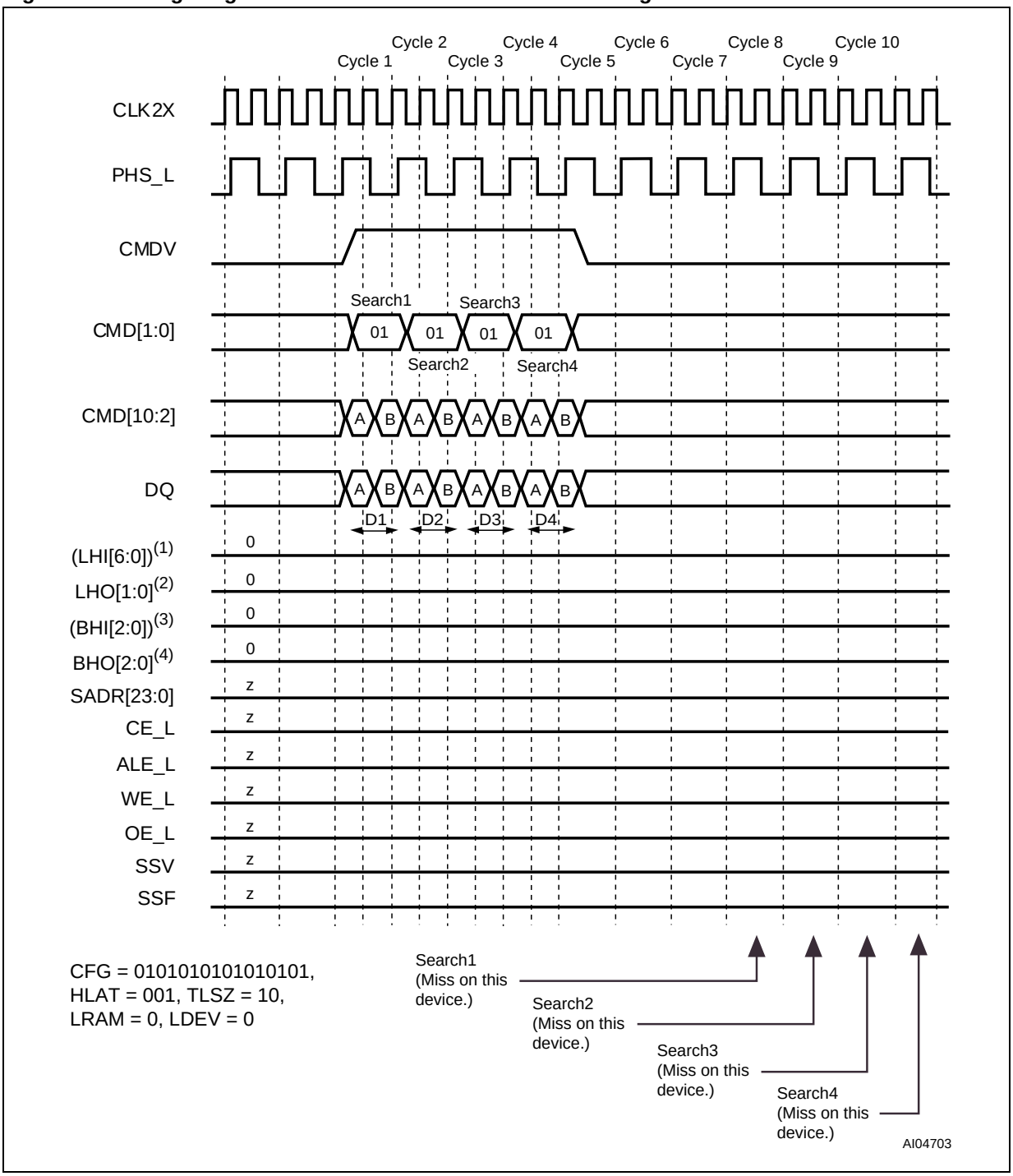
Timing Diagrams for x144 Using Up to 31 M7040N Devices

Figure 55. Timing Diagram for Each Device in Block Number 0 (Miss on Each Device)



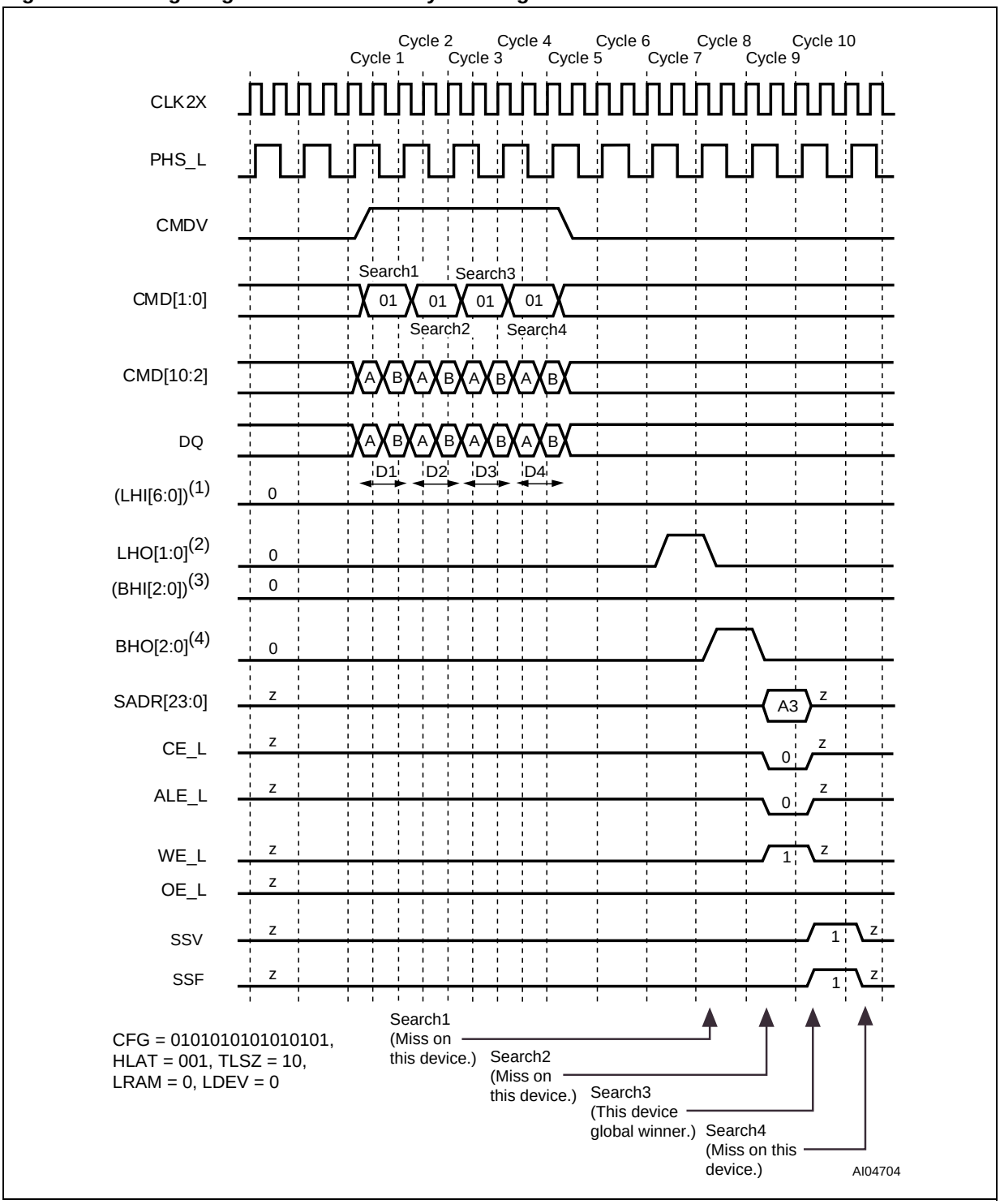
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 56. Timing Diagram for Each Device Above the Winning Device in Block Number 1



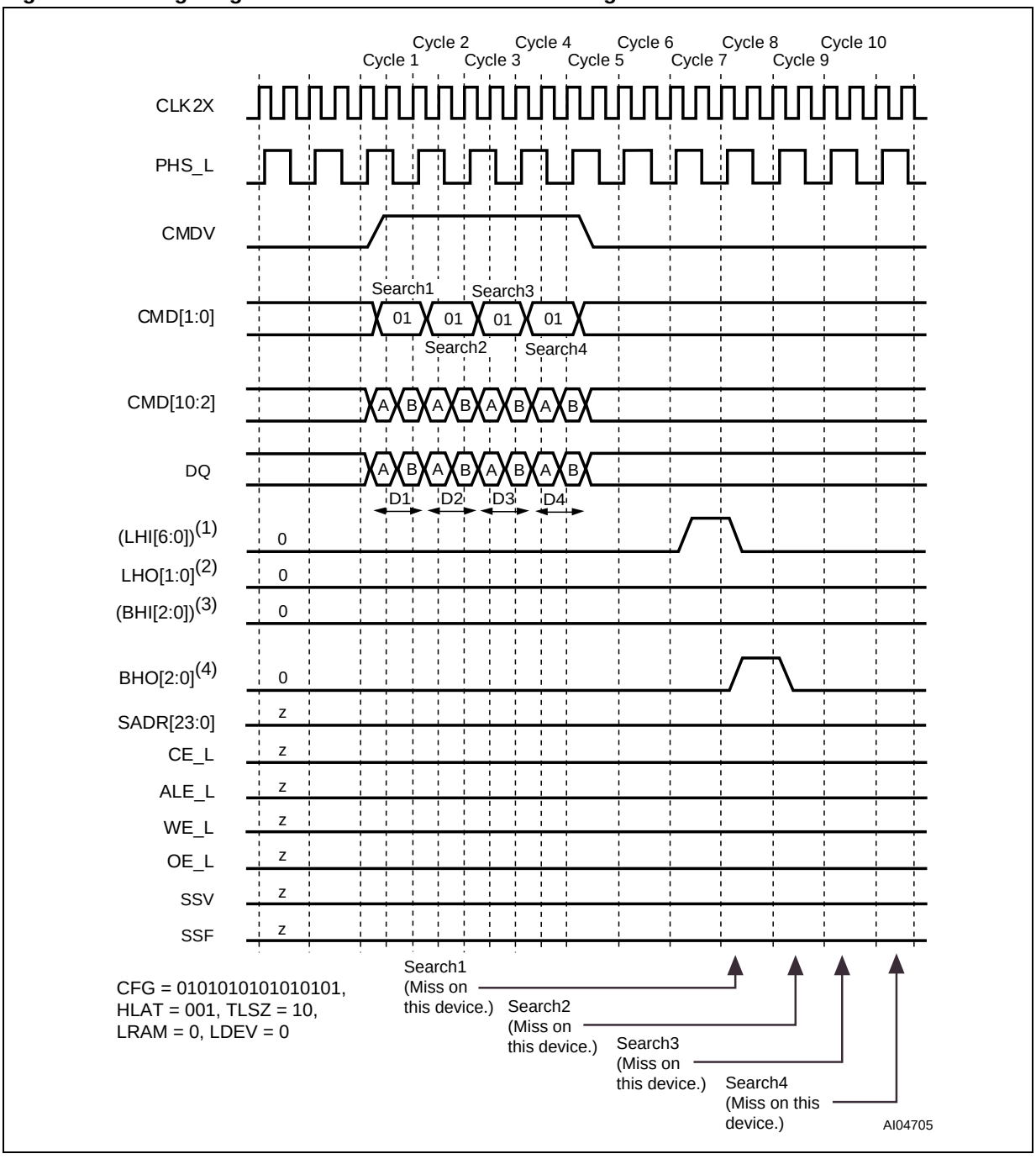
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 57. Timing Diagram for the Globally Winning Device in Block Number 1



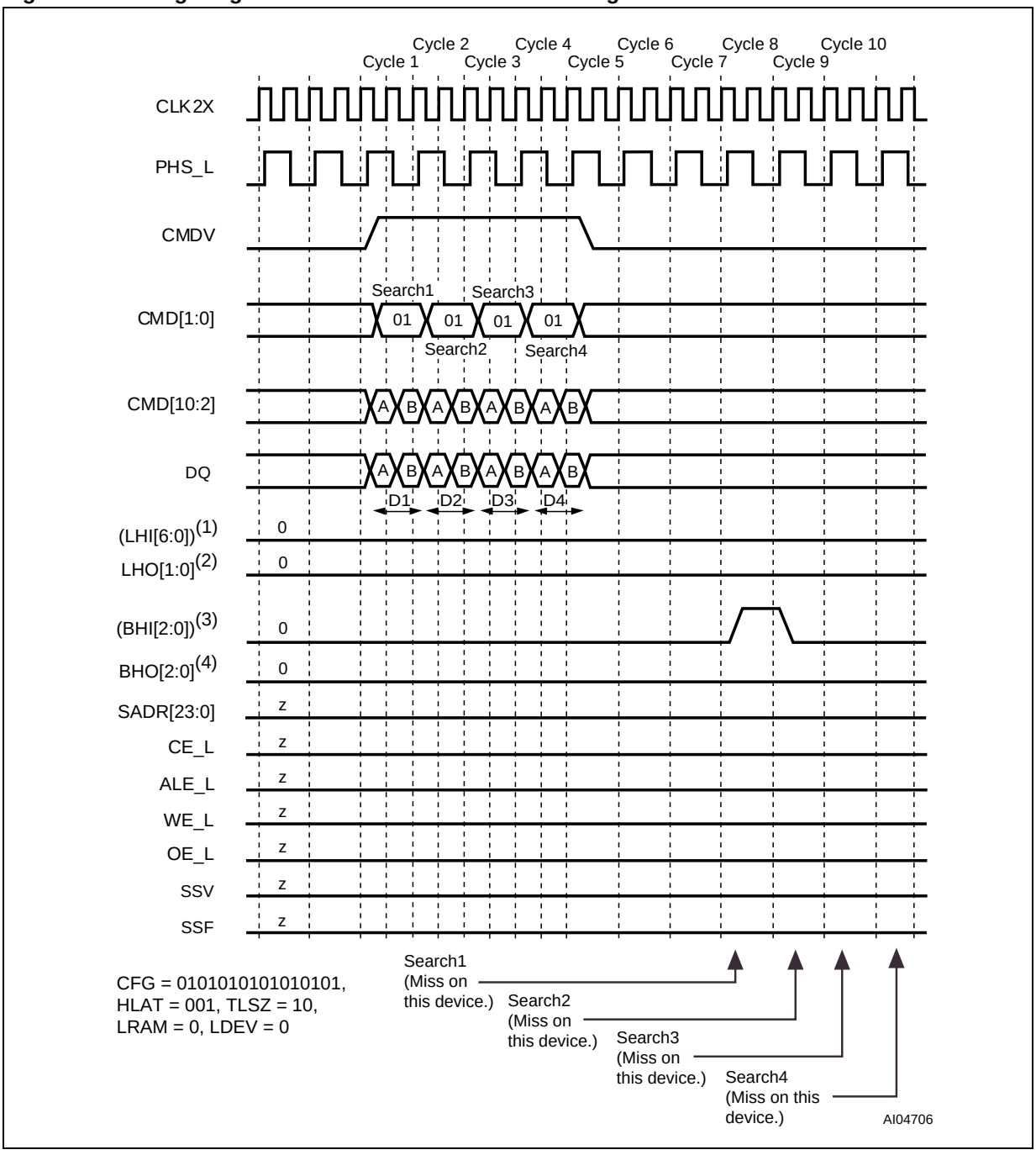
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 58. Timing Diagram for Devices Below the Winning Device in Block Number 1



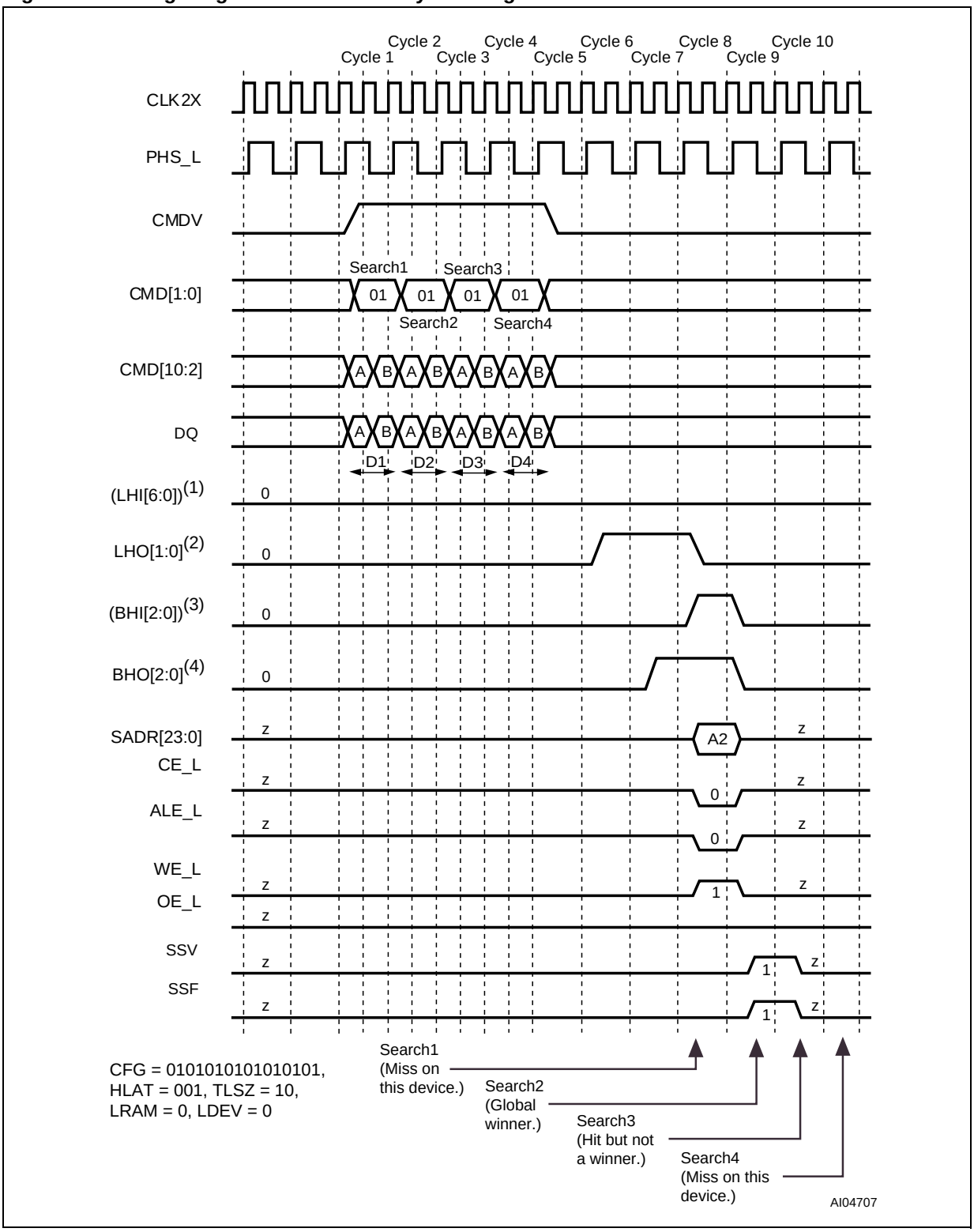
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 59. Timing Diagram for Devices Above the Winning Device in Block Number 2



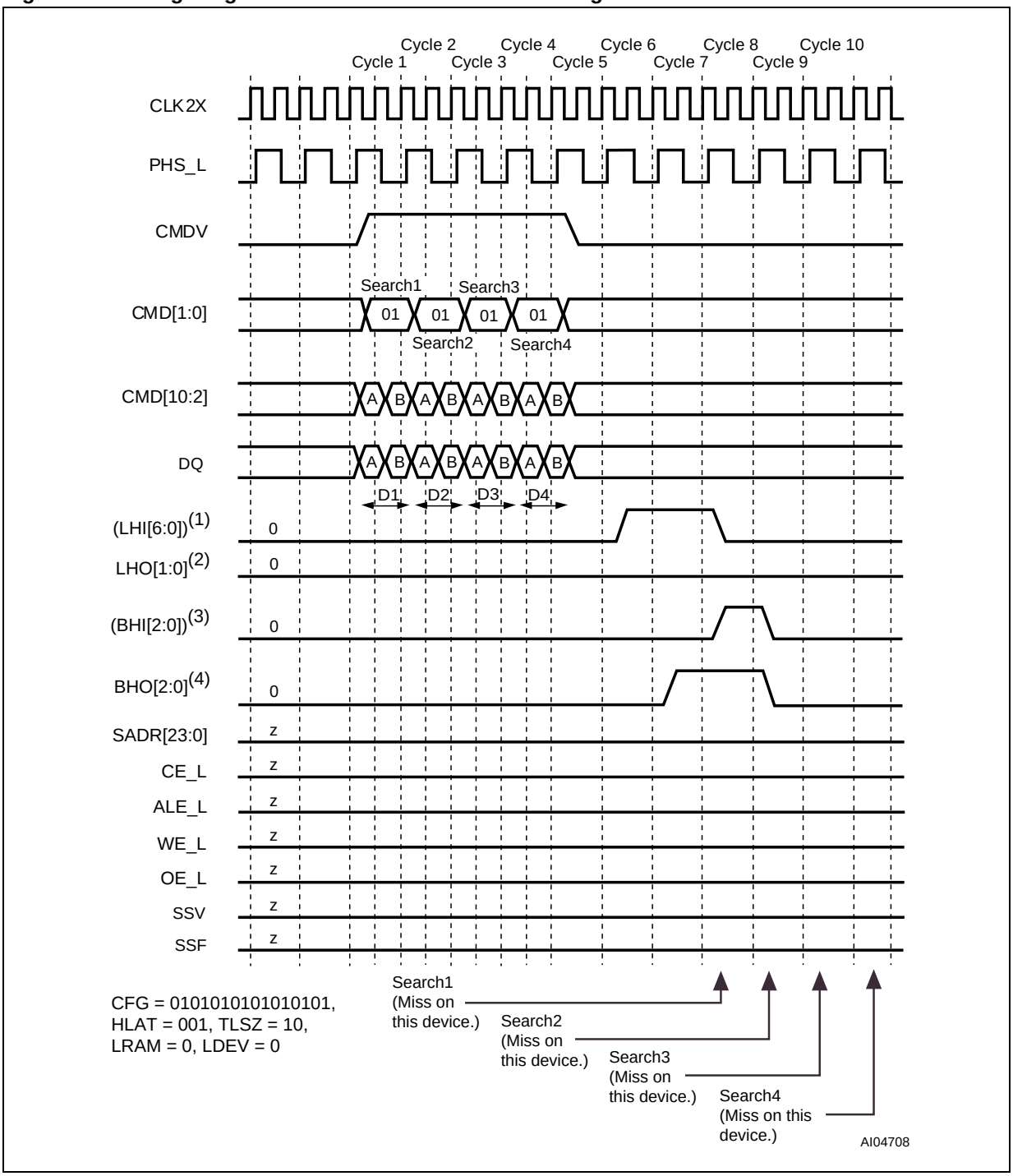
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 60. Timing Diagram for the Globally Winning Device in Block Number 2



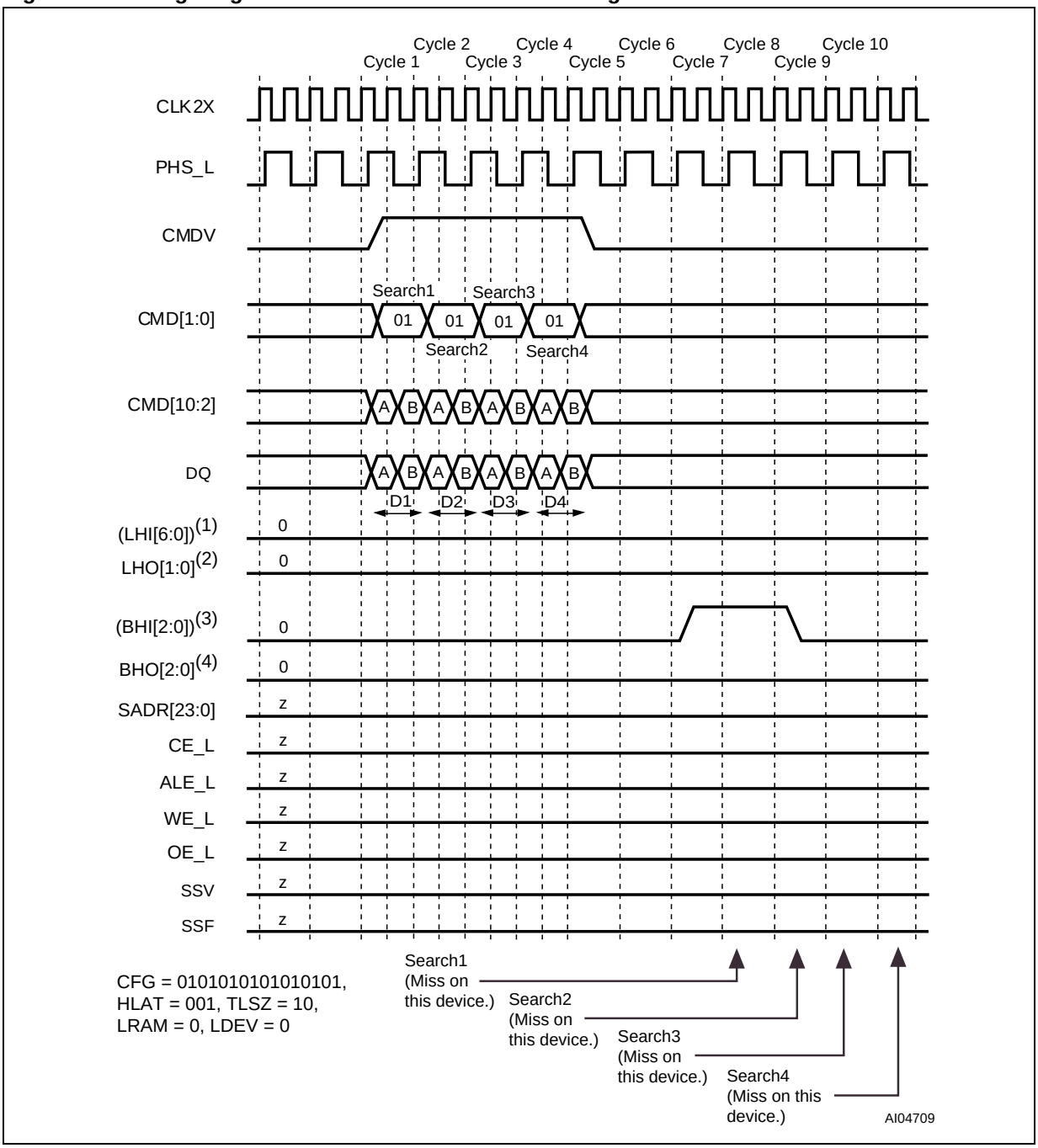
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 61. Timing Diagram for Devices Below the Winning Device in Block Number 2



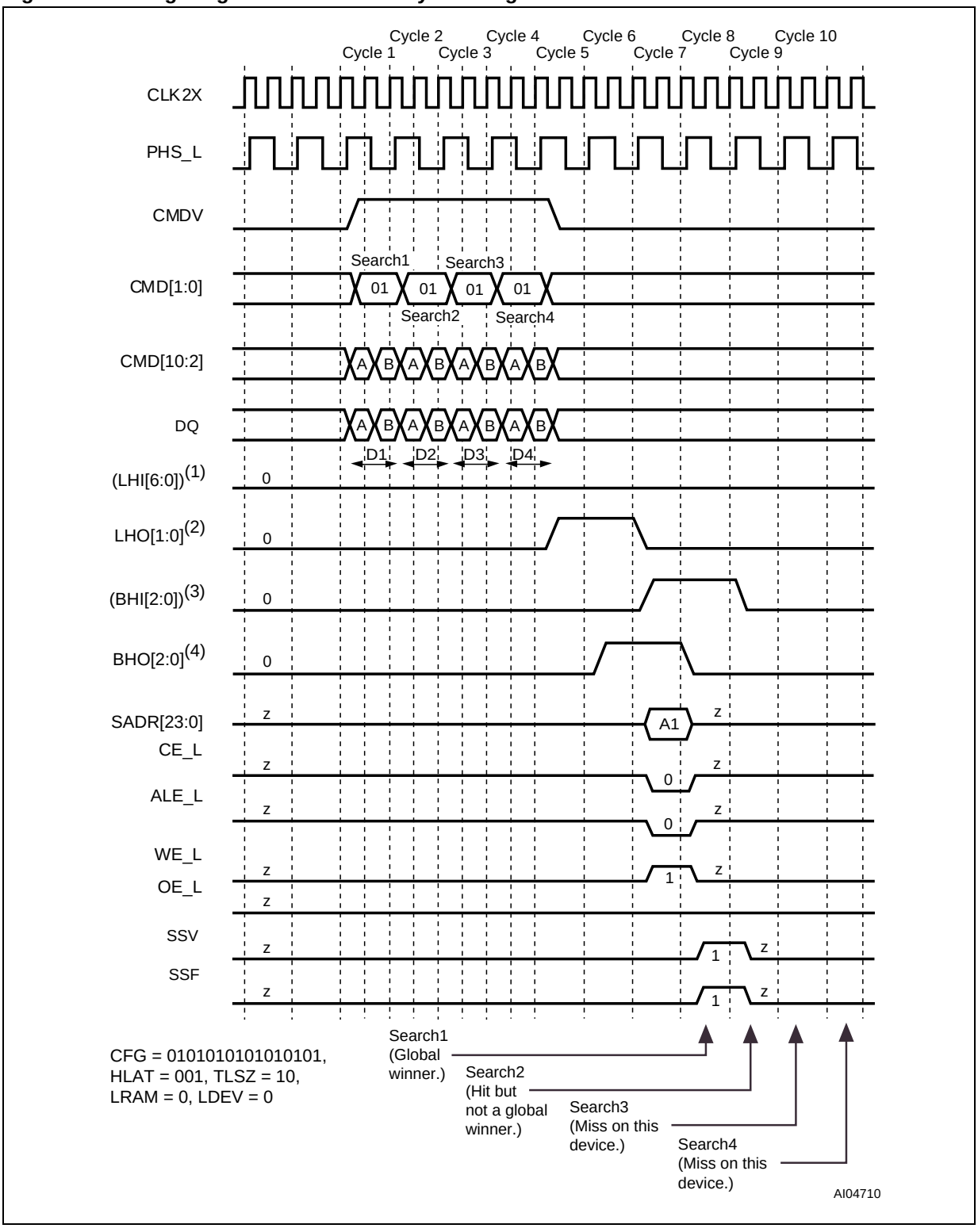
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 62. Timing Diagram for Devices Above the Winning Device in Block Number 3



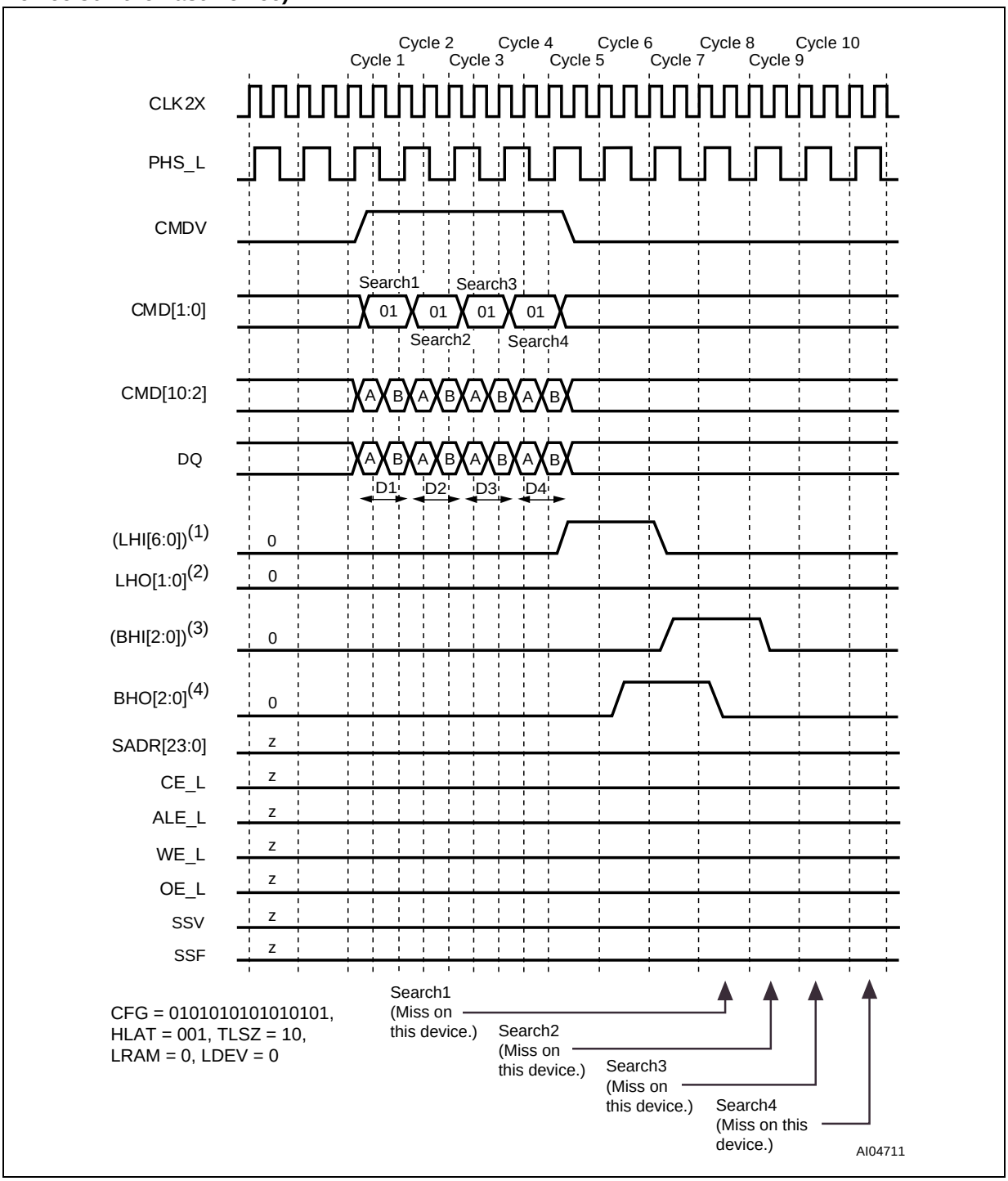
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 63. Timing Diagram for the Globally Winning Device in Block Number 3



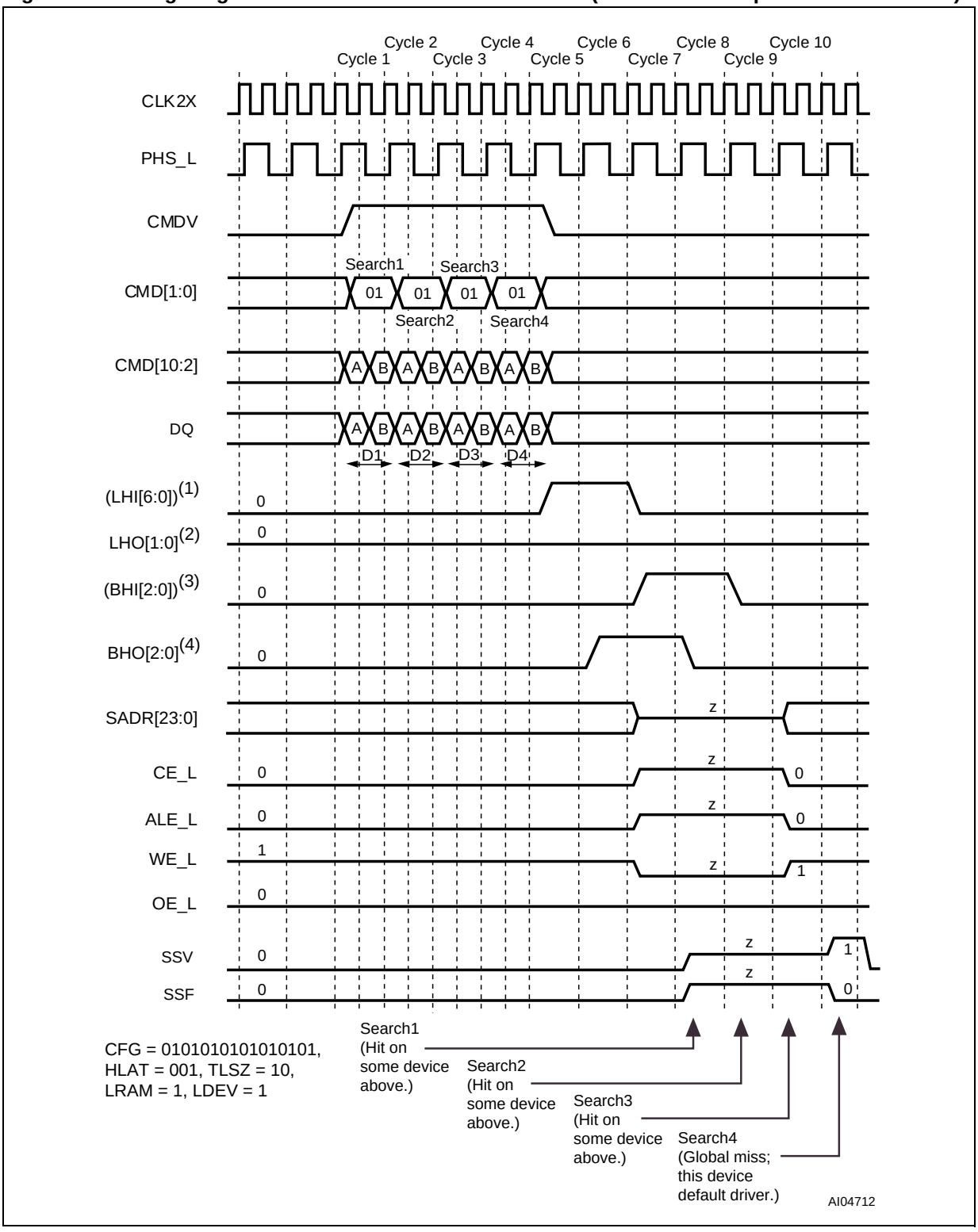
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 64. Timing Diagram for Devices Below the Winning Device in Block Number 3 (except Device 30 - the Last Device)



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 65. Timing Diagram for Device 6 in Block Number 3 (Device 30 in Depth-Cascaded Table)



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Table 40. Latency of SEARCH from Instruction to SRAM Access Cycle, 144-bit

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	32K x 144-bit	4
1–8 (TLSZ = 01)	256K x 144-bit	5
1–31 (TLSZ = 10)	992K x 144-bit	6

Table 41. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

288-bit SEARCH on Tables Configured as x288 Using a Single M7040N Device

The hardware diagram for this search subsystem is shown in Figure 66, page 91. Figure 67, page 92 shows the timing diagram for a SEARCH command in the 288-bit-configured table (CFG = 1010101010101010) consisting of a single device for one set of parameters: TLSZ = '00,' HLAT = '001,' LRAM = '1,' and LDEV = '1.'

The following is the sequence of operation for a single 144-bit SEARCH command (also refer to COMMAND CODES AND PARAMETERS, page 30).

– **Cycle A:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair used for bits [287:144] of the data being searched. DQ[71:0] must be driven with the 72-bit data ([287:216]) to be compared to all locations “0” in the four 72-bits-word page. The CMD[2] signal must be driven to logic “1.”

  Note: CMD[2] = 1 signals that the search is a x288-bit search. CMD[8:3] in this cycle is ignored.

– **Cycle B:** The host ASIC continues to drive the CMDV high and continues to apply the command code of SEARCH command ('10') on CMD[1:0]. The DQ[71:0] is driven with the 72-bit data ([215:144]) to be compared to all locations “1” in the four 72-bits-word page.

– **Cycle C:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair used for bits [143:0] of the data being searched. CMD[8:6] signals must be driven with the bits that will be driven on SADR[23:21] by this device if it has a hit. DQ[71:0] must be driven with the 72-bit data ([143:72]) to be compared to all locations “2” in the four 72-bits-word page. The CMD[2] signal must be driven to logic '0.'

– **Cycle D:** The host ASIC continues to drive the CMDV high and applies SEARCH command code ('10') on CMD[1:0]. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 24). The DQ[71:0] is driven with the 72-bit data ([71:0]) to be compared to all locations “3” in the four 72-bits-word page. CMD[5:2] is ignored because the LEARN Instruction is not supported for x288 tables.

  Note: For 288-bit searches, the host ASIC must supply four distinct 72-bit data words on DQ[71:0] during Cycles A, B, C, and D. The GMR Index in Cycle A selects a pair of GMRs that apply to DQ data in Cycles A and B. The GMR Index in Cycle C selects a pair of GMRs that apply to DQ data in Cycles C and D.

The logical 288-bit SEARCH operation is shown in Figure 68, page 93. The entire table of 288-bit entries is compared to a 288-bit word K that is presented on the DQ Bus in Cycles A, B, C, and D of the command using the GMR and local mask bits. The GMR is the 288-bit word specified by the two pairs of GMRs selected by the GMR Indexes in the command's Cycles A and C. The 288-bit word K that is presented on the DQ Bus in Cycles A, B, C, and D of the command is compared with each entry in the table starting at location "0." The first matching entry's location address, "L," is the winning address that is driven as part of the SRAM address on SADR[23:0] lines (see SRAM ADDRESSING, page 128).

Note: The matching address is always going to be location "0" in a four-entry page for a 288-bit SEARCH (two LSBs of the matching index will be '00').

The SEARCH command is a pipelined operation and executes at one-fourth the rate of the frequency of CLK2X for 288-bit searches in x288-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 288-bit SEARCH command (measured in CLK cycles) from the CLK2X cycle that contains the C and D Cycles is shown in Table 42, page 93.

The latency of a SEARCH from command to SRAM access cycle is 4 for only a single device in the table and TLSZ = 00. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in Table 43, page 93.

Figure 66. Hardware Diagram for a Table with One Device

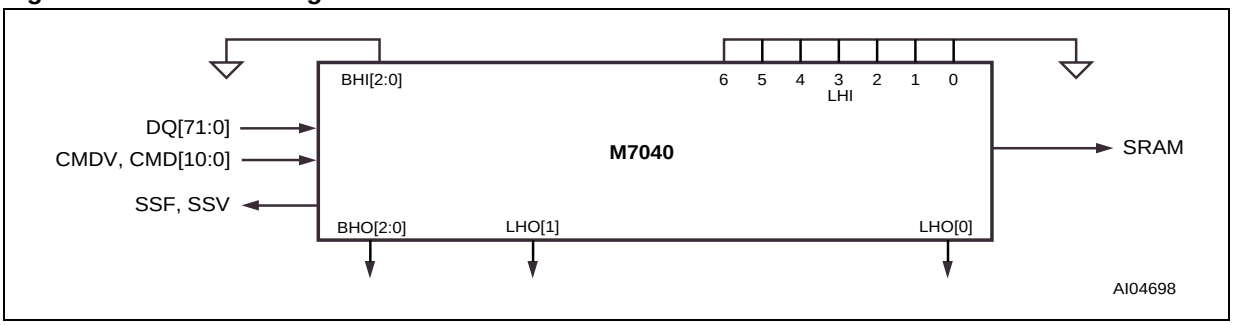


Figure 67. Timing Diagram for 288-bit SEARCH (One Device)

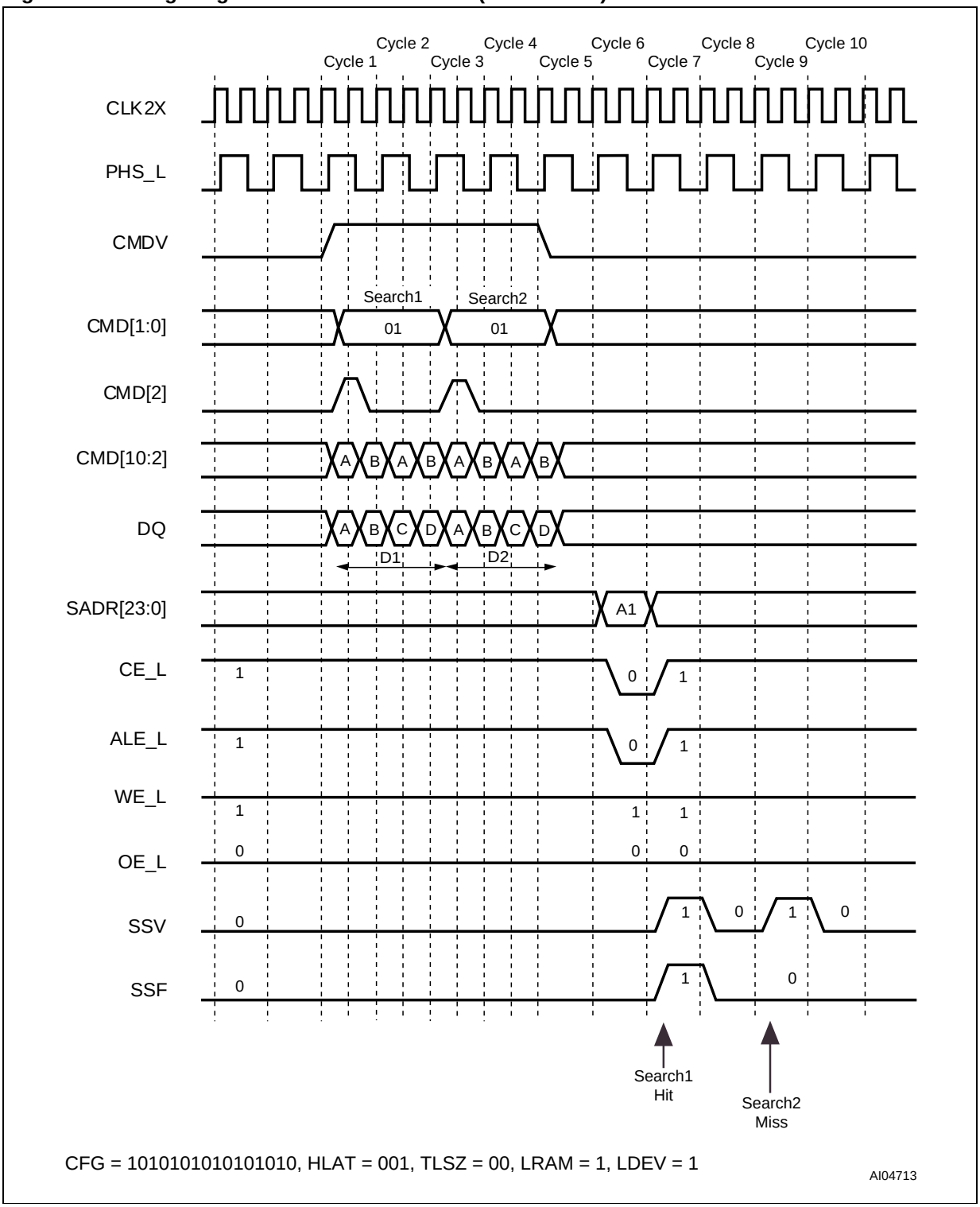


Figure 68. x288 Table with One Device

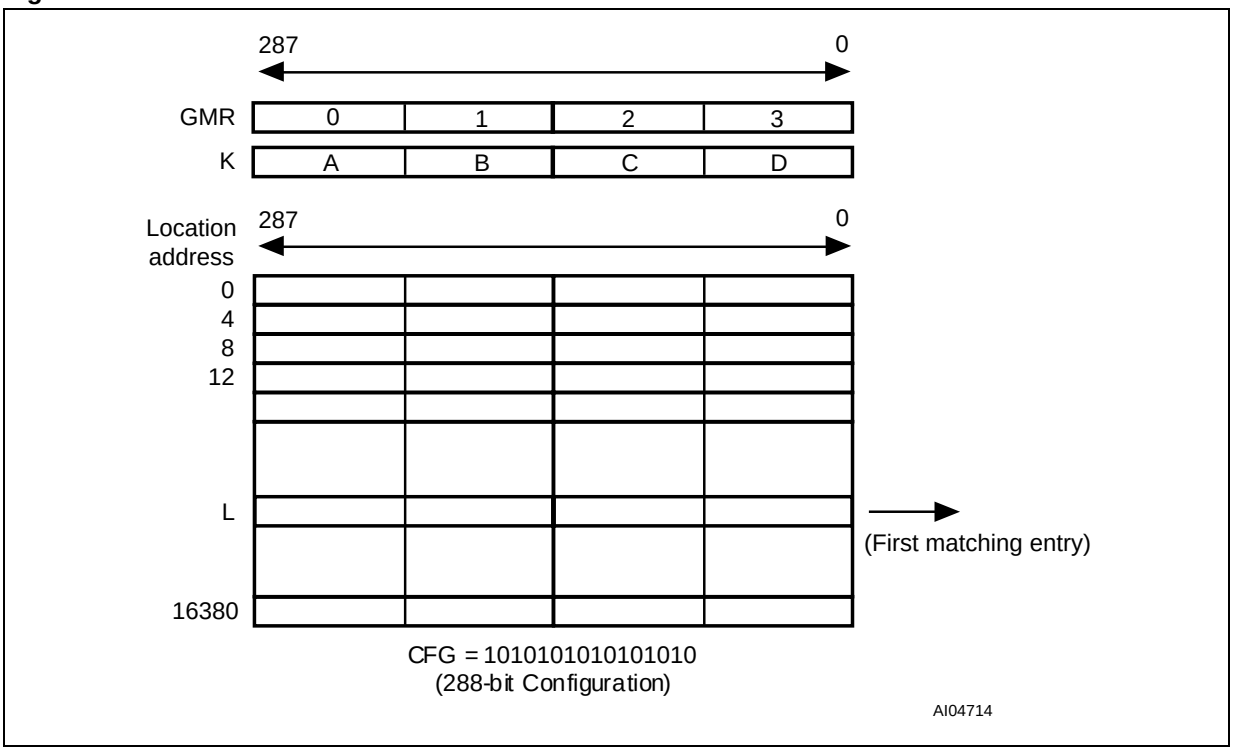


Table 42. Latency of SEARCH from Cycles C and D to SRAM Access Cycle

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	16K x 288-bit	4
2–8 (TLSZ = 01)	128K x 288-bit	5
2–31 (TLSZ = 10)	496K x 288-bit	6

Table 43. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

288-bit SEARCH on Tables x288-configured Using Up to Eight M7040N Devices

The hardware diagram of the search subsystem of eight devices is shown in Figure 69, page 96. The following are the parameters programmed in the eight devices.

– First seven devices (devices 0–6):
CFG = 1010101010101010, TLSZ = 01,
HLAT = 000, LRAM = 0, and LDEV = 0.

– Eighth device (device 7):
CFG = 1010101010101010, TLSZ = 01,
HLAT = 000, LRAM = 1, and LDEV = 1.

Note: All eight devices must be programmed with the same value of TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (Device 7 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (Devices 0 through 6 in this case).

Figure 71, page 98 shows the timing diagram for a SEARCH command in the 288-bit-configured table of eight devices for Device 0. Figure 72, page 99 shows the timing diagram for a SEARCH command in the 288-bit-configured table of eight devices for Device 1. Figure 73, page 100 shows the timing diagram for a SEARCH command in the 288-bit-configured table of eight devices for Device 7 (the last device in this specific table). For these timing diagrams three 288-bit searches are performed sequentially. The following HIT/MISS assumptions were made as shown in Table 44, page 95.

The following is the sequence of operation for a single 288-bit SEARCH command (also COMMAND CODES AND PARAMETERS, page 30).

– **Cycle A:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair used for bits [287:144] of the data being searched in this operation. DQ[71:0] must be driven with the 72-bit data ([287:216]) to be compared against all locations “0” in the four-word, 72-bit page. The CMD[2] signal must be driven to logic '1.'

  Note: CMD[2] = 1 signals that the search is a 288-bit search. CMD[8:3] in this cycle is ignored.

– **Cycle B:** The host ASIC continues to drive the CMDV high and applies SEARCH command code ('10') on CMD[1:0]. The DQ[71:0] is driven with the 72-bit data ([215:144]) to be compared against all locations “1” in the four 72-bits-word page.

– **Cycle C:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair used for bits [143:0] of the data being searched. CMD[8:6] signals must be driven with the bits that will be driven on SADR[23:21] by this device if it has a hit. DQ[71:0] must be driven with the 72-bit data ([143:72]) to be compared against all locations “2” in the four 72-bits-word page. The CMD[2] signal must be driven to logic '0.'

– **Cycle D:** The host ASIC continues to drive the CMDV high and applies SEARCH command code ('10') on CMD[1:0]. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 24). The DQ[71:0] is driven with the 72-bit data ([71:0]) to be compared to all locations “3” in the four 72-bits-word page. CMD[5:2] is ignored because the LEARN Instruction is not supported for x288 tables.

  Note: For 288-bit searches, the host ASIC must supply four distinct 72-bit data words on DQ[71:0] during Cycles A, B, C, and D. The GMR Index in Cycle A selects a pair of GMRs in each of the eight devices that apply to DQ data in Cycles A and B. The GMR Index in Cycle C selects a pair of GMRs in each of the eight devices that apply to DQ data in Cycles C and D.

The logical 288-bit SEARCH operation is shown in Figure 70, page 97. The entire table of 288-bit entries is compared to a 288-bit word K that is presented on the DQ Bus in Cycles A, B, C, and D of the command using the GMR and the local mask bits. The GMR is the 288-bit word specified by the two pairs of GMRs selected by the GMR Indexes in the command’s Cycles A and C in each of the eight devices. The 288-bit word K that is presented on the DQ Bus in Cycles A, B, C, and D of the command is compared to each entry in the table starting at location “0.” The first matching entry’s location address, “L,” is the winning address that is driven as part of the SRAM address on the SADR[23:0] lines (see SRAM ADDRESSING, page 128).

Note: The matching address is always going to be a location “0” in a four-entry page for 288-bit SEARCH (two LSBs of the matching index will be '00').

The SEARCH command is a pipelined operation and executes search at one-fourth the rate of the frequency of CLK2X for 288-bit searches in x288-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 288-bit SEARCH command (measured in CLK cycles) from the CLK2X cycle that contains the C and D Cycles is shown in Table 45, page 101.

The latency of search from command to SRAM access cycle is 5 for only a single device in the table and TLSZ = 01. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in Table 46, page 101.

Table 44. Hit/Miss Assumption

Search Number	1	2	3
Device 0	Hit	Miss	Miss
Device 1	Miss	Hit	Miss
Device 2-6	Miss	Miss	Miss
Device 7	Miss	Miss	Miss

Figure 69. Hardware Diagram for a Table with Eight Devices

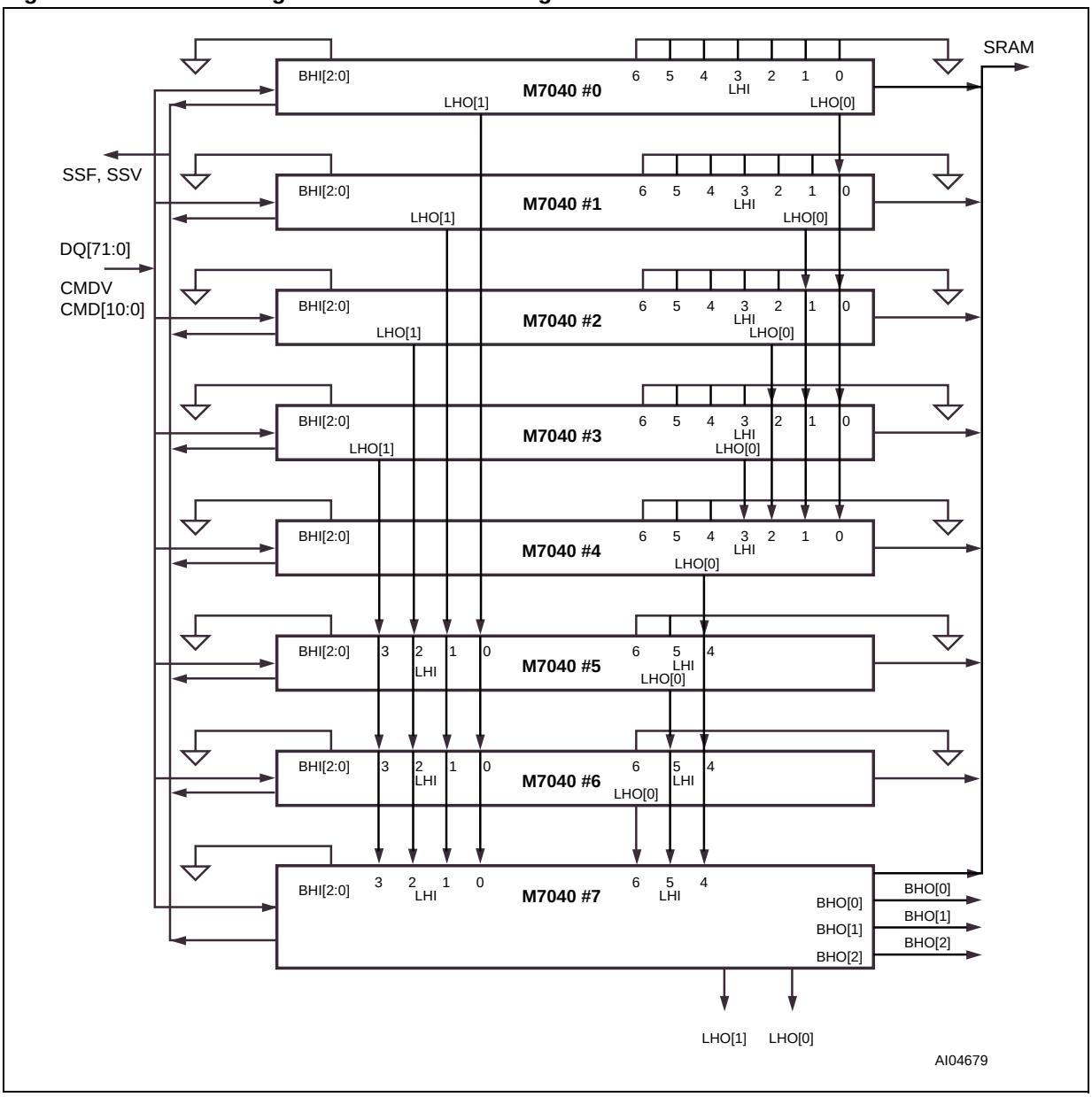
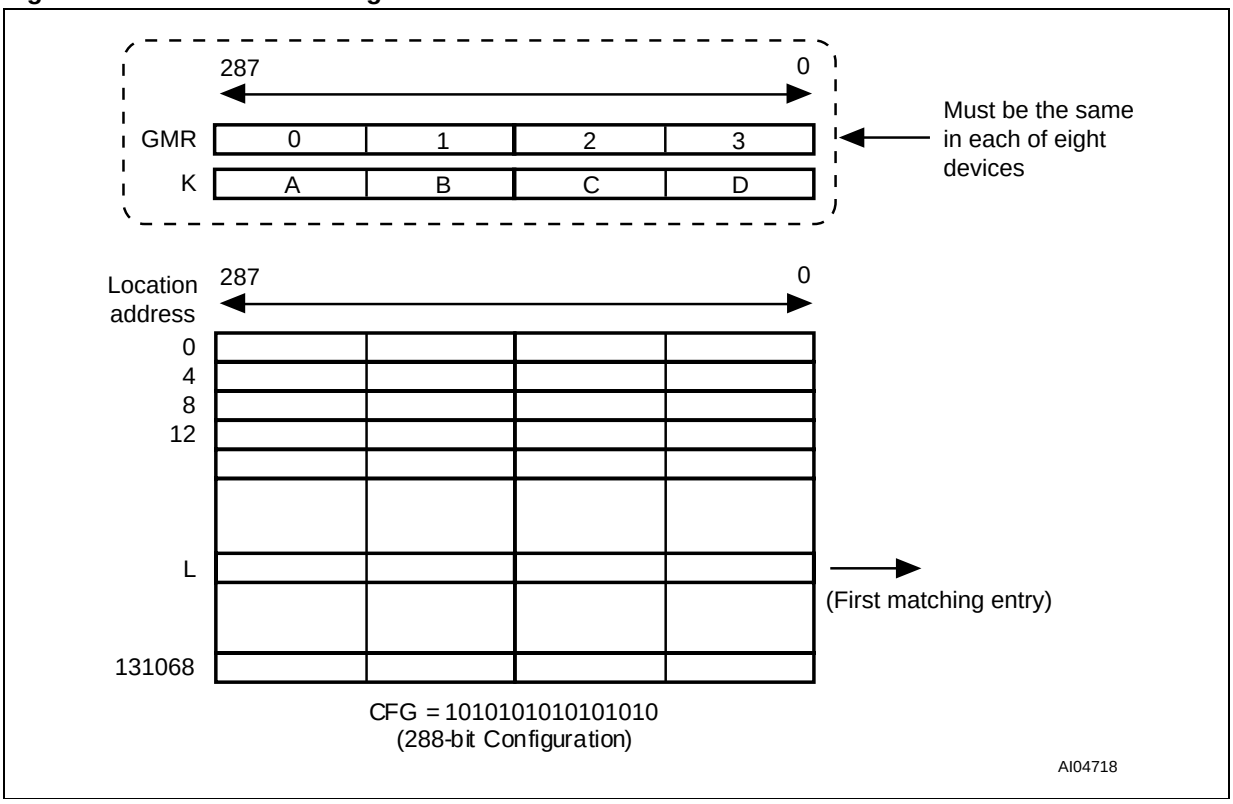
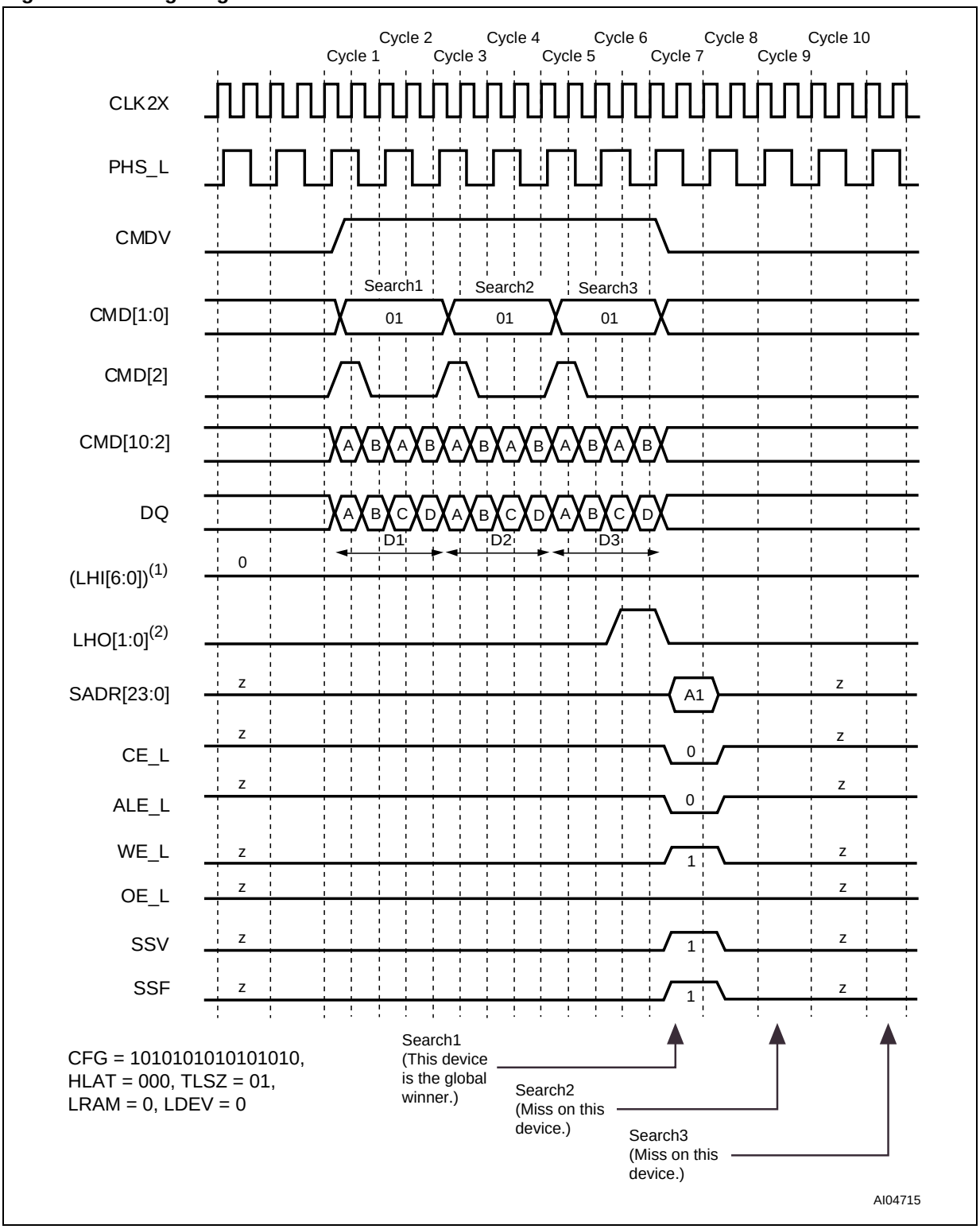


Figure 70. x288 Table with Eight Devices



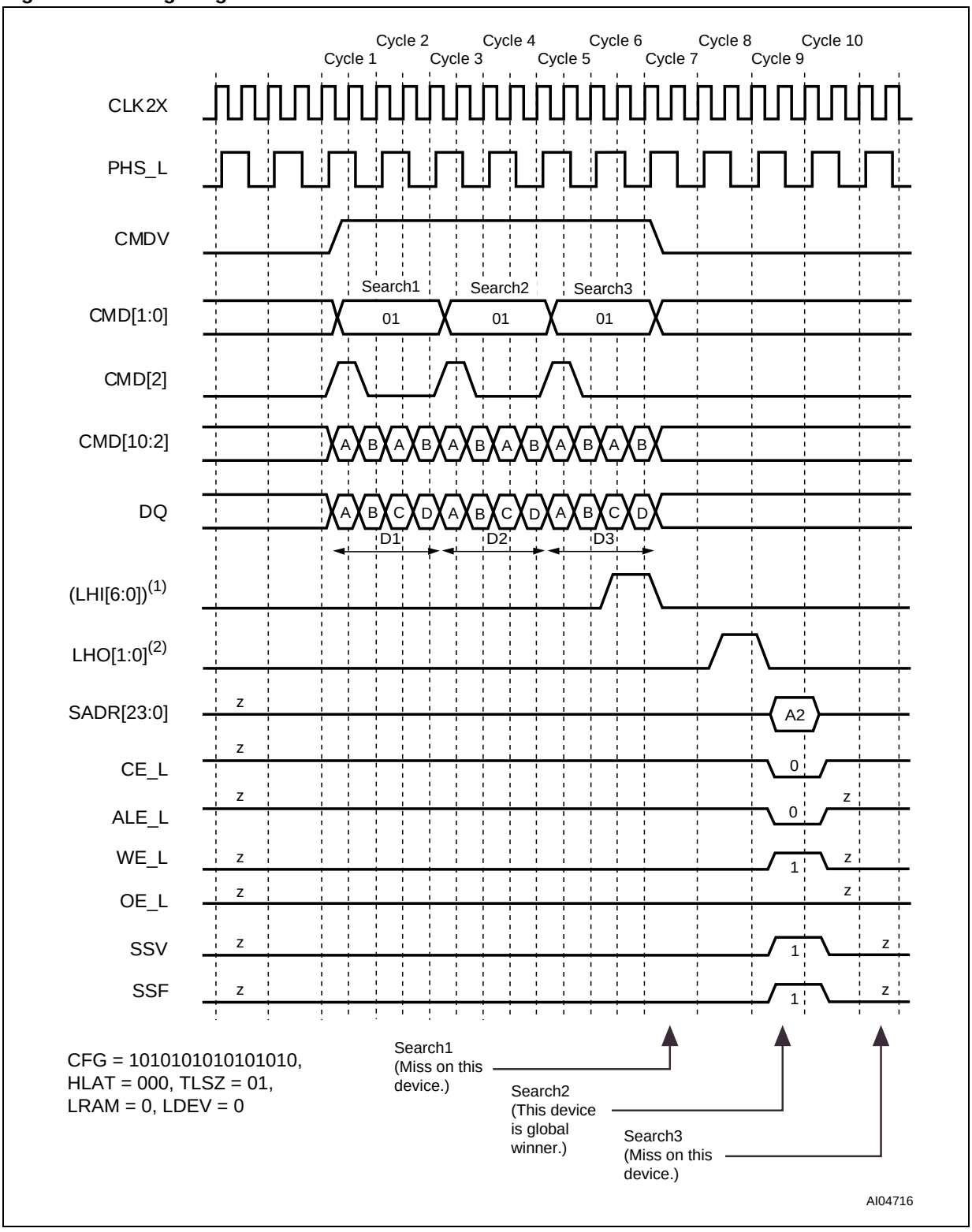
Timing Diagrams for x288-configured Using Up to Eight M7040N Devices

Figure 71. Timing Diagram for 288-bit SEARCH for Device Number 0



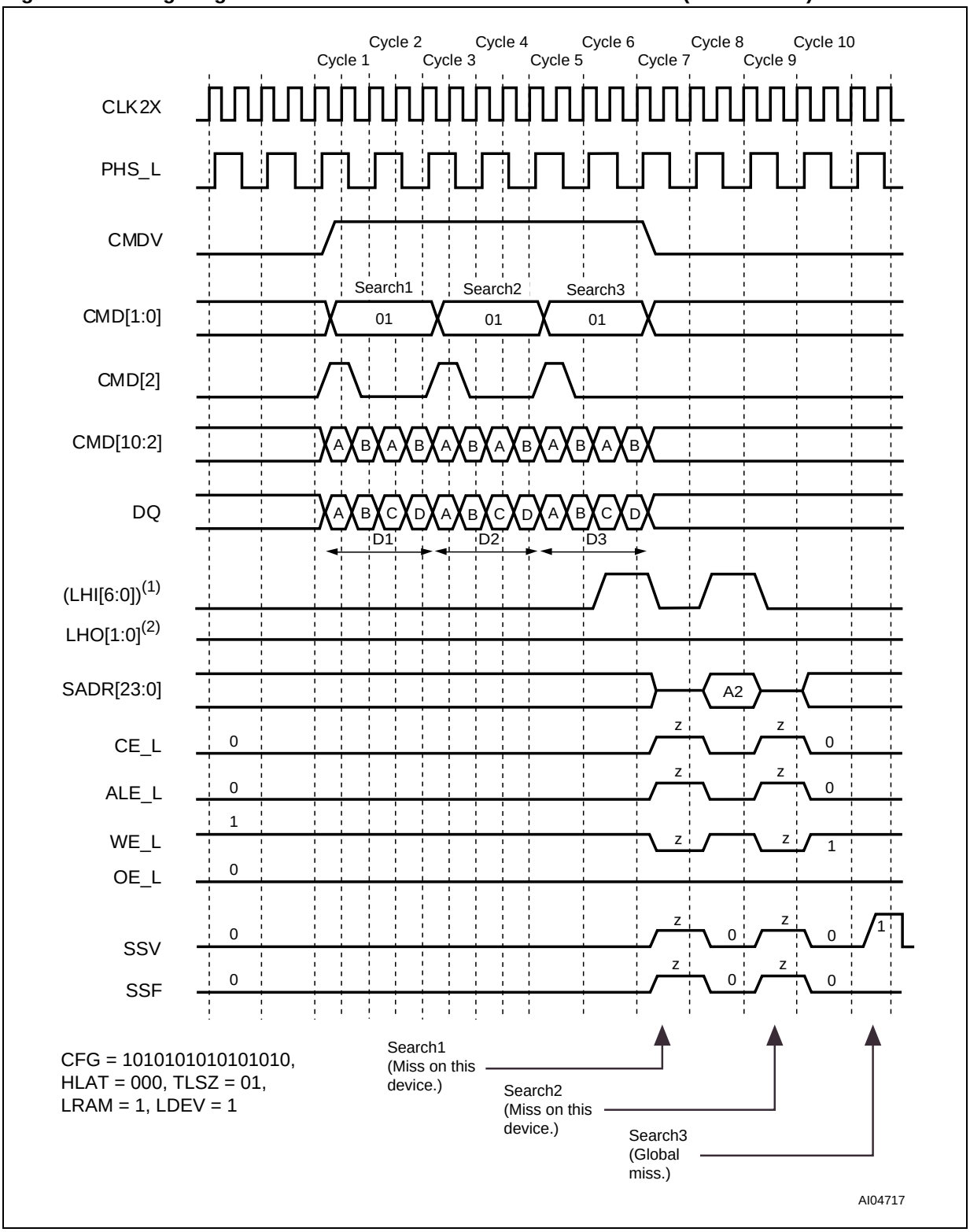
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.

Figure 72. Timing Diagram for 288-bit SEARCH for Device Number 1



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.

Figure 73. Timing Diagram for 288-bit SEARCH for Device Number 7 (Last Device)



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.

Table 45. Latency of SEARCH from Cycles C and D to SRAM Access Cycle, 288-bit

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	16K x 288-bit	4
1–8 (TLSZ = 01)	128K x 288-bit	5
1–31 (TLSZ = 10)	496K x 288-bit	6

Table 46. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

288-bit Search on Tables Configured as x288 Using Up to 31 M7040N Devices

The hardware diagram of the search subsystem of 31 devices is shown in Figure 74, page 103. Each of the four blocks in the diagram represents a block of eight M7040N devices, except the last which has seven devices.The diagram for a block of eight devices is shown in Figure 75, page 104. The following are the parameters programmed into the 31 devices.

– First thirty devices (devices 0–29):
CFG = 1010101010101010, TLSZ = 10,
HLAT = 000, LRAM = 0, and LDEV = 0.

– Thirty-first device (device 30):
CFG = 1010101010101010, TLSZ = 10,
HLAT = 000, LRAM = 1, and LDEV = 1.

Note: All 31 devices must be programmed with the same value of TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (Device 30 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (Devices 0 through 29 in this case).

The timing diagrams referred to in this paragraph reference the HIT/MISS assumptions defined in Table 47, page 103. For the purpose of illustrating the timings, it is further assumed that there is only one device with the matching entry in each block. Figure 77, page 106 shows the timing diagram for a SEARCH command in the 288-bit-configured table consisting of 31 devices for each of the eight devices in Block 0. Figure 78, page 107 shows the timing diagram for a SEARCH command in the 288-bit-configured table of 31 devices for all devices above the winning device in Block 1. Figure 79, page 108 shows the timing diagram for the globally winning device (the final winner within its own and all blocks) in Block 1. Figure 80, page 109 shows the timing diagram for all the devices below the globally winning device in Block 1. Figure 81, page 110, Figure 82, page 111, and Figure 83, page 112, respectively, show the timing diagrams of the devices above the globally winning device, the globally winning device, and the devices below the globally winning device for Block 2. Figure 84, page 113, Figure 85, page 114, Figure 86, page 115, and Figure 87, page 116, respectively, show the timing diagrams of the device above the globally winning device, the globally winning device, the devices below the globally winning device (except Device 30), and last device (Device 30) for Block 3.

The following is the sequence of operation for a single 288-bit SEARCH command (see COMMAND CODES AND PARAMETERS, page 30).

– **Cycle A:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair used for bits [287:144] of the data being searched. DQ[71:0] must be driven with the 72-bit data ([287:216])to be compared to all locations “0” in the four 72-bit-word page. The CMD[2] signal must be driven to logic '1.'

  Note: CMD[2] = 1 signals that the search is a x288-bit search. CMD[8:6] is ignored in this cycle.

– **Cycle B:** The host ASIC continues to drive the CMDV high and applies SEARCH command ('10') on CMD[1:0]. The DQ[71:0] is driven with the 72-bit data ([215:144]) to be compared to all locations '1' in the four 72-bits-word page.

– **Cycle C:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair used for the bits [143:0] of the data being searched. CMD[8:6] signals must be driven with the bits that will be driven by this device on SADR[23:21] if it has a hit. DQ[71:0] must be driven with the 72-bit data ([143:72]) to be compared to all locations “2” in the four 72-bit-word page. The CMD[2] signal must be driven to logic '0.'

– **Cycle D:** The host ASIC continues to drive the CMDV high and continues to apply SEARCH command code ('10') on CMD[1:0]. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 24). The DQ[71:0] is driven with the 72-bit data ([71:0]) to be compared to all locations “3” in the four 72-bit-word page. CMD[5:2] is ignored because the LEARN Instruction is not supported for x288 tables.

  Note: For 288-bit searches, the host ASIC must supply four distinct 72-bit data words on DQ[71:0] during Cycles A, B, C, and D. The GMR Index in Cycle A selects a pair of GMRs in each of the 31 devices that apply to DQ data in Cycles A and B. The GMR Index in Cycle C selects a pair of GMRs in each of the 31 devices that apply to DQ data in Cycles C and D.

The logical 288-bit SEARCH operation is as shown in Figure 76, page 105. The entire table of 288-bit entries is compared to a 288-bit word K that is presented on the DQ Bus in Cycles A, B, C, and D of the command using the GMR and local mask bits. The GMR is the 288-bit word specified by the two pairs of GMRs selected by the GMR Indexes in the command’s Cycles A and C in each of the 31 devices. The 288-bit word K that is presented on the DQ Bus in Cycles A, B, C, and D of the command is compared to each entry in the table starting at location “0.” The first matching entry’s location address, “L,” is the winning address that is driven as part of the SRAM address on the SADR[23:0] lines (see SRAM ADDRESSING, page 128).

Note: The matching address is always going to be location “0” in a four-entry page for 288-bit search (two LSBs of the matching index will be '00').

The SEARCH command is a pipelined operation and executes a search at one-fourth the rate of the frequency of CLK2X for 288-bit searches in x288-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 288-bit SEARCH command (measured in CLK cycles) from the CLK2X cycle that contains Cycles C and D shown in Table 48, page 117.

The latency of a SEARCH from command to SRAM access cycle is 6 for only a single device in the table and TLSZ = 10. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in Table 49, page 117

The 288-bit SEARCH operation is pipelined and executes as follows:

– Four cycles from the last cycle of the SEARCH command each of the devices knows the outcome internal to it for that operation.

– In the fifth cycle from the SEARCH command, the devices in a block (which is less than or equal to eight devices resolving the winner within them using an LHI[6:0] and LHO[1:0] signalling mechanism) arbitrate for a winner.

– In the sixth cycle after the SEARCH command, the blocks of devices resolve the winning block through a BHI[2:0] and BHO[2:0] signalling mechanism. The winning device within the winning block is the global winning device for the SEARCH operation.

Table 47. Hit/Miss Assumption

Search Number	1	2	3
Block 0	Miss	Miss	Miss
Block 1	Miss	Miss	Hit
Block 2	Miss	Hit	Hit
Block 3	Hit	Hit	Miss

Figure 74. Hardware Diagram for a Table with 31 Devices

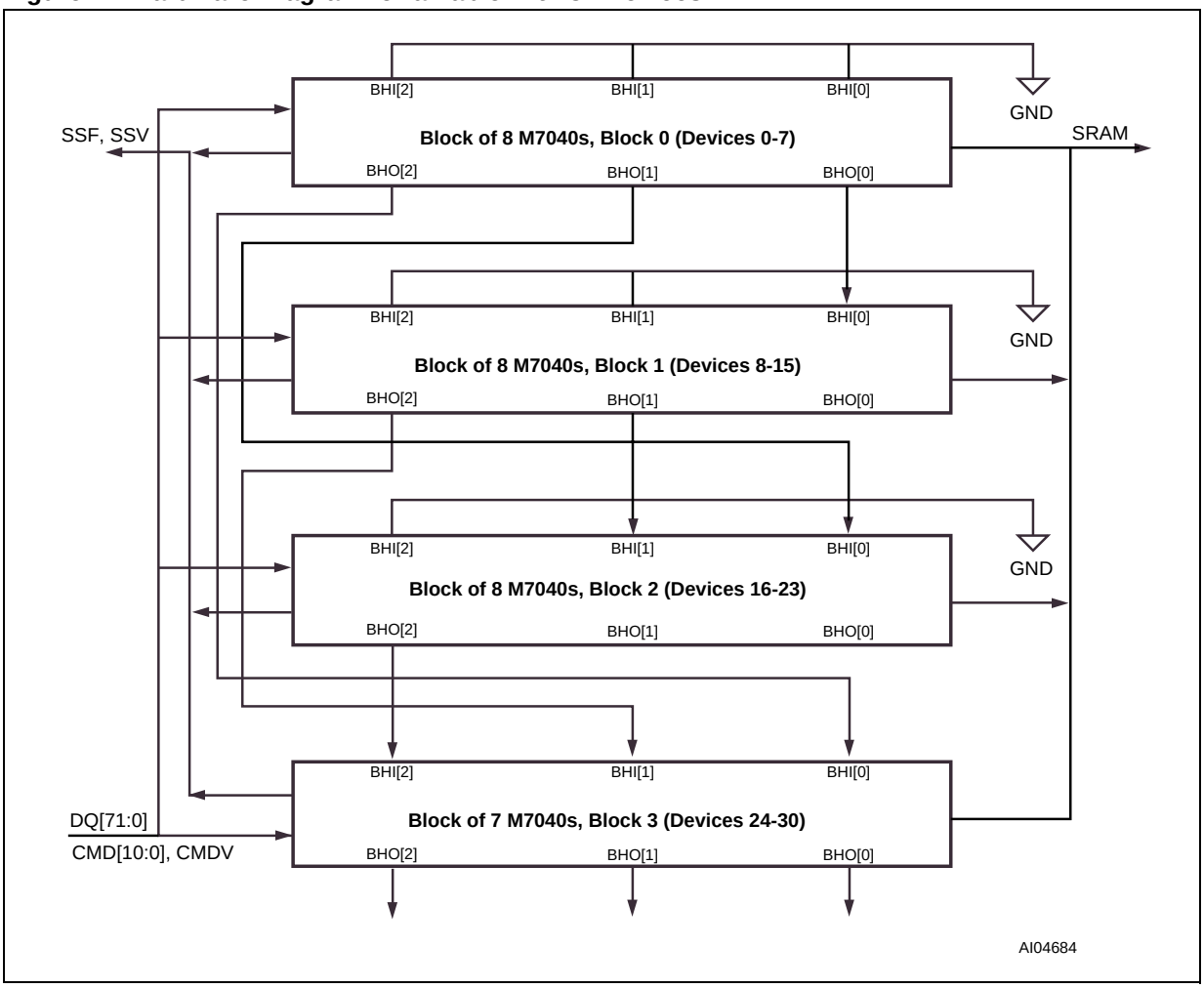


Figure 75. Hardware Diagram for a Block of Up to Eight Devices

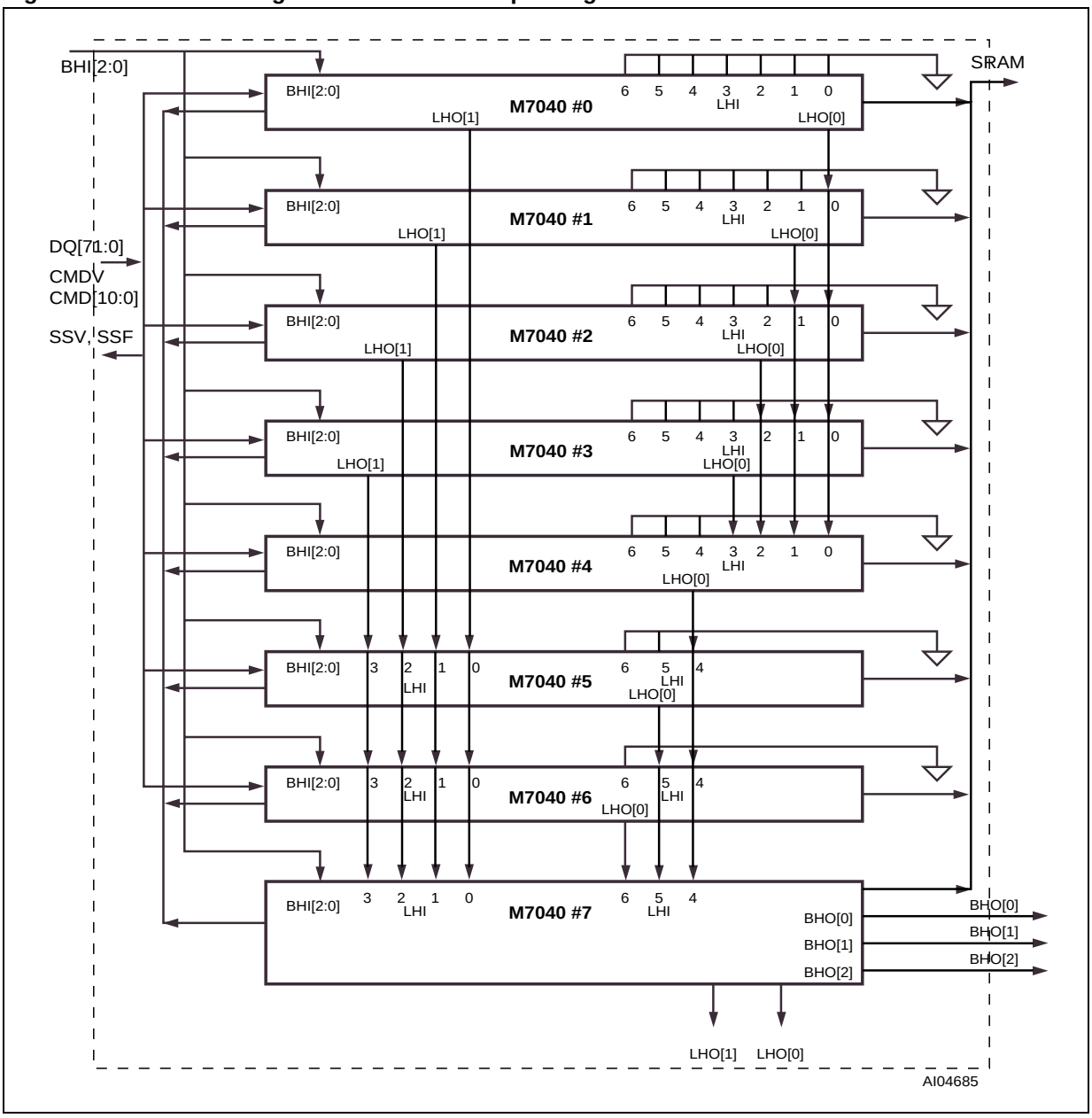
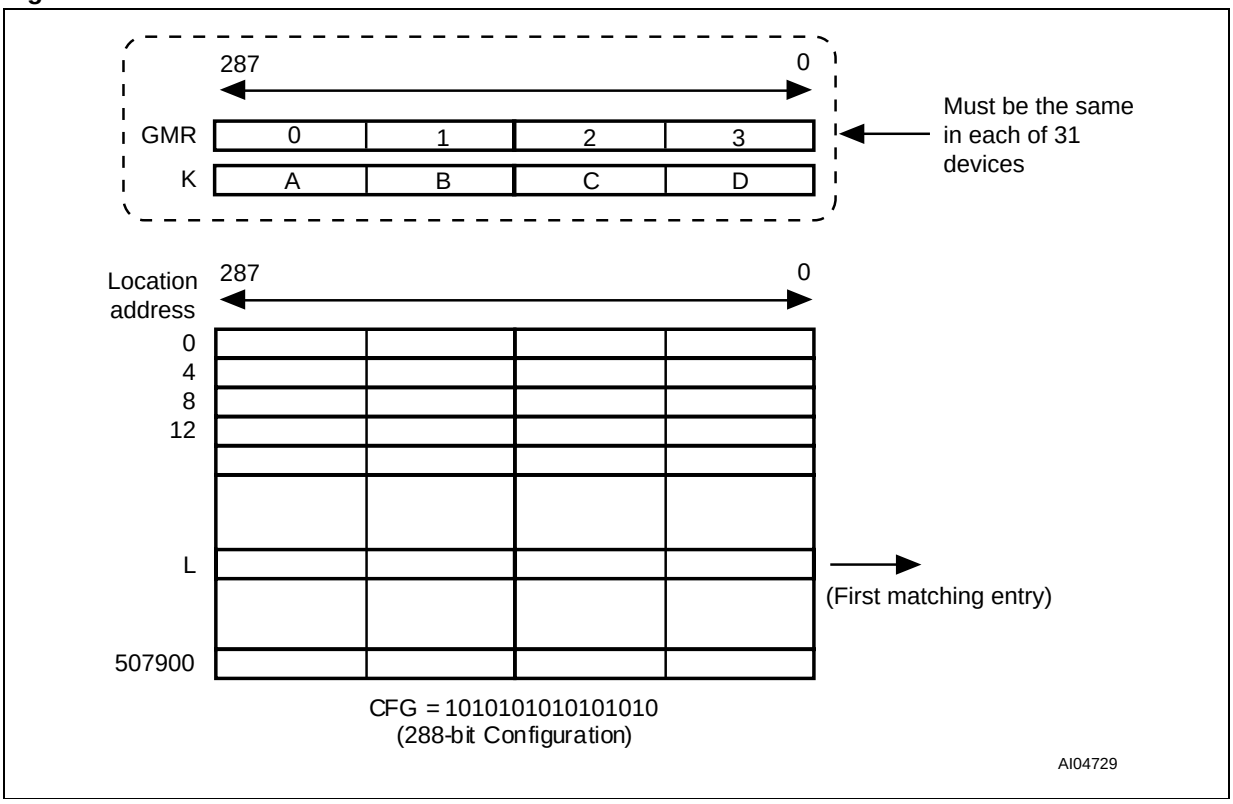
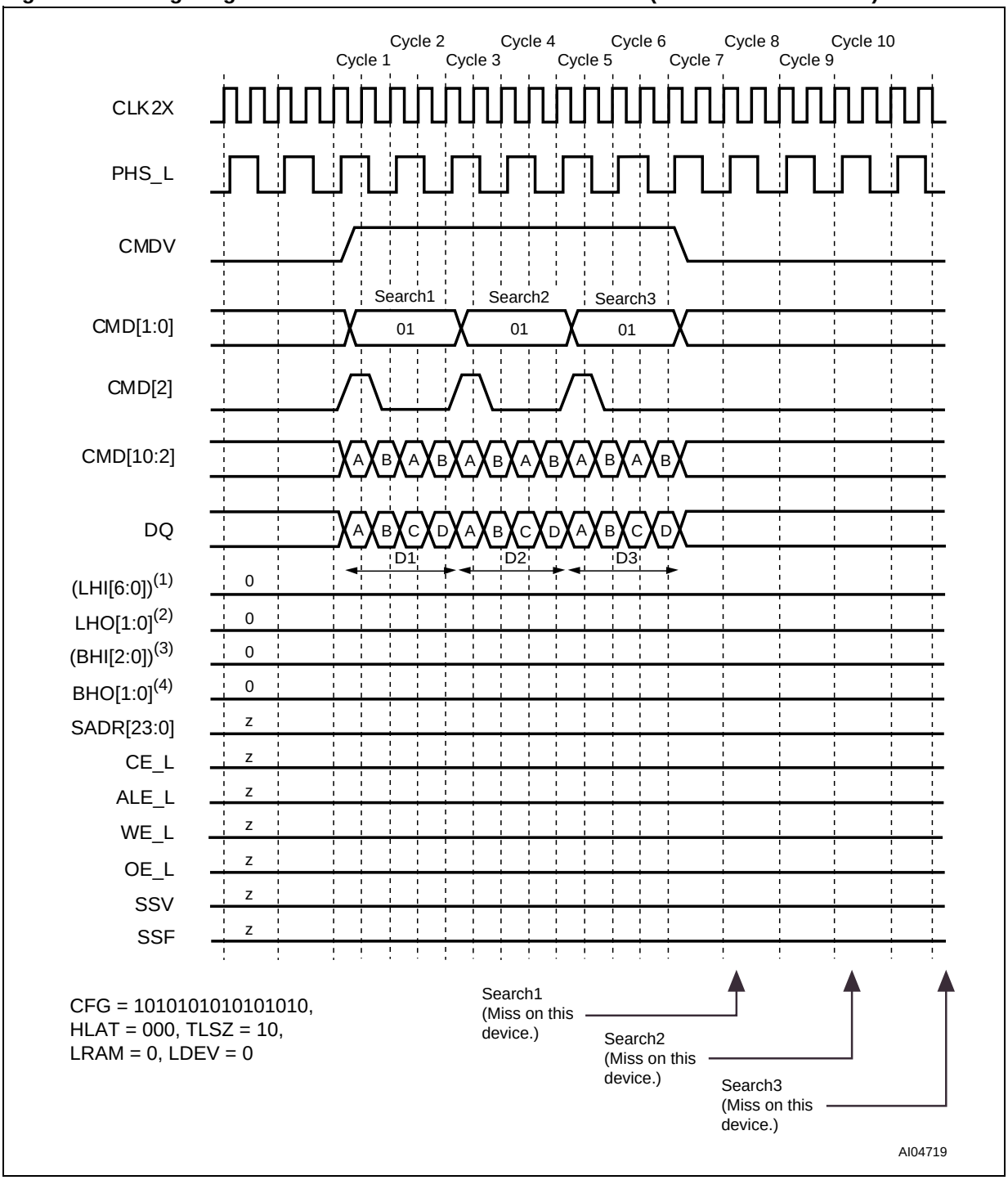


Figure 76. x288 Table with 31 Devices



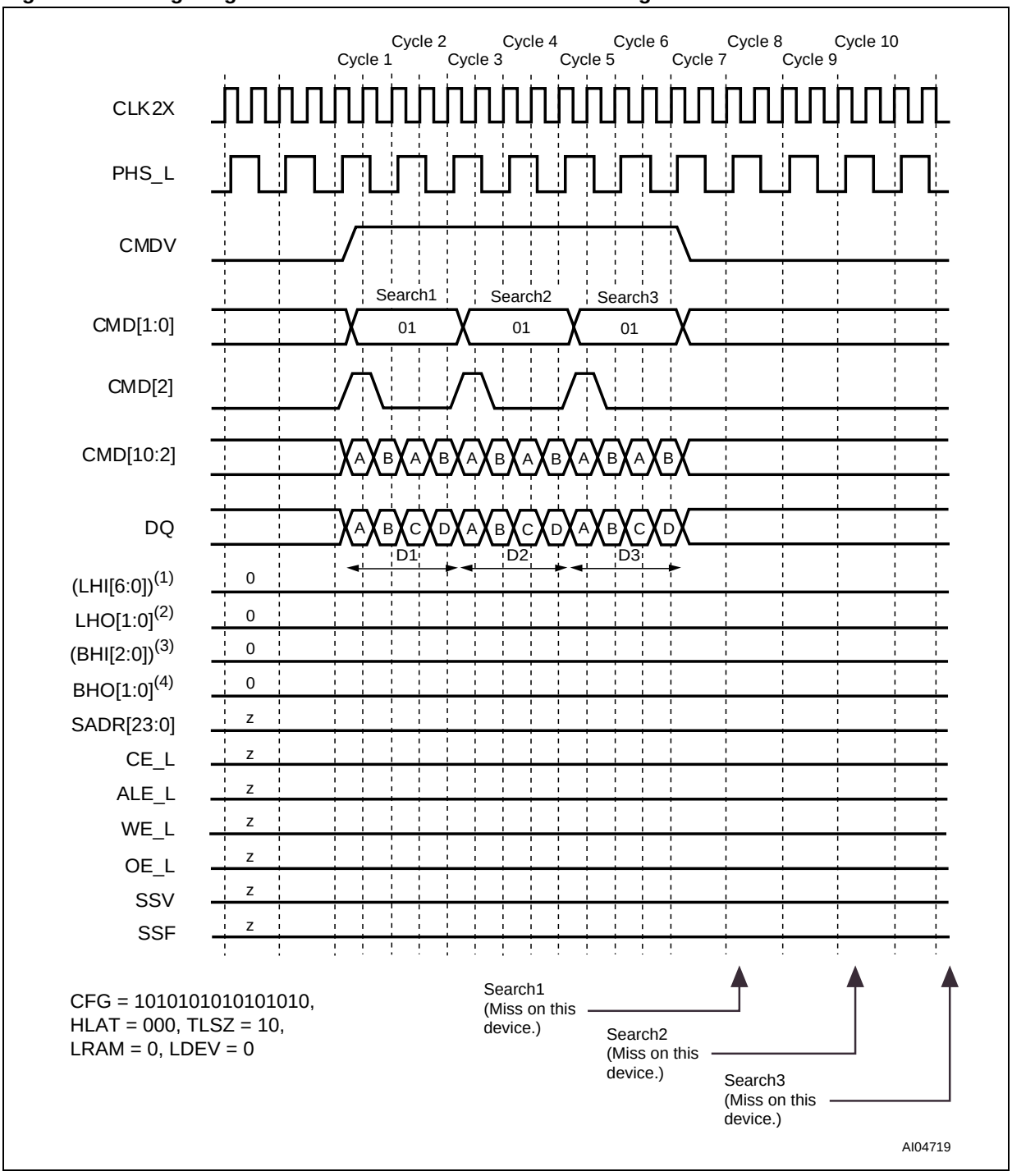
Timing Diagrams for x288 Using Up to 31 M7040N Devices

Figure 77. Timing Diagram for Each Device in Block Number 0 (Miss on Each Device)



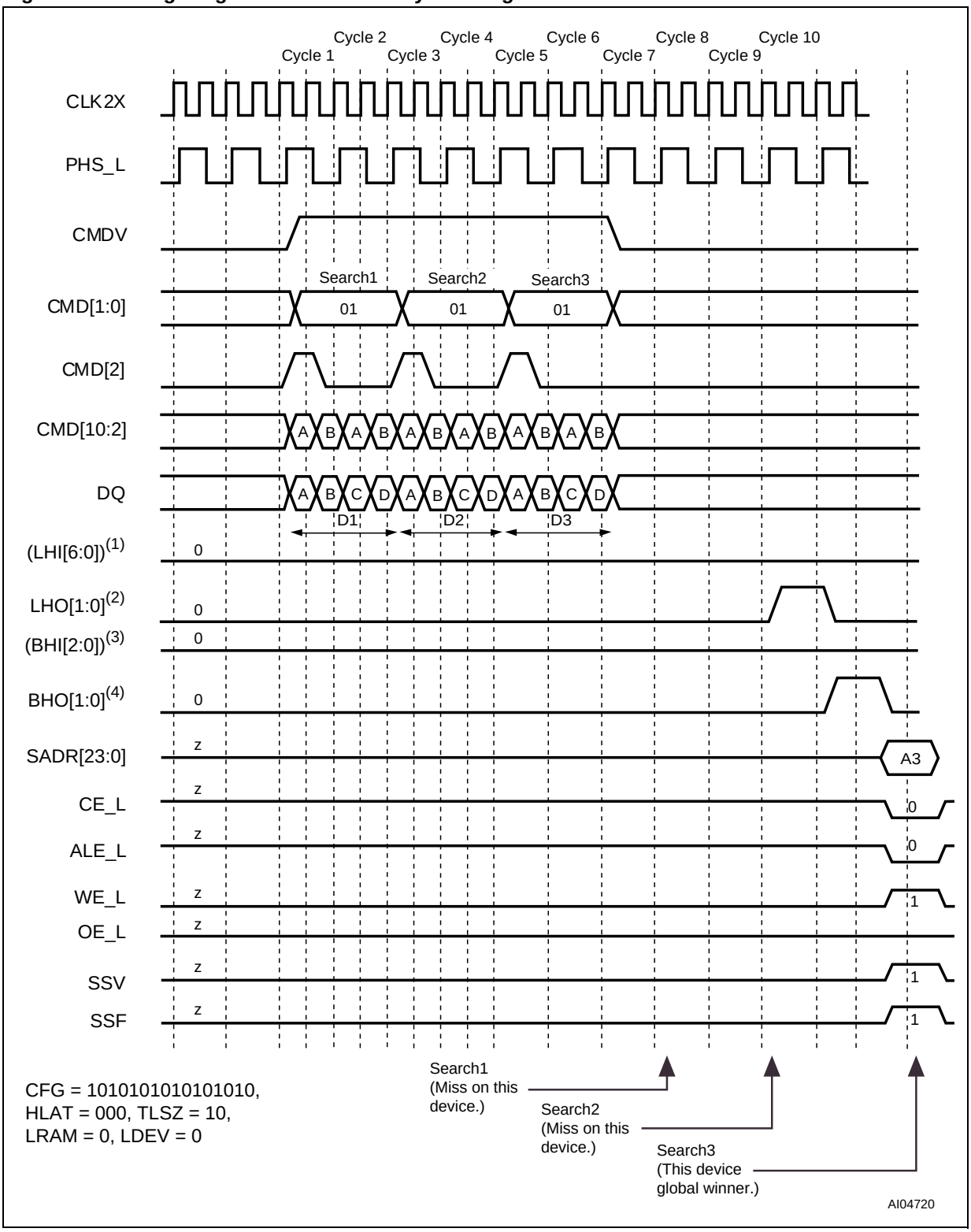
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 78. Timing Diagram for Each Device Above the Winning Device in Block Number 1



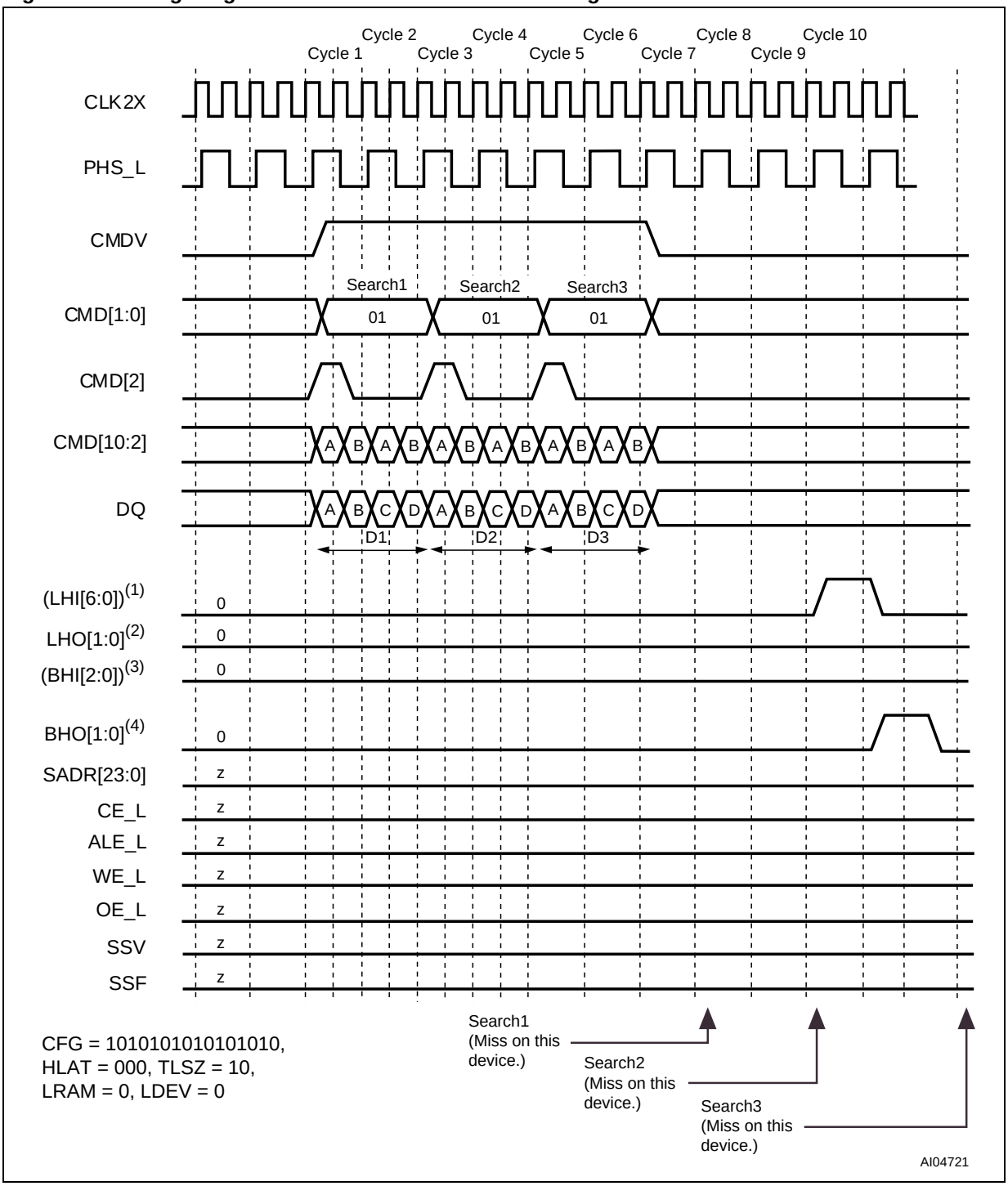
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 79. Timing Diagram for the Globally Winning Device in Block Number 1



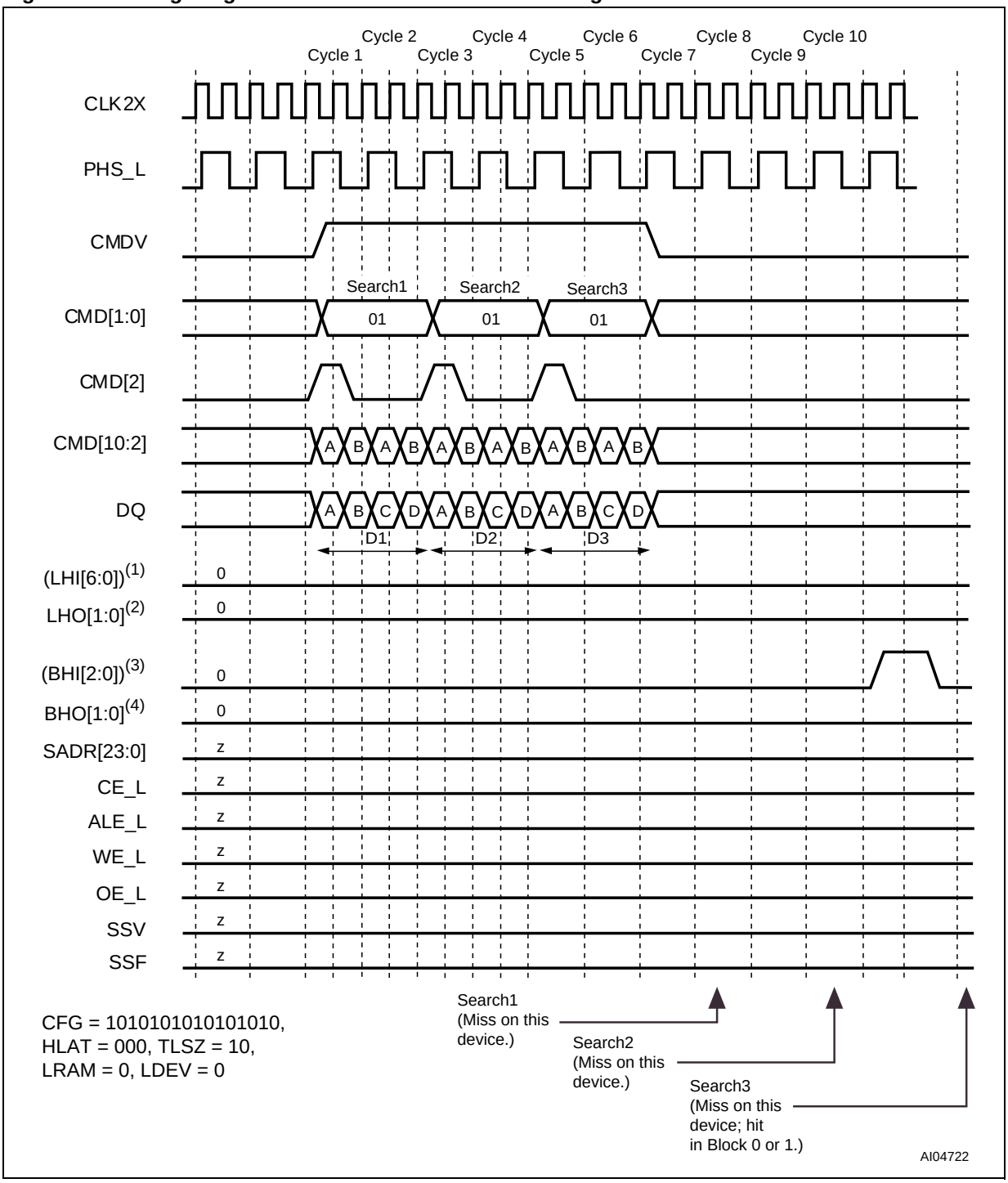
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 80. Timing Diagram for Devices Below the Winning Device in Block Number 1



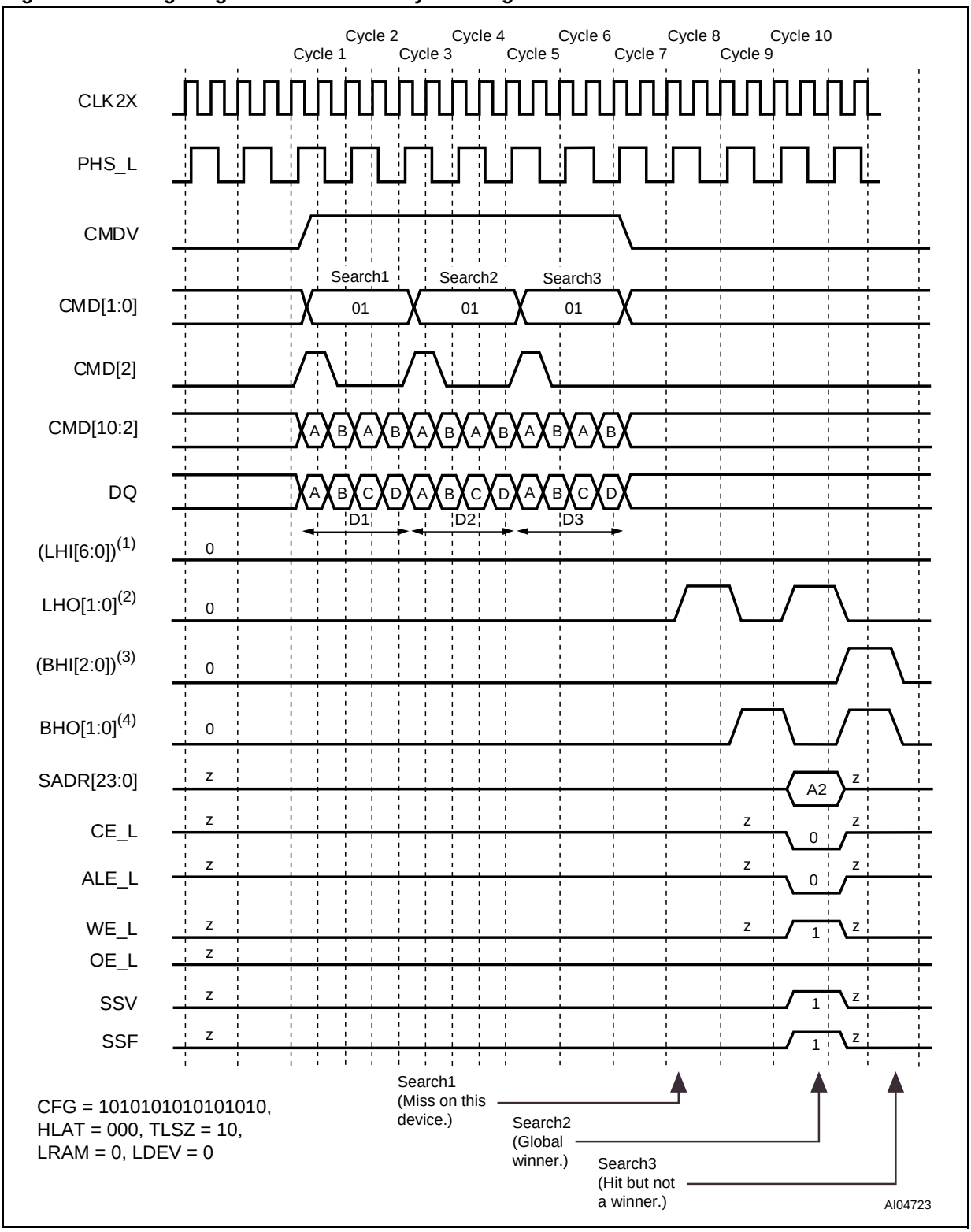
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 81. Timing Diagram for Devices Above the Winning Device in Block Number 2



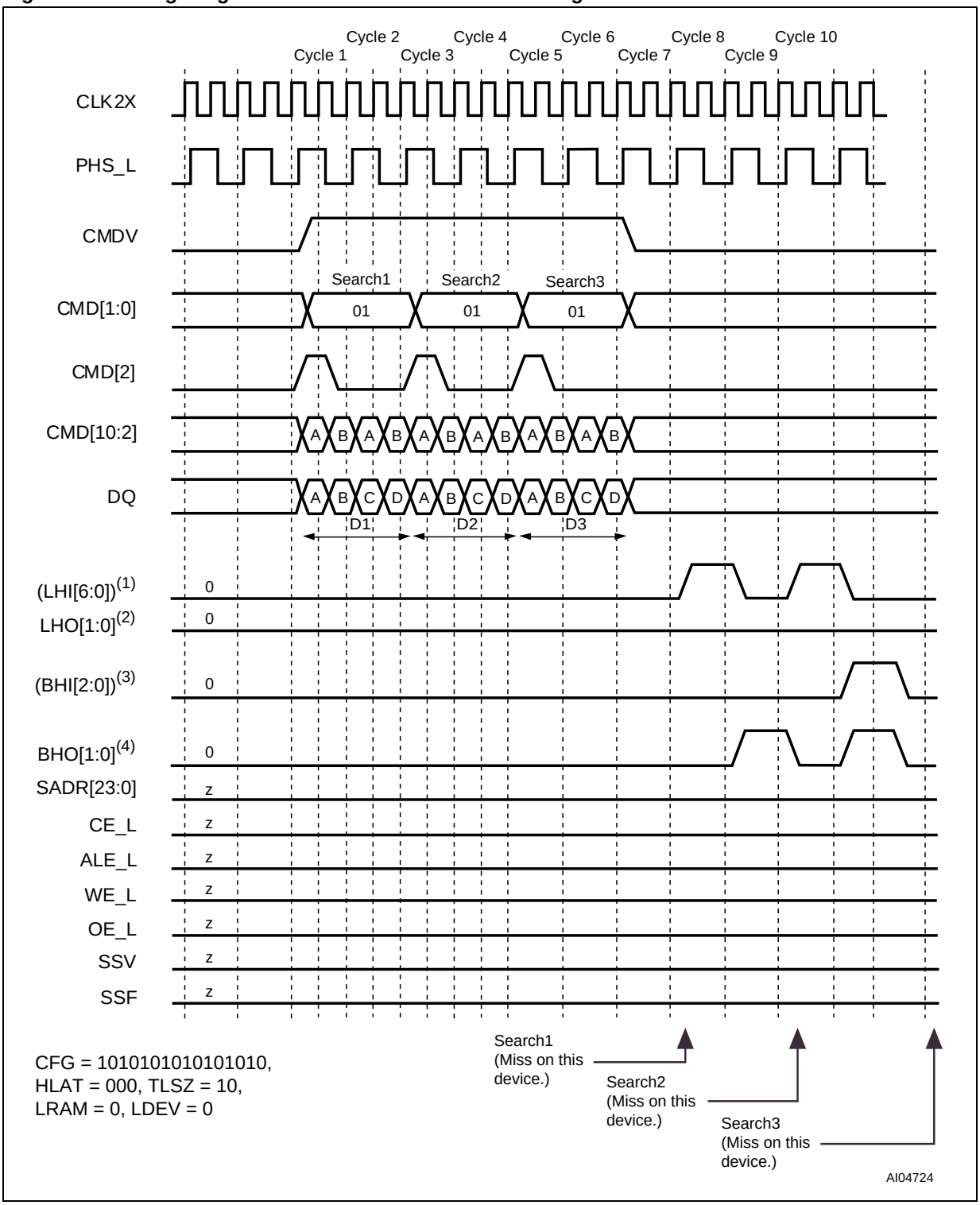
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 82. Timing Diagram for the Globally Winning Device in Block Number 2



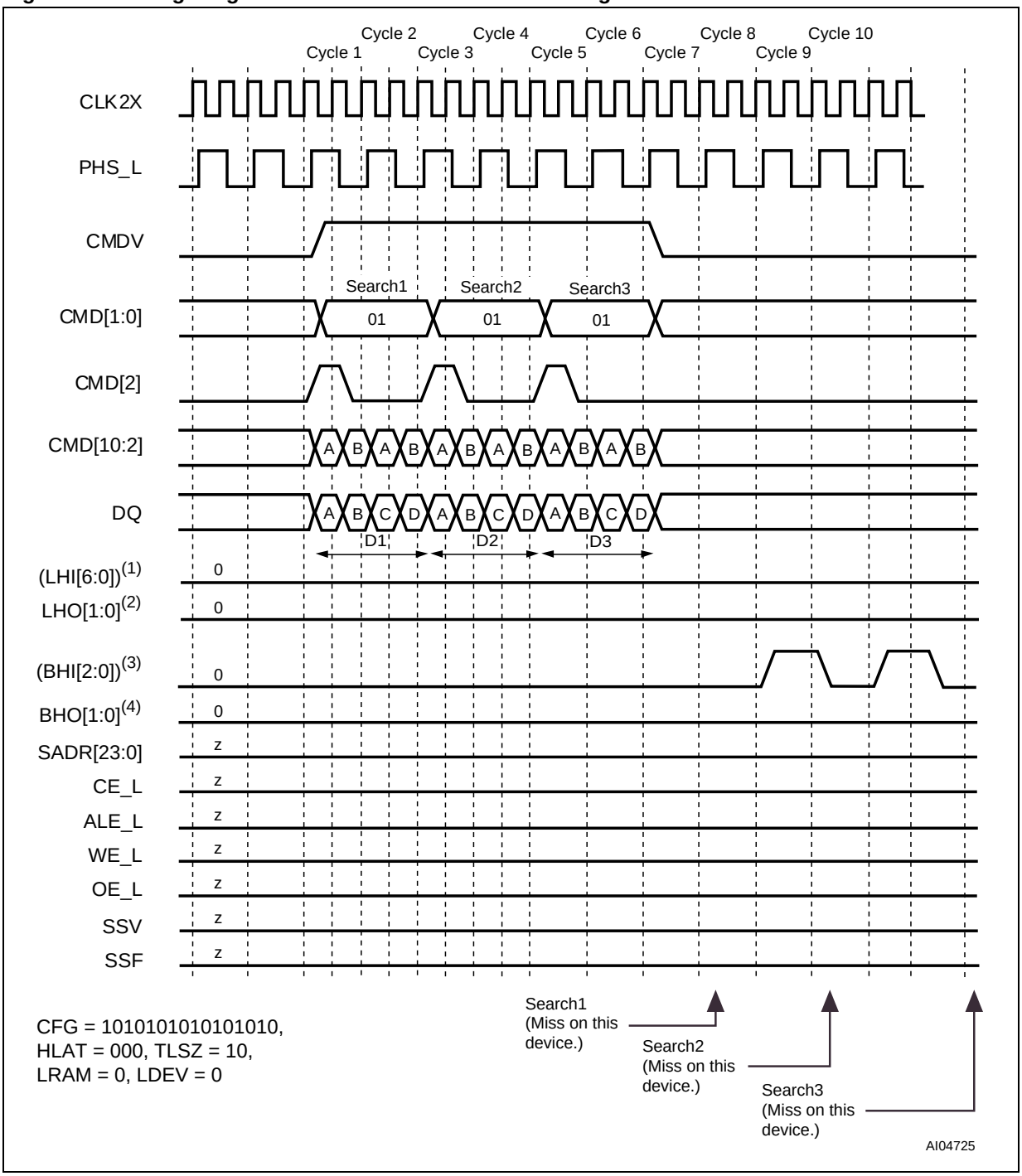
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 83. Timing Diagram for Devices Below the Winning Device in Block Number 2



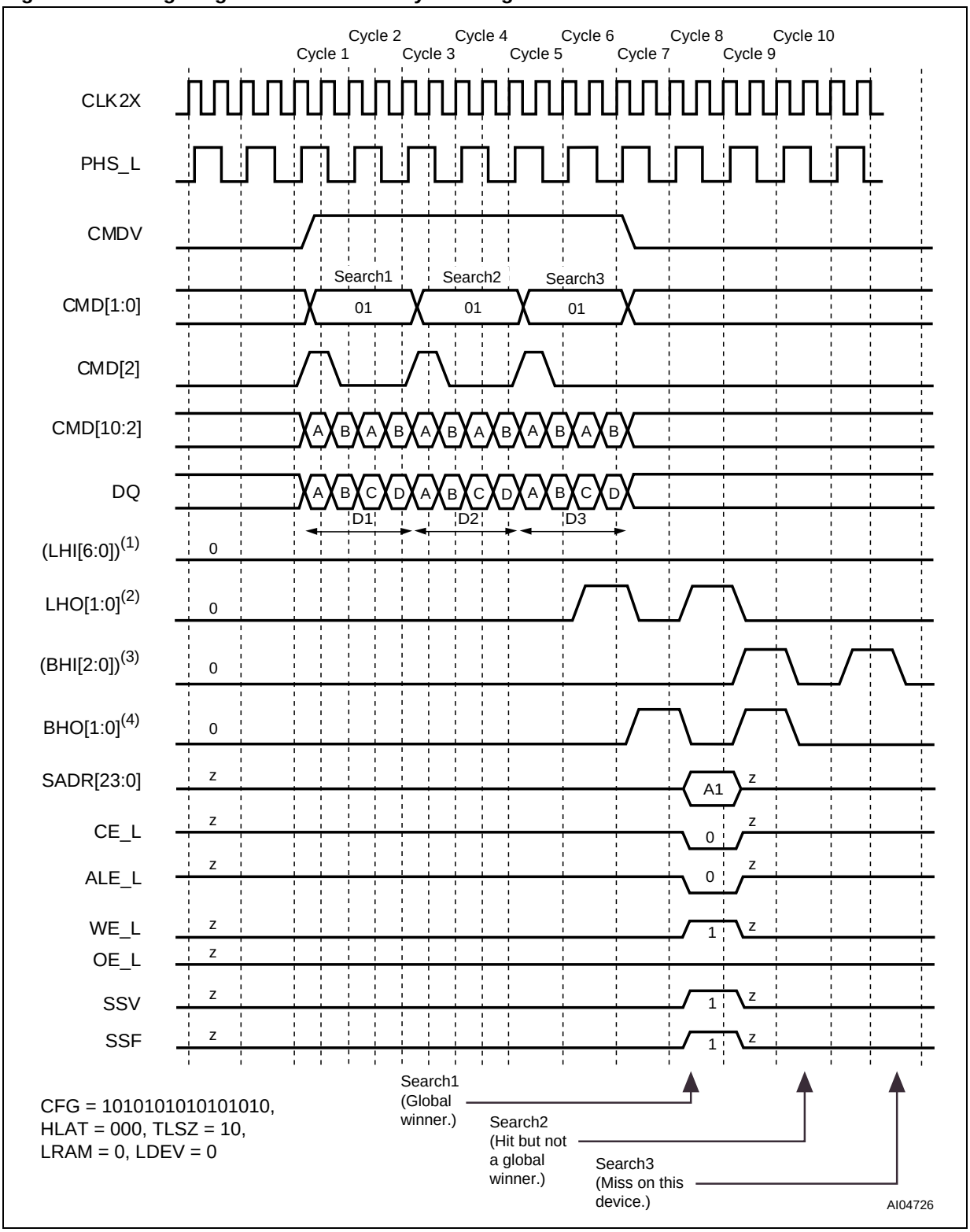
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 84. Timing Diagram for Devices Above the Winning Device in Block Number 3



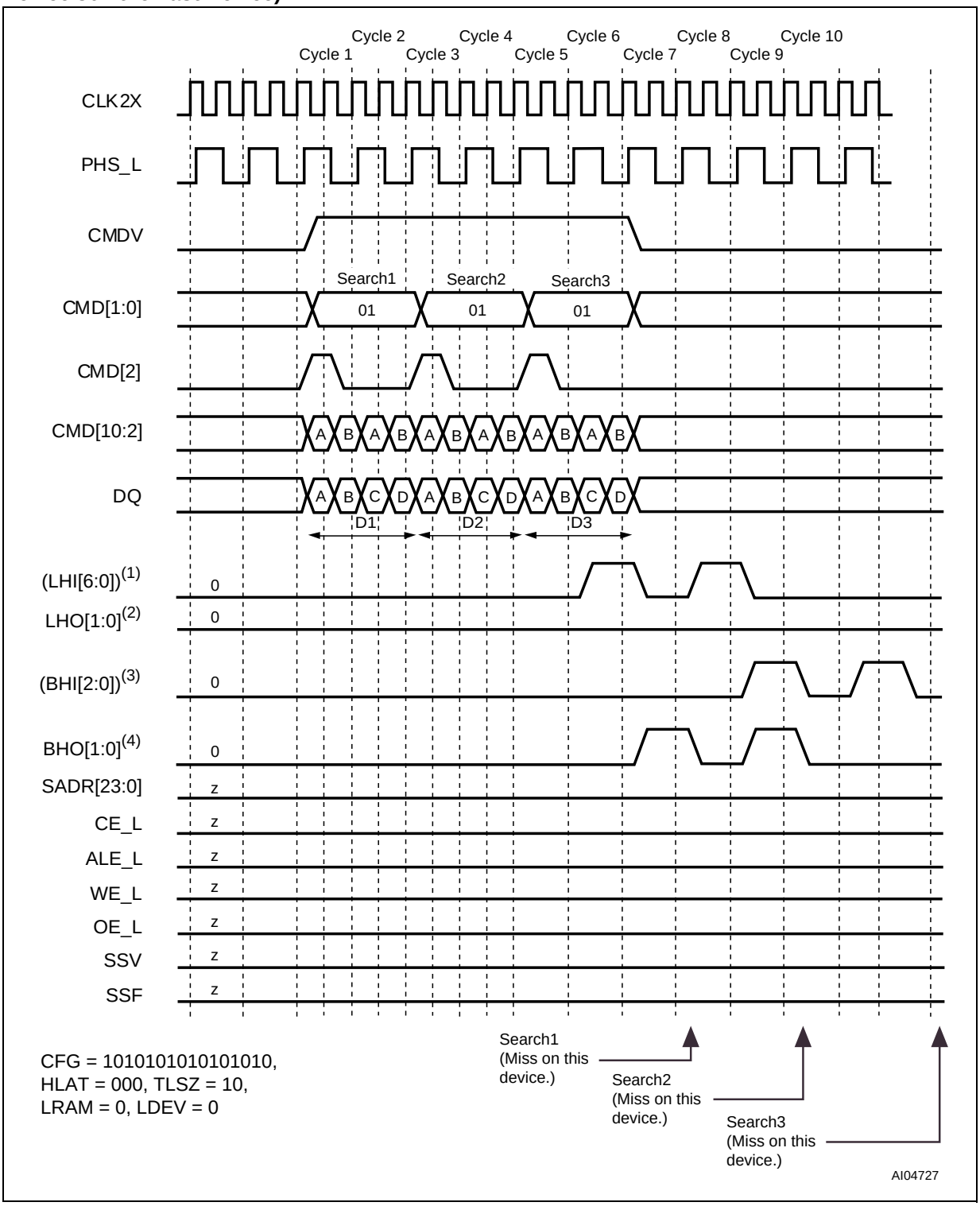
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 85. Timing Diagram for the Globally Winning Device in Block Number 3



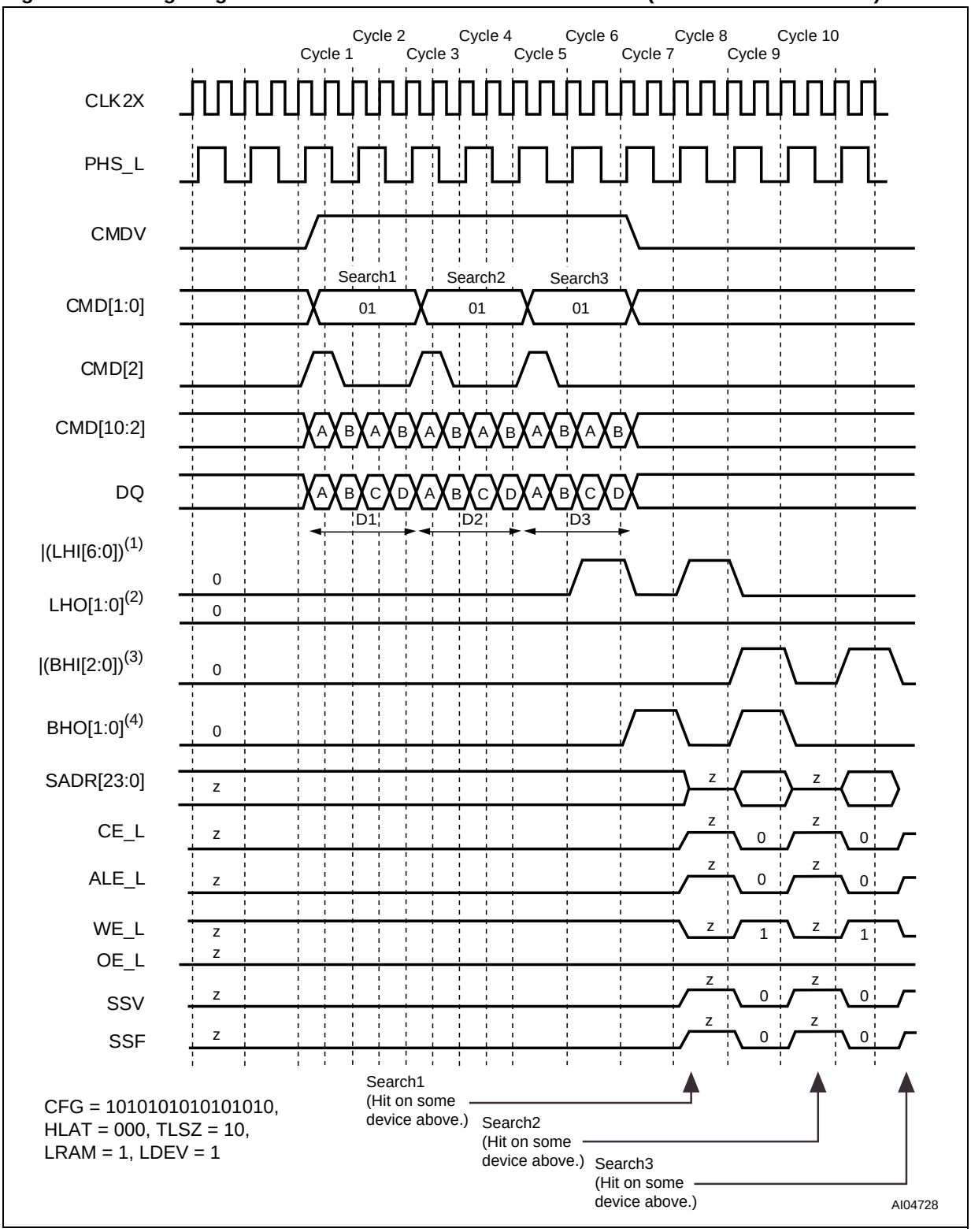
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 86. Timing Diagram for Devices Below the Winning Device in Block Number 3 (except Device 30 - the Last Device)



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 87. Timing Diagram of the Last Device in Block Number 3 (Device 30 in the Table)



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Table 48. Latency of SEARCH from Cycles C and D to SRAM Access Cycle, 288-bit

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	16K x 288-bit	4
2–8 (TLSZ = 01)	128K x 288-bit	5
2–31 (TLSZ = 10)	496K x 288-bit	6

Table 49. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

MIXED SEARCHES

Tables Configured with Different Widths Using an M7040N with CFG_L LOW

The sample operation shown is for a single device with CFG = 1010010100000000. It contains three tables of x72, x144, and x288 widths. The operation may be generalized to a block of 8–31 devices using four blocks; the timing and the pipeline operation is the same as described previously for fixed searches on a table of one-width-size.

Figure 88, page 118 shows three sequential searches:

– a 72-bit search on the table configured as x72;
– a 144-bit search on a table configured as x144; and
– a 288-bit search on the table configured as x288 bits that each results in a hit.

Note: The DQ[71:70] will be '00' in both of the Cycles A and B of the x72-bit search (Search1). DQ[71:70] is '01' in both of the Cycles A and B of the x144-bit search (Search2). DQ[71:70] is '10' in all of the Cycles A, B, C, and D of the x288-bit search (Search 3). By having table designation bits, the M7040N enables the creation of many tables in a bank of search engines of different widths.

Figure 89, page 119 shows the sample table. Two bits in each 72-bit entry will need to designated as the Table Number Bits. One example choice can be the '00' values for the table configured as x72, '01' values for tables configured as x144, and '10' values for tables configured as x288. For the above explanation, it is further assumed that bits [71:70] for each entry will be designed as these Table Designation Bits.

Tables Configured to Different Widths using an M7040N with CFG_L HIGH

Searches on tables of different widths using Table Designation Bits in the data array can be wasteful of these bits. In order to avoid wasting these bits and still support up to three tables of x72, x144, and x288, the CMD[2] and CMD[9] (in CFG_L high mode) in Cycle A of the command can be used as shown in Table 50, page 119.

Figure 88. Timing Diagram for Mixed SEARCH (One Device)

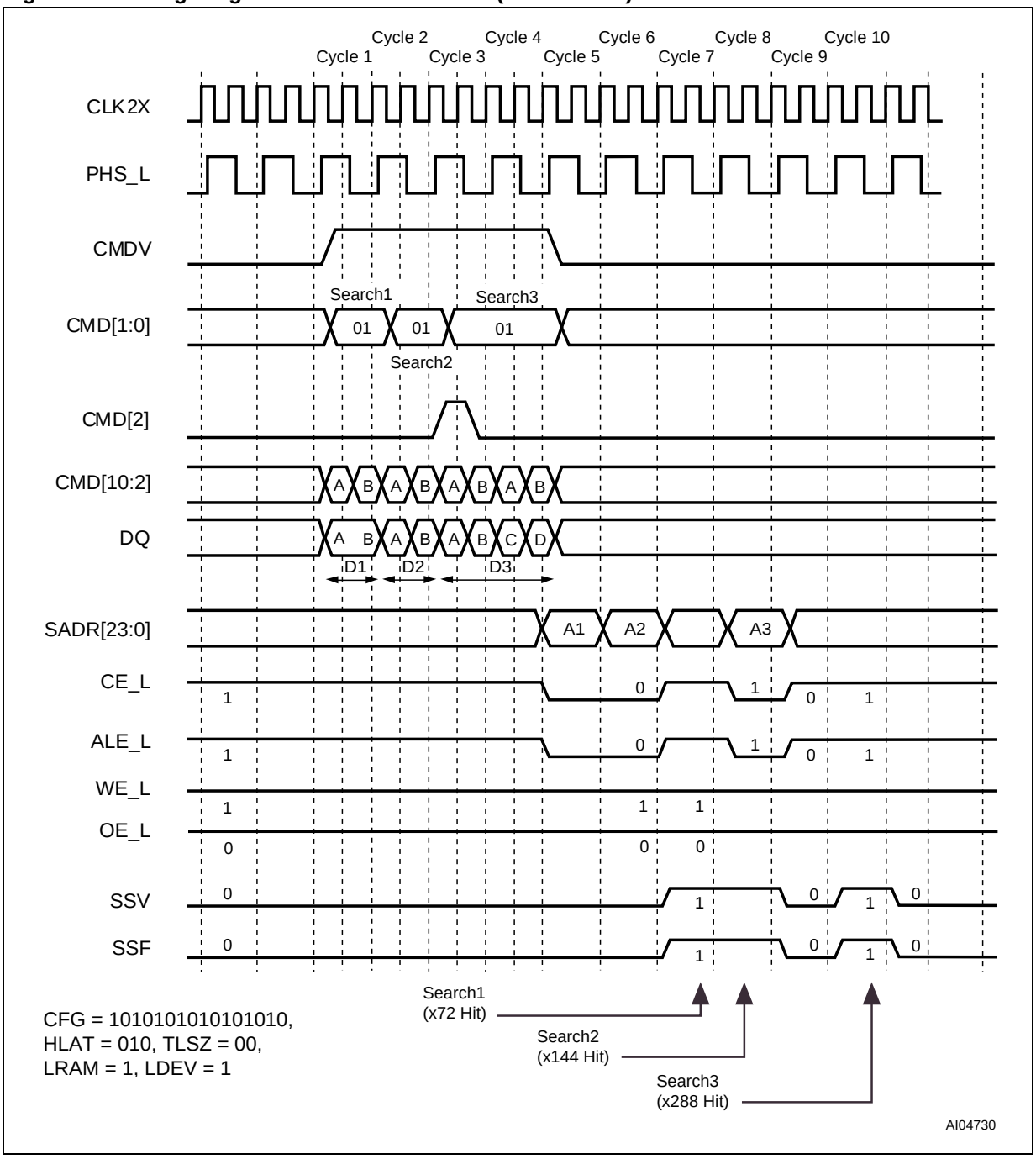


Figure 89. Multi-Width Configurations Example

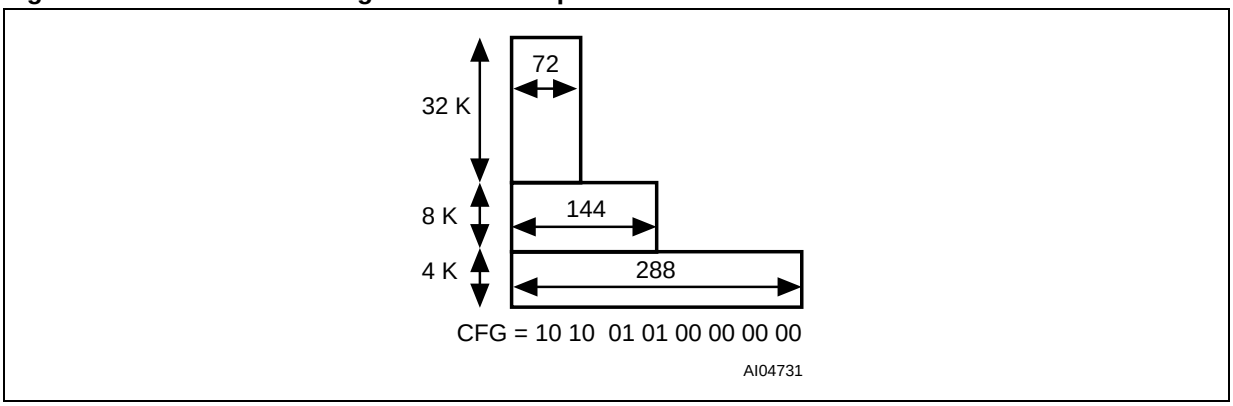


Table 50. Searches with CFG_L Set HIGH

CMD[9]	CMD[2]	SEARCH
0	0	Search 72-bit-configured partitions only
1	0	Search 144-bit-configured partitions only
X	1	Cycles A and B for searching 288-bit-configured partitions
X	0	Cycles C and D for searching 288-bit-configured partitions

LRAM AND LDEV DESCRIPTION

When search engines are cascaded using multiple M7040Ns, the SADR, CE_L, and WE_L (3-state signals) are all tied together. In order to eliminate external pull-up and pull-downs, one device in a bank is designated as the default driver. For non-SEARCH or non-LEARN cycles (see LEARN COMMAND in the section below) or search cycles with a global miss, the SADR, CE_L, and WE_L signals are driven by the device with the LRAM Bit set.

Note: It is important that only one device in a bank of search engines that are cascaded have this bit set. Failure to do so will cause contention on SADR, CE_L, WE_L, and can potentially cause damage to the device(s).

Similarly, when search engines using multiple M7040Ns are cascaded, SSF and SSV (also 3-state signals) are tied together. In order to eliminate external pull-up and pull-downs, one device in a bank is designated as the default driver. For non-SEARCH cycles or SEARCH cycles with a global miss the SSF and SSV signals are driven by the device with the LDEV Bit set.

Note: It is important that only one device in a bank of search engines that are cascaded together have this bit set. Failure to do so will cause contention on SSV and SSF and can potentially cause damage to the device(s).

LEARN COMMAND

Bit [0] of each 72-bit data location specifies whether an entry in the database is occupied. If all the entries in a device are occupied, the device asserts FULO signal to inform the downstream devices that it is full.

The result of this communication between depth-cascaded devices determines the global FULL signal for the entire table. The FULL signal in the last device determines the fullness of the depth-cascaded table.

In a depth-cascaded table, only a single device will learn the entry through the application of a LEARN Instruction. The determination of which device is going to learn is based on the FULI and FULO signalling between the devices. The first non-full device learns the entry by storing the contents of the specified comparand registers to the location(s) pointed to by NFA.

In a x72-configured table the LEARN command writes a single 72-bit location. In a x144-configured table the LEARN command writes the next even and odd 72-bit locations. In 144-bit mode, Bit[0] of the even and odd 72-bit locations is '0,' which indicates they are cascaded empty, or '1,' which indicates they are occupied.

The global FULL signal indicates to the Table Controller (the host ASIC) that all entries within a block are occupied and that no more entries can be learned. The M7040N updates the signal after each WRITE or LEARN command to a data array. The LEARN command generates a WRITE cycle to the external SRAM, also using the NFA register as part of the SRAM address (see SRAM ADDRESSING, page 128).

The LEARN command is supported on a single block containing up to eight devices if the table is configured either as a x72 or a x144. The LEARN command is not supported for x288-configured tables.

LEARN is a pipelined operation and lasts for two CLK cycles, as shown in Figure 90, page 121 where TLSZ = 00, and Figure 91, page 122 and Figure 92, page 123 where TLSZ = 01 (which assume the device performing the LEARN operation is not the last device in the table and has its LRAM Bit set to '0.'

Note: The OE_L for the device with the LRAM Bit set goes high for two cycles for each LEARN (one during the SRAM WRITE cycle, and one the cycle before). The latency of the SRAM WRITE cycle from the second cycle of the Instruction is shown in Table 51, page 123.

The sequence of operation is as follows:

– **Cycle 1A**: The host ASIC applies the LEARN Instruction on the CMD[1:0], using CMDV = 1. The CMD[5:2] field specifies the index of the comparand register pair that will be written in the data array in the 144-bit-configured table. For a LEARN in a 72-bit-configured table, the even-numbered comparands specified by this index will be written. CMD[8:6] carries the bits that will be driven on SADR[23:21] in the SRAM WRITE cycle.

– **Cycle 1B**: The host ASIC continues to drive CMDV to '1,' CMD[1:0] to '11,' and CMD[5:2] with the comparand pair index. CMD[6] must be set to '0' if the LEARN is being performed on a 72-bit-configured table, and to '1' if the LEARN is being performed on a 144-bit-configured table.

– **Cycle 2:** The host ASIC drives the CMDV to '0.' At the end of Cycle 2, a new instruction can begin. The latency of the SRAM WRITE is the same as the search to the SRAM READ Cycle.

Figure 90. Timing Diagram of LEARN: TLSZ = 00

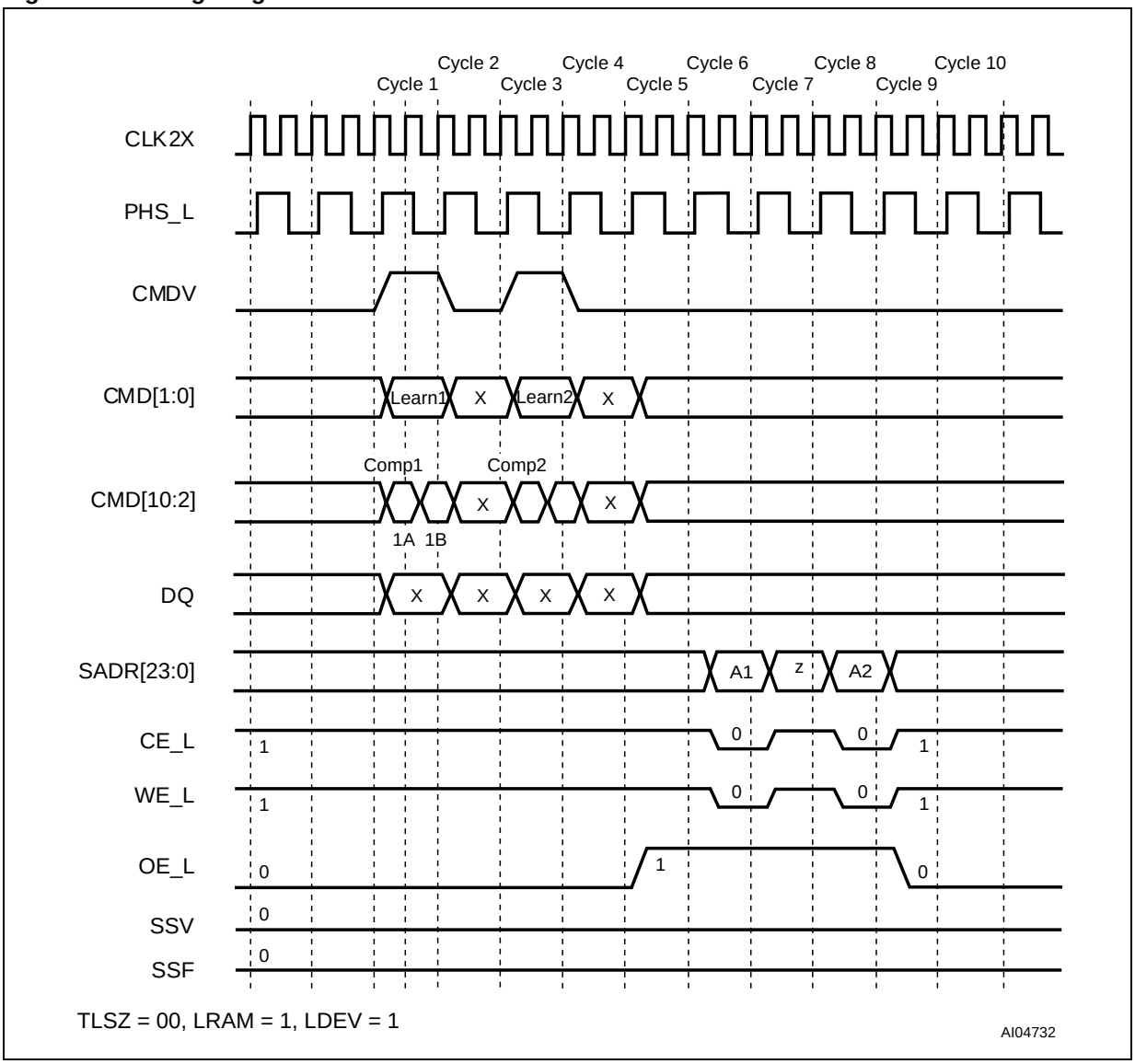


Figure 91. Timing Diagram of LEARN: TLSZ = 01 (Except on the Last Device)

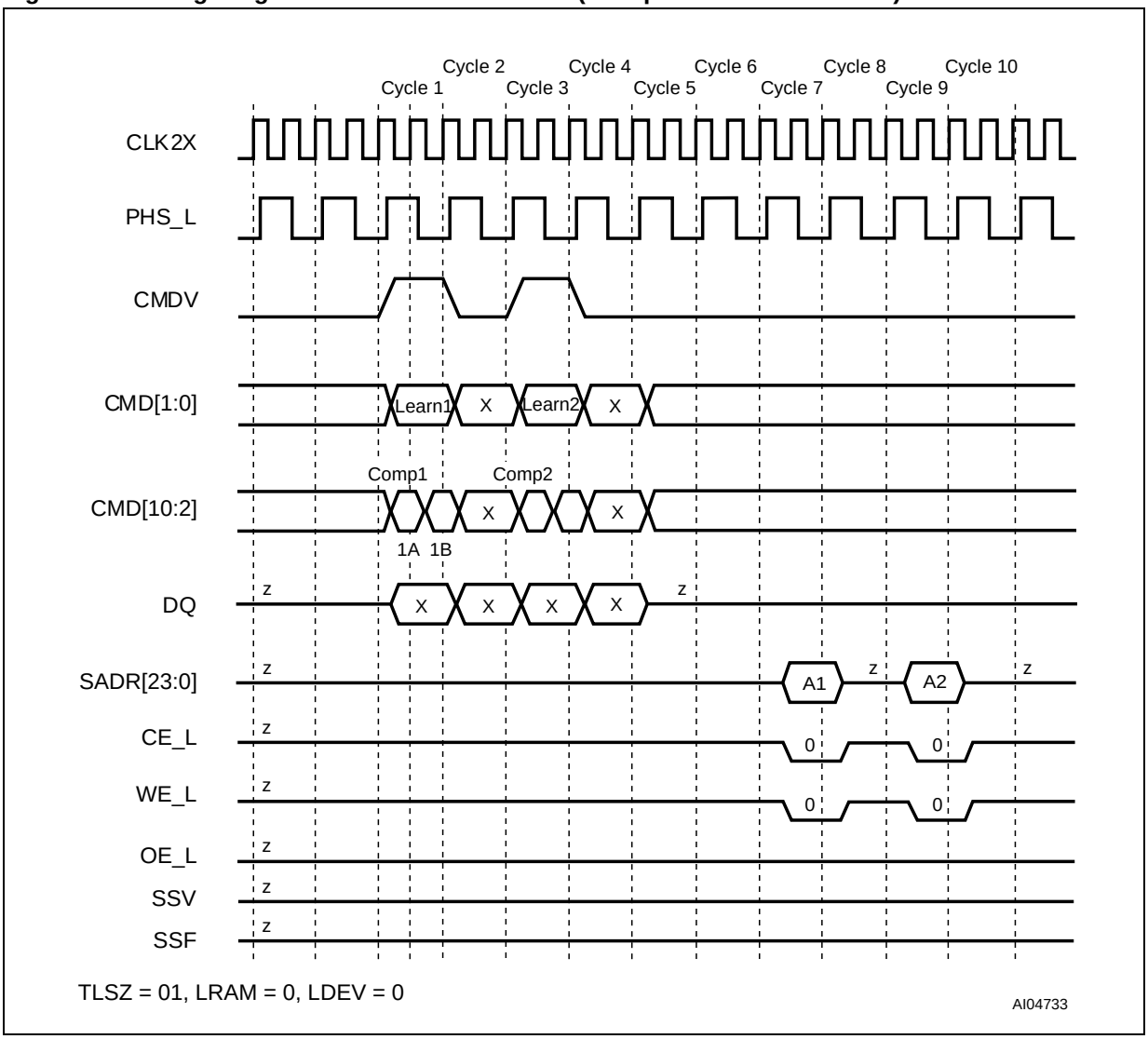


Figure 92. Timing Diagram of LEARN on Device 7: TLSZ = 01

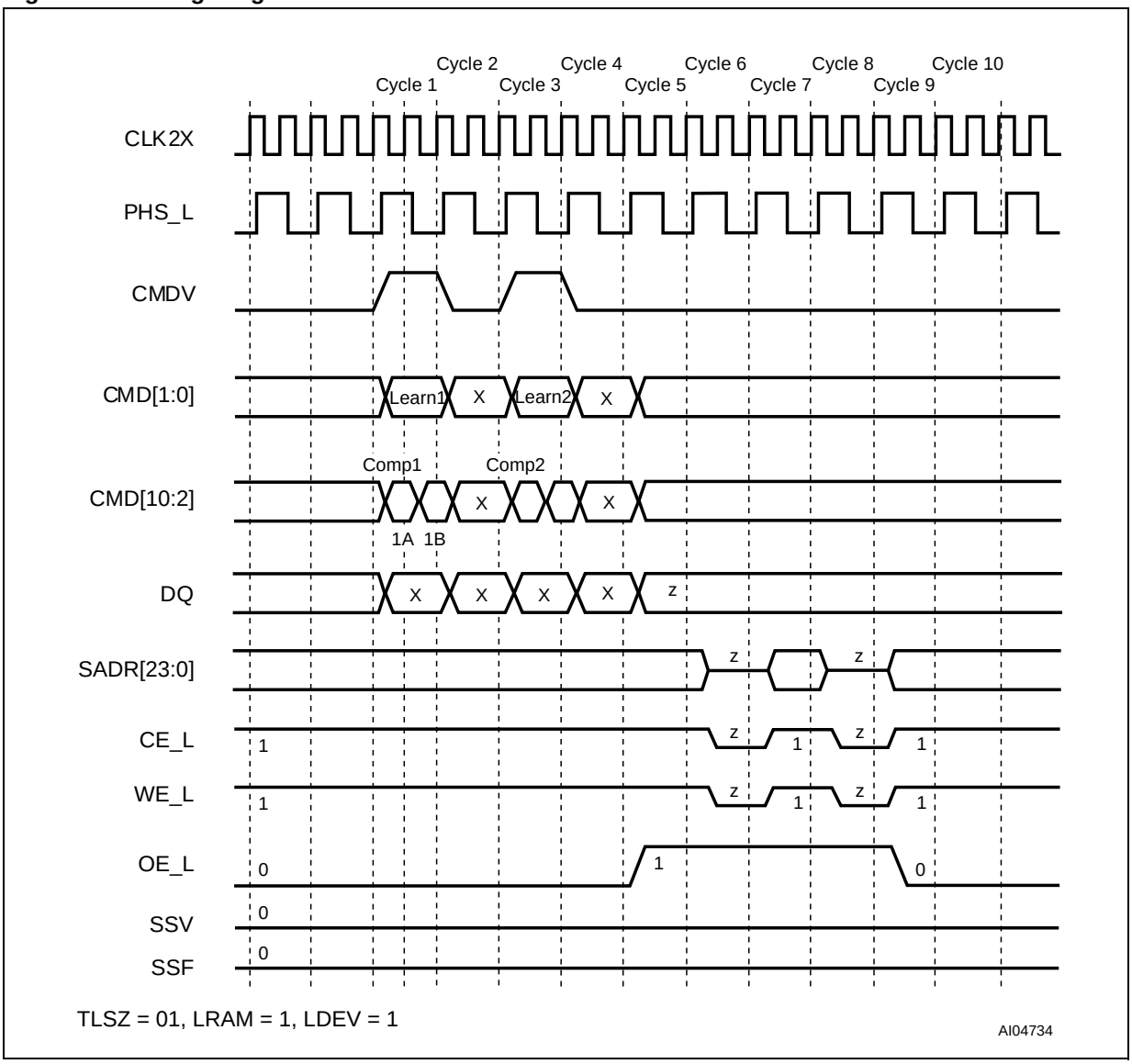


Table 51. Latency of SRAM WRITE Cycle from Second Cycle of LEARN Instruction

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	16K x 72-bit	4
2–8 (TLSZ = 01)	128K x 72-bit	5
2–31 (TLSZ = 10)	496K x 72-bit	6

DEPTH-CASCADING

The search engine application can depth-cascade the device to various table sizes of different widths (e.g., 72-bit, 144-bit, and 288-bit configurations). The devices perform all the necessary arbitration to decide which device drives the SRAM Bus. The latency of the searches increases as the table size increases while the search rate remains constant.

Depth-Cascading Up to Eight Devices (One Block)

Figure 93, page 125 shows how up to eight devices can cascade to form a 512K x 72, 256K x 144, or 128K x 288 bit table. It also shows the interconnection between the devices for depth-cascading. Each Search Engine asserts the LHO[1] and LHO[0] signals to inform downstream devices of its result. The LHI[6:0] signals for a device are connected to LHO signals of the upstream devices. The host ASIC must program the TLSZ to '01' for each of up to eight devices in a block. Only a single device drives the SRAM Bus in any single cycle.

Depth-Cascading Up to 31 Devices (4 Blocks)

Figure 94, page 126 shows how to cascade up to four blocks. Each block contains up to eight M7040Ns (except the last block) and the interconnection within each is shown in Figure 93, page 125.

Note: The interconnection between blocks for depth-cascading is important. For each SEARCH, a block asserts BHO[2], BHO[1], and BHO[0]. The BHO[2:0] signals for a block are the signals taken only from the last device in the block. For all other devices within that block, these signals stay open and floating. The host ASIC must program the table size (TLSZ) field to '10' in each of the devices for cascading up to 31 devices (in up to four blocks).

Depth-Cascading to Generate a “FULL” Signal

Bit[0] of each of the 72-bit entries is designated as a special bit (1 = occupied; 0 = empty). For each LEARN or PIO WRITE to the data array, each device asserts FULO[1] and FULO[0] if it does not have any empty locations (see Figure 95, page 127).

Each device combines the FULO signals from the devices above it with its own “full” status to generate a FULL signal that gives the “full” status of the table up to the device asserting the FULL signal. Figure 95, page 127 shows the hardware connection diagram for generating the FULL signal that goes back to the ASIC. In a depth-cascaded block of up to eight devices, the FULL signal from the last device should be fed back to the ASIC controller to indicate the fullness of the table. The FULL signal of the other devices should be left open.

Note: The LEARN instruction is supported for only up to eight devices, whereas FULL cascading is allowed only for one block in tables containing more than eight devices. In tables for which a LEARn instruction is not going to be used, the Bit[0] of each 72-bit entry should always be set to '1.'

Figure 93. Depth-Cascading to Form a Single Block

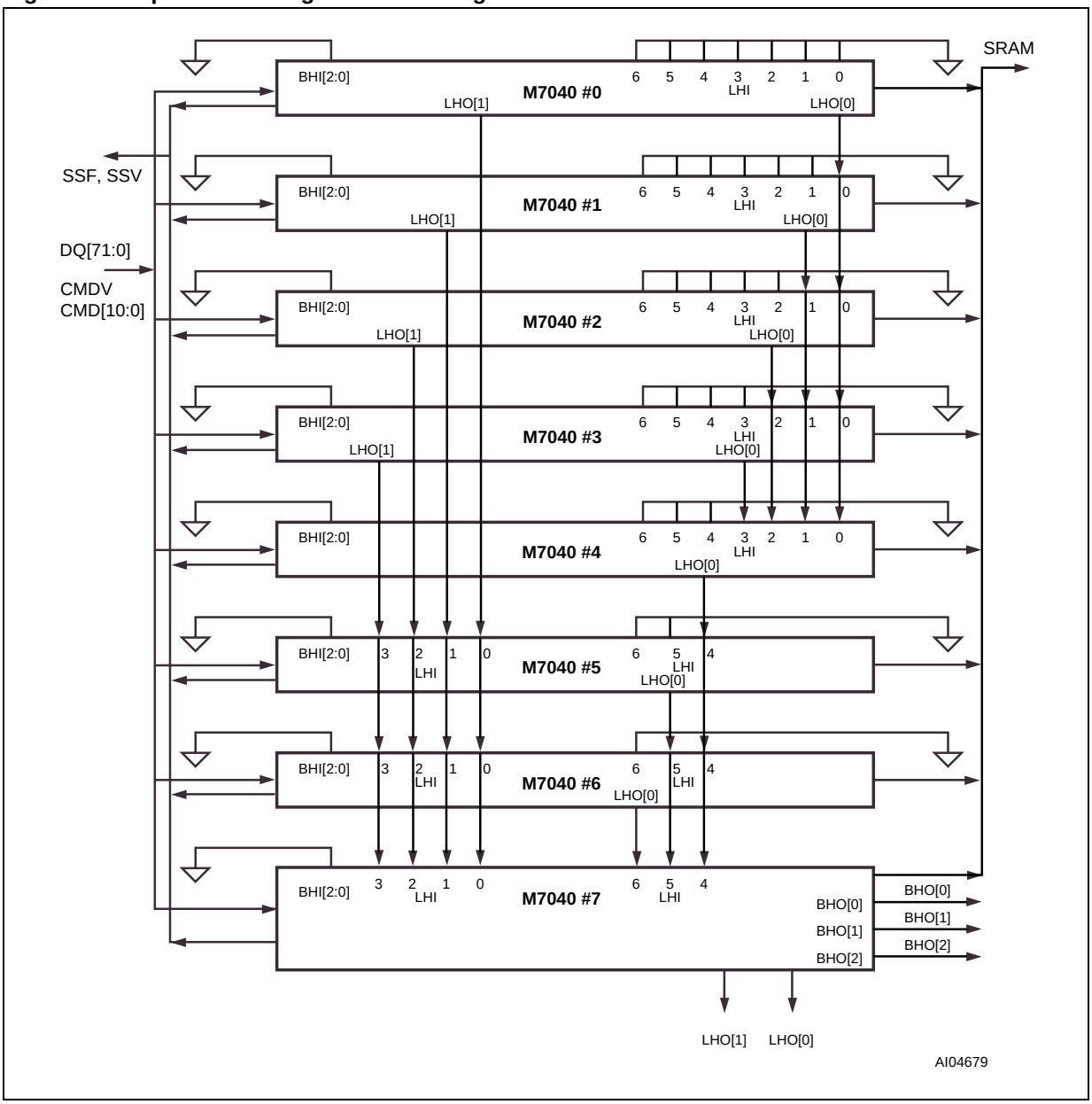


Figure 94. Depth-Cascading Four Blocks

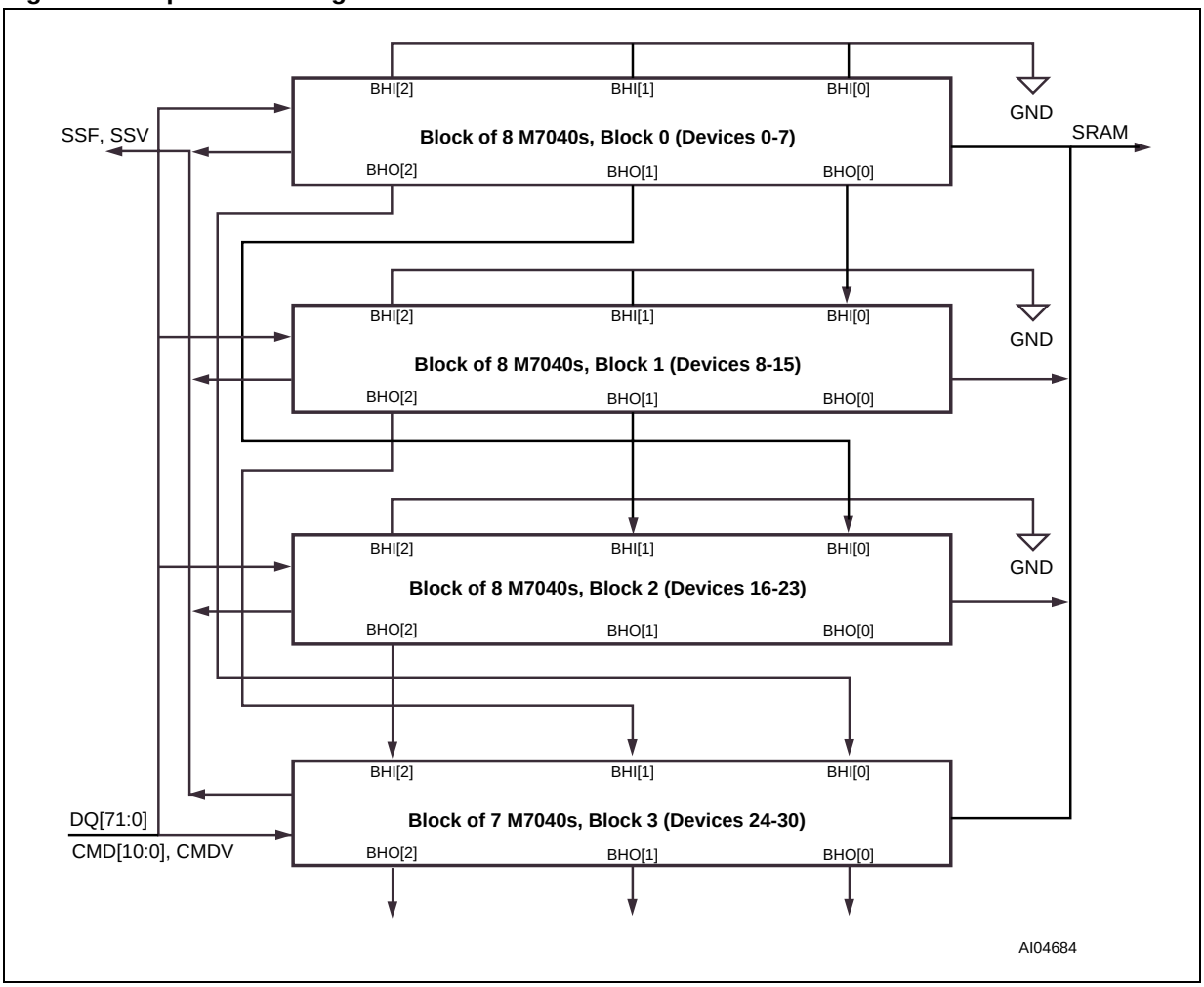
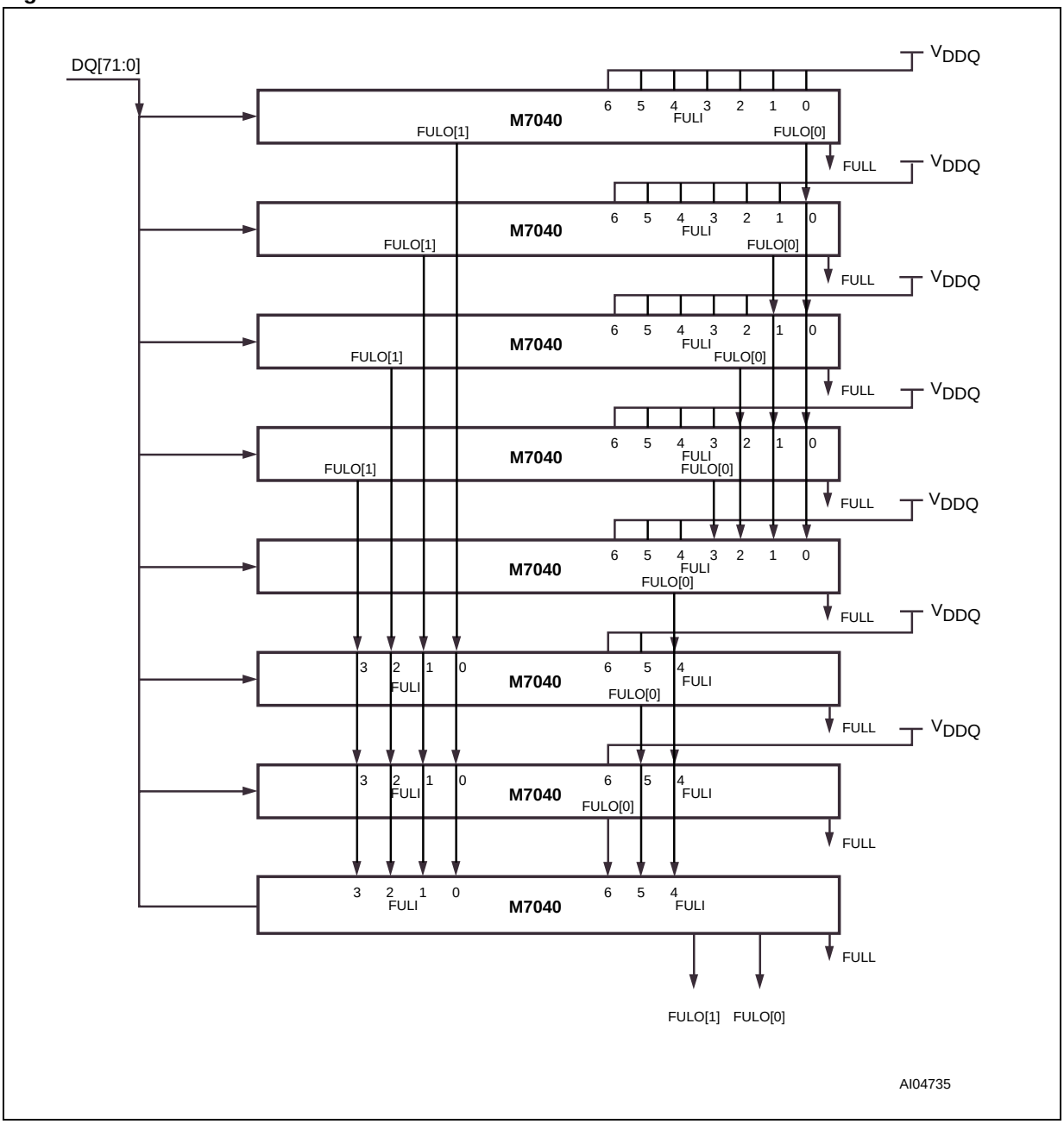


Figure 95. “FULL” Generation in a Cascaded Table



SRAM ADDRESSING

Table 52 describes the commands used to generate addresses on the SRAM Address Bus. The index [15:0] field contains the address of a 72-bit entry that results in a hit in 72-bit-configured quadrant. It is the address of the 72-bit entry that lies at the 144-bit page, and the 288-bit page boundaries in 144-bit- and 288-bit-configured quadrants, respectively.

REGISTERS, page 22 of this specification, describes the NFA and SSR Registers. ADR[15:0] contains the address supplied on the DQ Bus during PIO access to the M7040N. Command Bits 8, 7, and 6 {CMD[8:6]} are passed from the command to the SRAM Address Bus (see COMMAND CODES AND PARAMETERS, page 30 for more information). ID[4:0] is the ID of the device driving the SRAM Bus (see Figure 3, page 9 and Table 2, page 8 for more information).

Table 52. Generating an SRAM Bus Address

Command	SRAM Operation	23	22	21	[20:16]	[15:0]
SEARCH	READ	C8	C7	C6	ID[4:0]	Index[15:0]
LEARN	WRITE	C8	C7	C6	ID[4:0]	NFA[15:0]
PIO READ	READ	C8	C7	C6	ID[4:0]	ADR[15:0]
PIO WRITE	WRITE	C8	C7	C6	ID[4:0]	ADR[15:0]
Indirect Access	WRITE/READ	C8	C7	C6	ID[4:0]	SSR[15:0]

SRAM PIO Access

SRAM READ enables READ access to off-chip SRAM that contains associative data. The latency from the issuance of the READ Instruction to the address appearing on the SRAM Bus is the same as the latency of the SEARCH Instruction and will depend on the TLSZ value parameter programmed in the device Configuration Register. The latency of the ACK from the READ Instruction is the same as the latency of the SEARCH Instruction to the SRAM address plus the HLAT programmed in the Configuration Register.

Note: SRAM READ is a blocking operation – no new instruction can begin until the ACK is returned by the selected device performing the access.

SRAM WRITE enables WRITE access to the off-chip SRAM containing associative data. The latency from the second cycle of the WRITE Instruction to the address appearing on the SRAM Bus is the same as the latency of the SEARCH Instruction and will depend on the TLSZ value parameter programmed in the device Configuration Register. **Note:** SRAM WRITE is a pipelined operation – new instruction can begin right after the previous command has ended.

SRAM READ with a Table of One Device

SRAM READ enables READ access to the off-chip SRAM containing associative data. The latency from the issuance of the READ Instruction to the address appearing on the SRAM Bus is the same as the latency of the SEARCH Instruction and will depend on the TLSZ value parameter programmed in the device configuration register. The latency of the ACK from the READ Instruction is the same as the latency of the SEARCH Instruction to the SRAM address plus the HLAT programmed in the configuration register.

The following explains the SRAM READ operation in a table with only one device that has the following parameters: TLSZ = 00, HLAT = 000, LRAM = 1, and LDEV = 1. Figure 96, page 129 shows the associated timing diagram.

For the following description, the selected device refers to the only device in the table because it is the only device to be accessed.

The sequence of the operation is as follows:

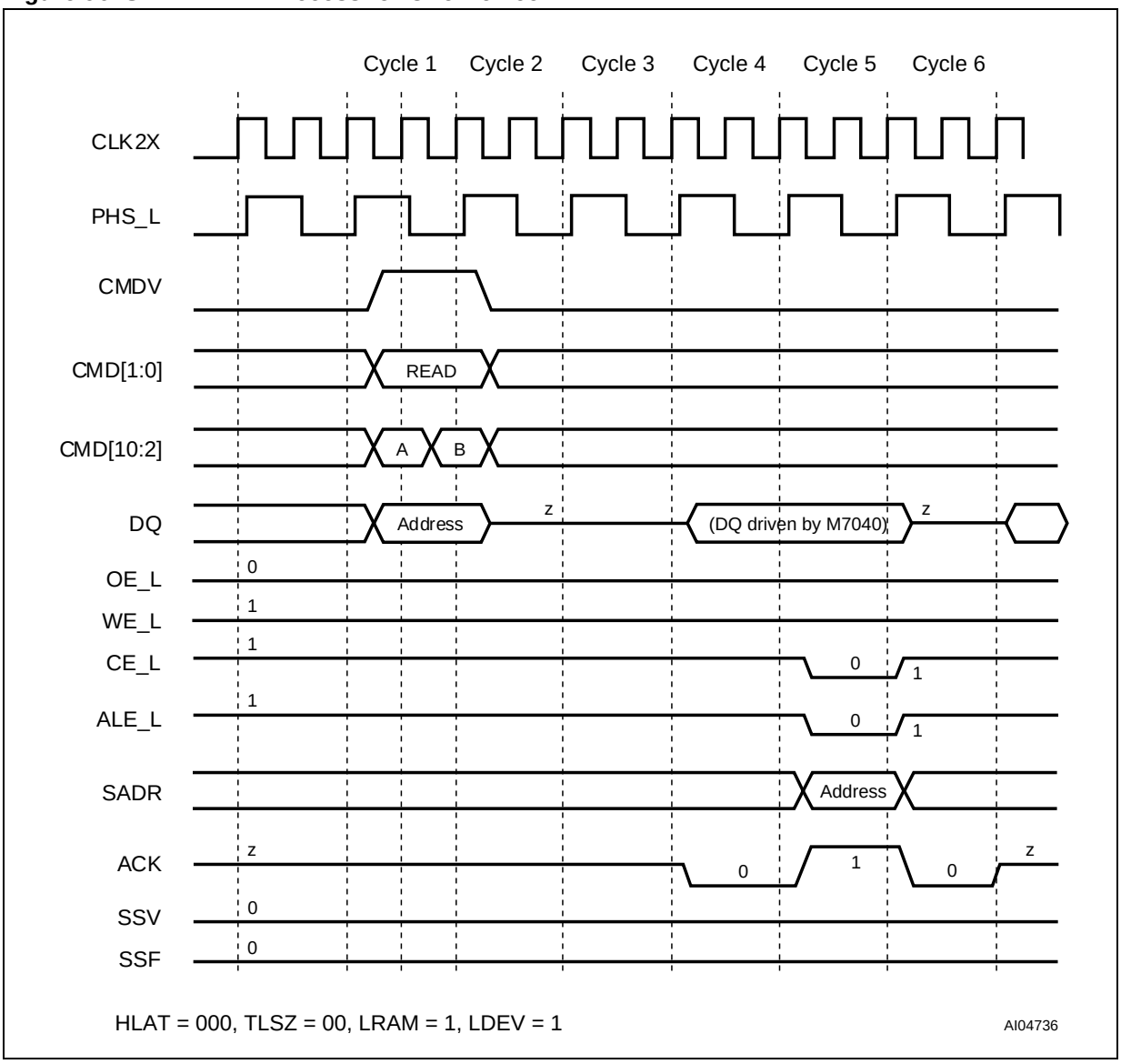
– **Cycle 1A:** The host ASIC applies the READ Instruction on the CMD[1:0], using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. During this cycle, the host ASIC also supplies SADR[23:21] on CMD[8:6] in this cycle.

– **Cycle 1B:** The host ASIC continues to apply the READ Instruction on the CMD[1:0] using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address.

– **Cycle 2:** The host ASIC floats DQ[71:0] to a 3-state condition.
– **Cycle 3:** The host ASIC keeps DQ[71:0] in a 3-state condition.
– **Cycle 4:** The selected device starts to drive DQ[71:0] and drives ACK from High-Z to low.
– **Cycle 5:** The selected device drives the READ address on SADR[23:0]; it also drives ACK high, CE_L low, and ALE_L low.
– **Cycle 6:** The selected device drives CE_L high, ALE_L high, the SADR Bus, and the DQ Bus in a 3-state condition; it drives ACK low.

At the end of Cycle 6, the selected device floats ACK in a 3-state condition, and a new command can begin.

Figure 96. SRAM READ Access for One Device



SRAM READ with a Table of Up to Eight Devices

The following explains the SRAM READ operation completed through a table of up to eight devices using the following parameters: TLSZ = 01. Figure 97, page 131 diagrams a block of eight devices.

The following assumes that SRAM access is successfully achieved through M7040N Device 0. Figure 98, page 132 and Figure 99, page 133 show timing diagrams for Device 0 and Device 7, respectively.

– **Cycle 1A:** The host ASIC applies the READ Instruction on the CMD[1:0] using CMDV = 1. The DQ Bus supplies the address, with DQ[20:19] set to '10' to select the SRAM address. The host ASIC selects the device for which ID[4:0] matches the DQ[25:21] lines. During this cycle the host ASIC also supplies SADR[23:21] on CMD[8:6].
– **Cycle 1B:** The host ASIC continues to apply the READ Instruction on the CMD[1:0] using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address.
– **Cycle 2:** The host ASIC floats DQ[71:0] to a 3-state condition.
– **Cycle 3:** The host ASIC keeps DQ[71:0] in a 3-state condition.
– **Cycle 4:** The selected device starts to drive DQ[71:0].
– **Cycle 5:** The selected device continues to drive DQ[71:0] and drives ACK from high-Z to low
– **Cycle 6:** The selected device drives the READ address on SADR[23:0]. It also drives ACK high, CE_L low, WE_L high, and ALE_L low.
– **Cycle 7:** The selected device drives CE_L, ALE_L, WE_L, and the DQ Bus in a 3-state condition. It continues to drive ACK low.

At the end of Cycle 7, the selected device floats ACK in 3-state condition and a new command can begin.

Figure 97. Table with Eight Devices

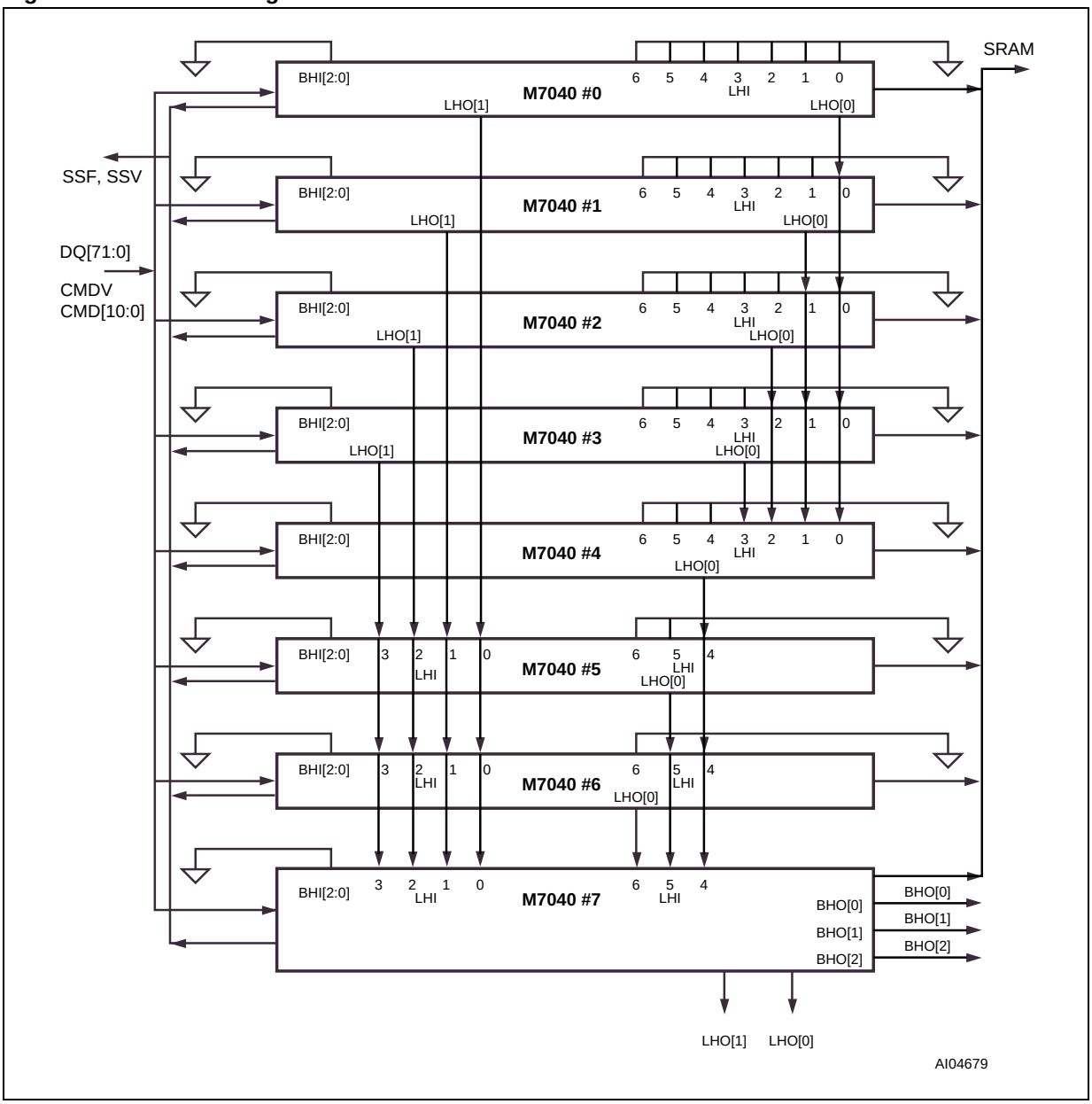


Figure 98. SRAM READ Through Device 0 in a Block of Eight Devices

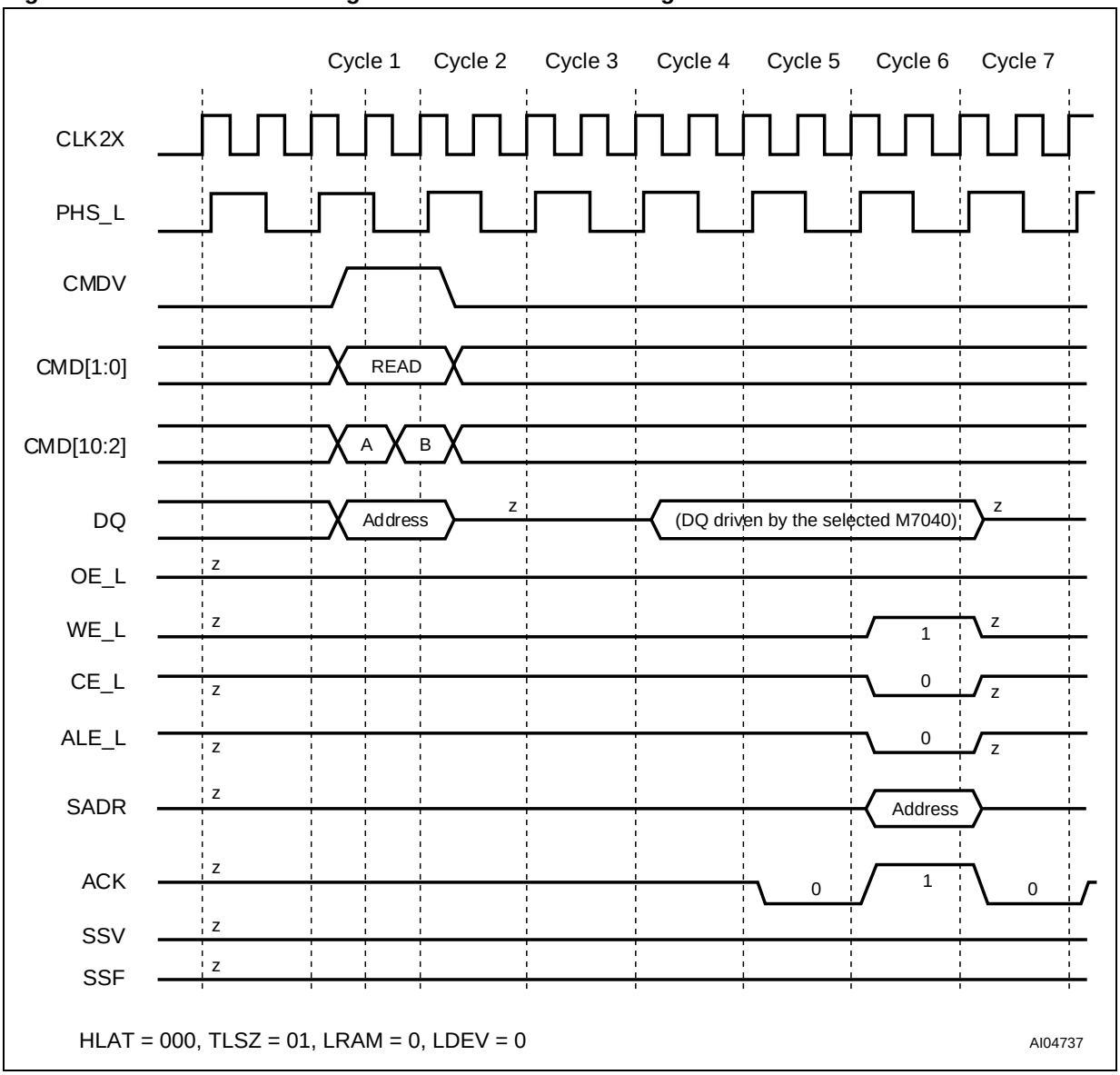
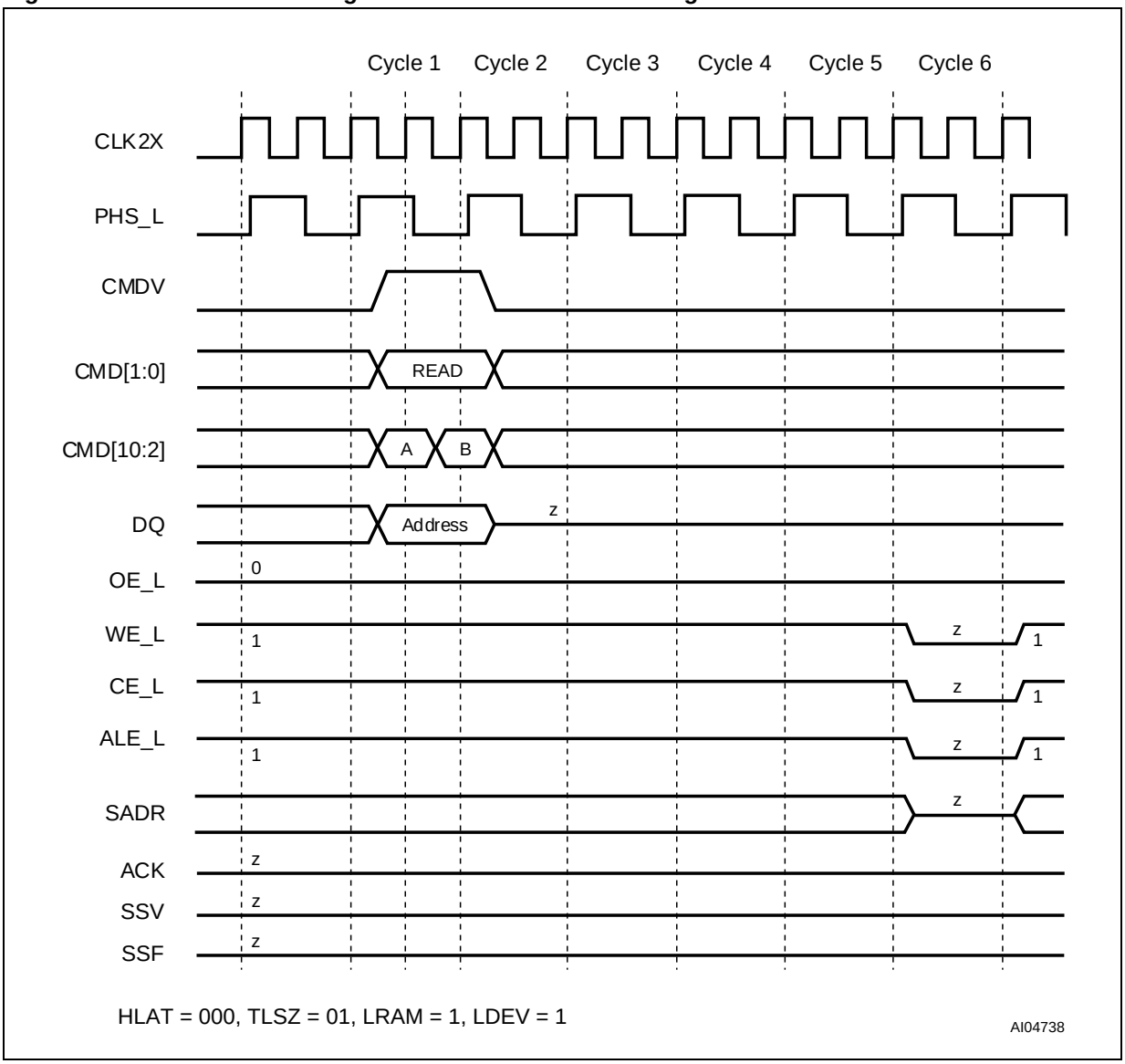


Figure 99. SRAM READ Timing for Device 7 in a Block of Eight Devices



SRAM READ with a Table of Up to 31 Devices

The following explains the SRAM READ operation accomplished through a table of up to 31 devices, using the following parameters: TLSZ = 10. The diagram of such a table is shown in Figure 100, page 135.

The following assumes that SRAM access is being accomplished through M7040N Device 0 and that Device 0 is the selected device. Figure 101, page 136 and Figure 102, page 137 show the timing diagrams for Device 0 and Device 30, respectively.

– **Cycle 1A:** The host ASIC applies the READ Instruction to CMD[1:0] using CMDV = 1. The DQ Bus supplies the address, with DQ[20:19] set to '10,' to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. During this cycle, the host ASIC also supplies SADR[23:21] on CMD[8:6].
– **Cycle 1B:** The host ASIC continues to apply the READ Instruction to CMD[1:0] using CMDV = 1. The DQ Bus supplies the address, with DQ[20:19] set to '10,' to select the SRAM address.
– **Cycle 2:** The host ASIC floats DQ[71:0] to a 3-state condition.
– **Cycle 3:** The host ASIC keeps DQ[71:0] in a 3-state condition.
– **Cycle 4:** The selected device starts to drive DQ[71:0].
– **Cycles 5 to 6:** The selected device continues to drive DQ[71:0].
– **Cycle 7:** The selected device continues to drive DQ[71:0] and drives an SRAM READ cycle.
– **Cycle 8:** The selected device drives ACK from Z to low.
– **Cycle 9:** The selected device drives ACK to high.
– **Cycle 10:** The selected device drives ACK from high to low.

At the end of Cycle 10, the selected device floats ACK in a 3-state condition.

Figure 100. Table of 31 Devices Made of Four Blocks

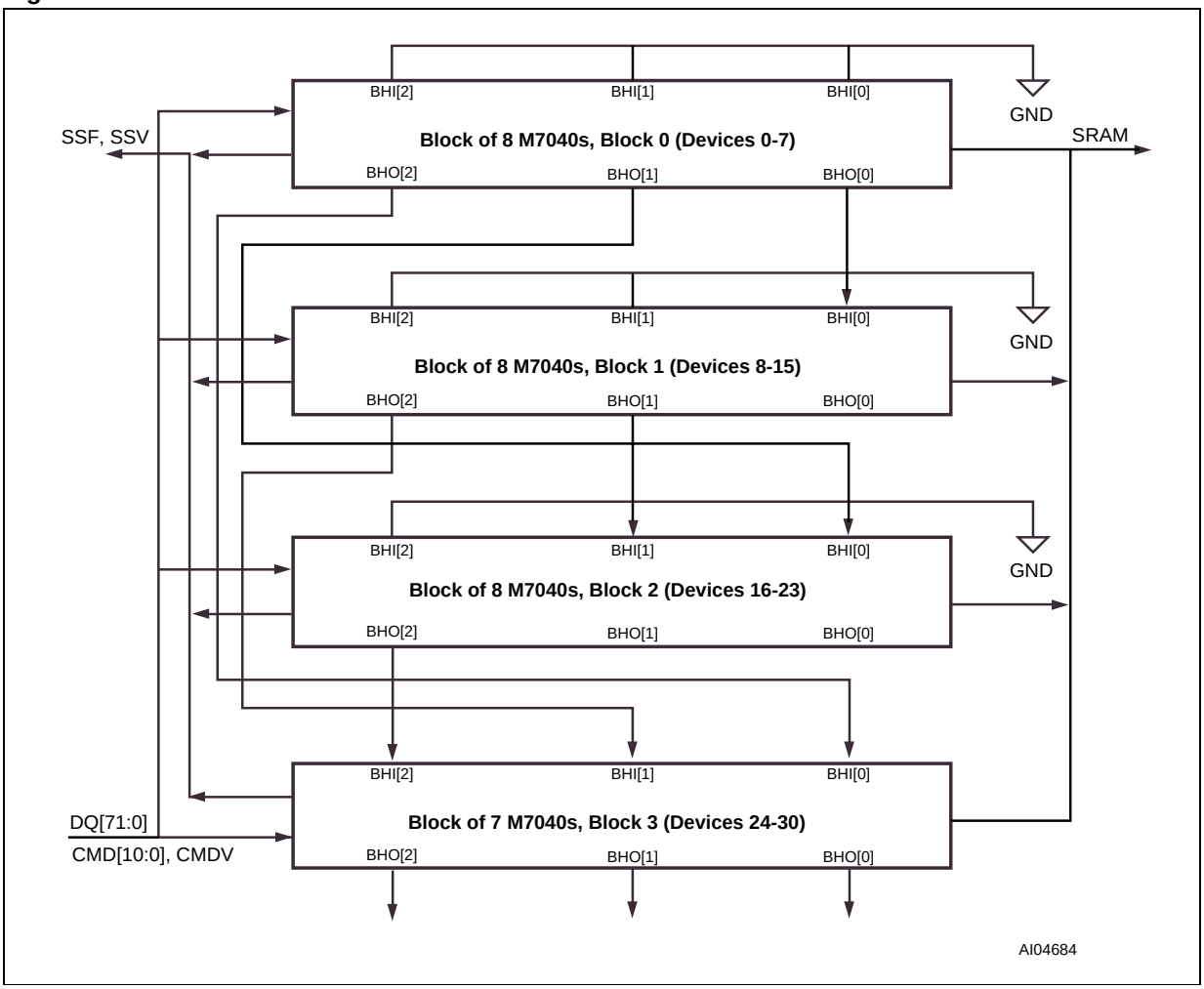


Figure 101. SRAM READ Through Device 0 in a Bank of 31 Devices (Device 0 Timing)

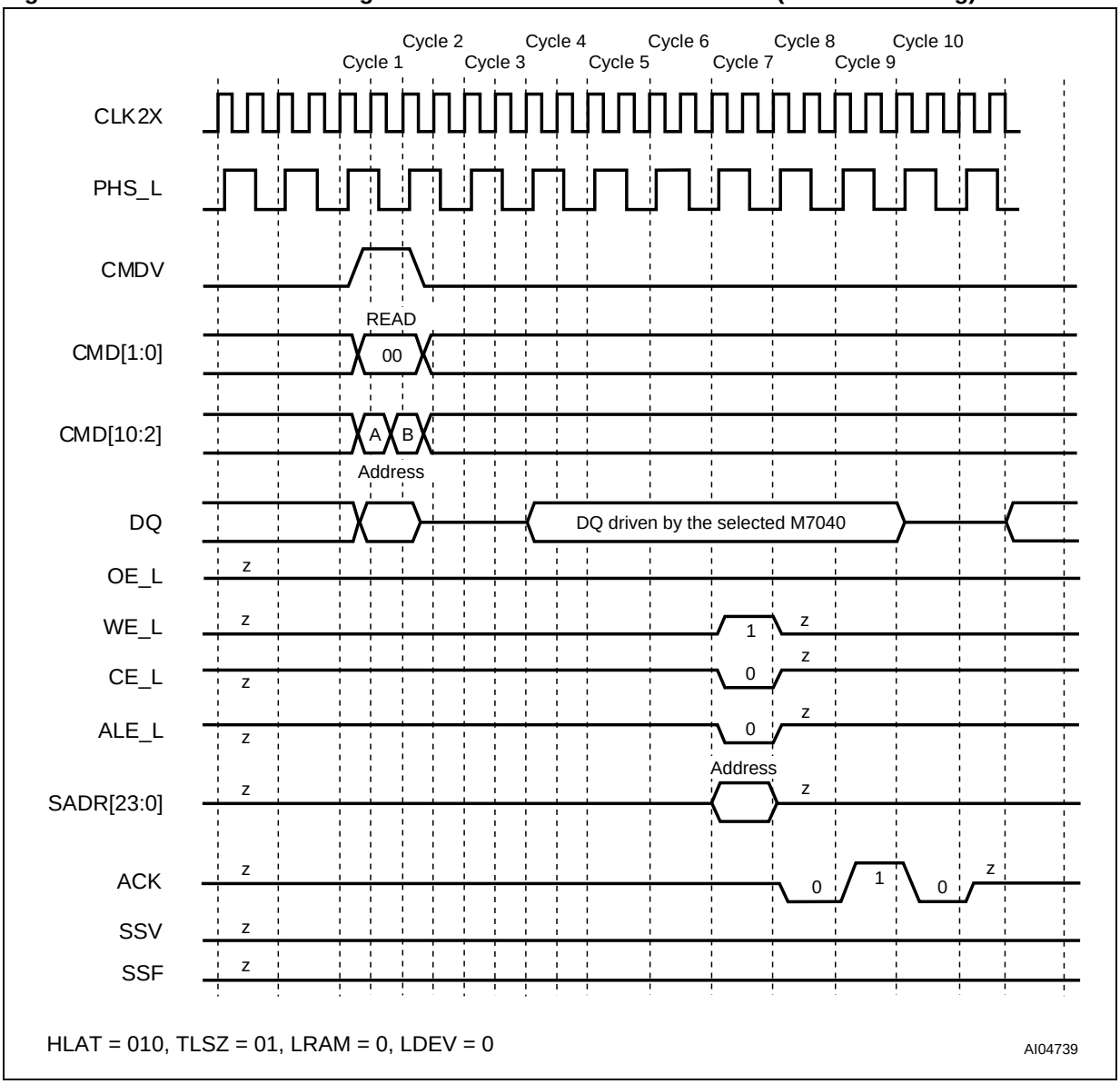
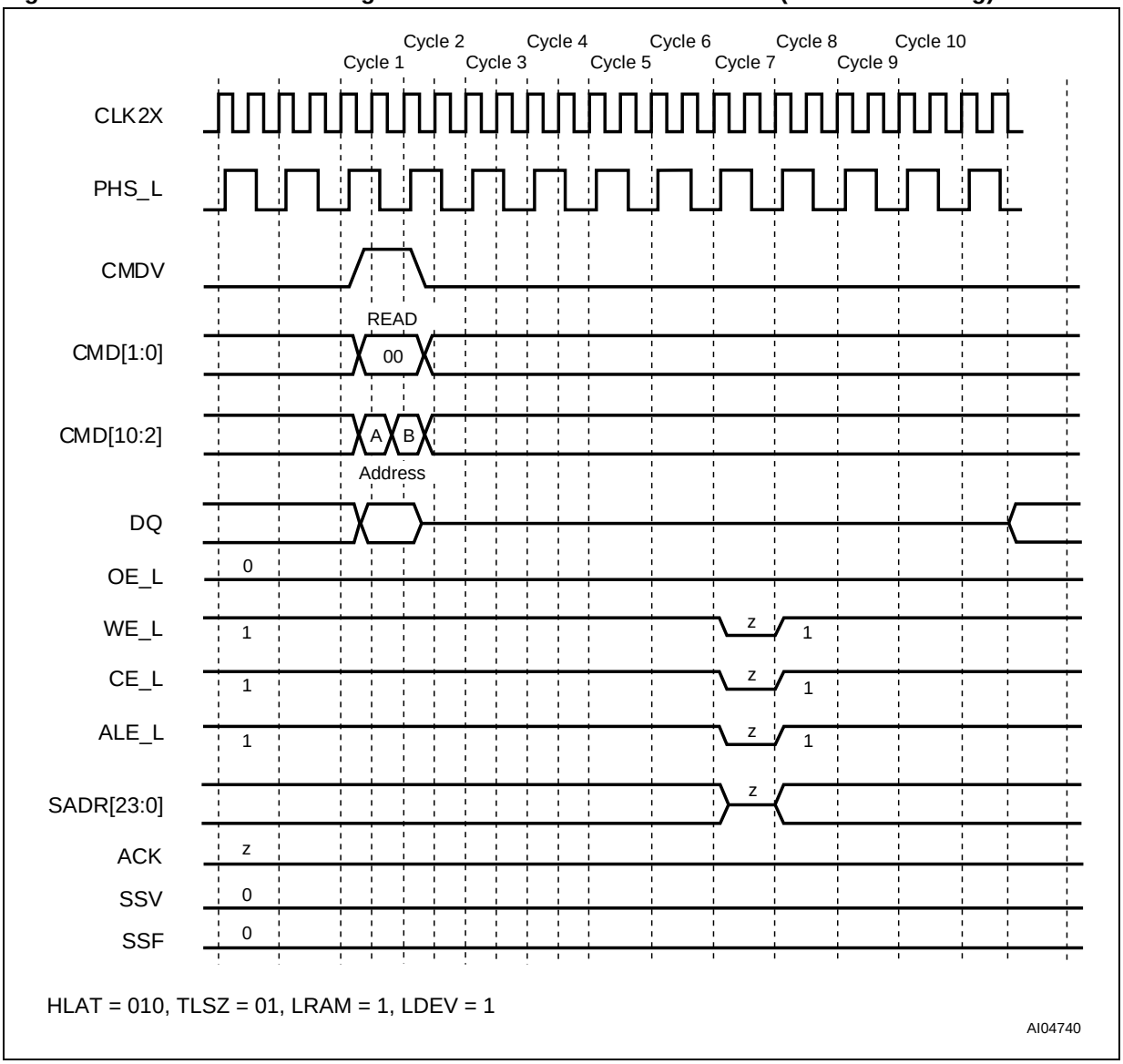


Figure 102. SRAM READ Through Device 0 in a Bank of 31 Devices (Device 30 Timing)



SRAM WRITE with a Table of One Device

SRAM WRITE enables WRITE access to the off-chip SRAM that contains associative data. The latency from the second cycle of the WRITE Instruction to the address appearing on the SRAM Bus is the same as the latency of the SEARCH Instruction, and will depend on the TLSZ value parameter programmed in the device configuration register. The following explains the SRAM WRITE operation accomplished with a table of only one device of the following parameters: TLSZ = 00, HLAT = 000, LRAM = 1, and LDEV = 1. Figure 103, page 139 shows the timing diagram.

For the following description the selected device refers to the only device in the table as it is the only device that will be accessed.

– **Cycle 1A:** The host ASIC applies the WRITE Instruction on CMD[1:0] using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. The host ASIC also supplies SADR[23:21] on CMD[8:6] in this cycle.

  Note: CMD[2] must be set to '0' for SRAM WRITE because Burst WRITEs into the SRAM are not supported.

– **Cycle 1B:** The host ASIC continues to apply the WRITE Instruction on CMD[1:0], using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address.

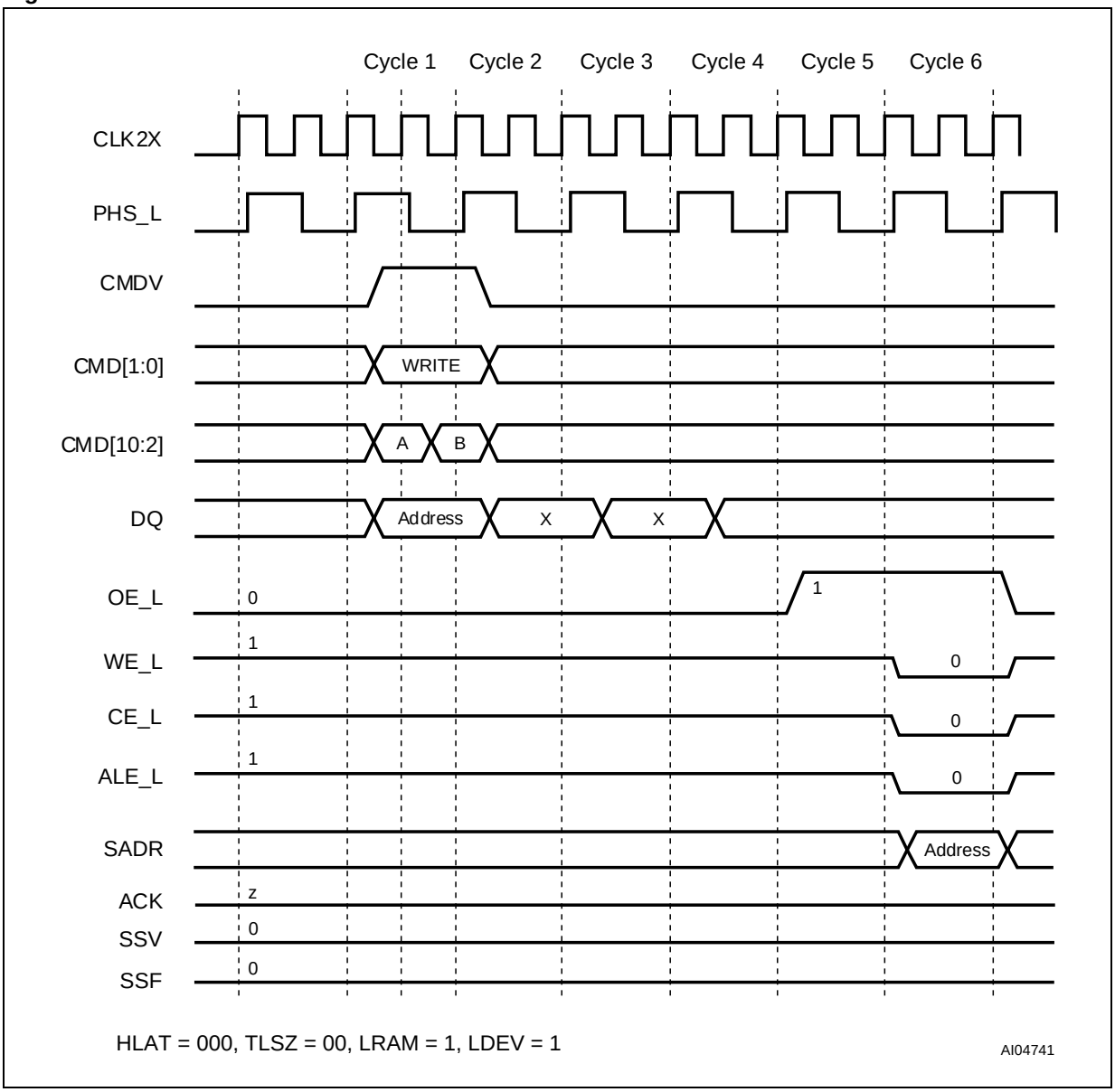
  Note: CMD[2] must be set to '0' for SRAM WRITE because Burst WRITEs into the SRAM are not supported.

– **Cycle 2:** The host ASIC continues to drive DQ[71:0]. The data in this cycle is not used by the M7040N device.

– **Cycle 3:** The host ASIC continues to drive DQ[71:0]. The data in this cycle is not used by the M7040N device.

At the end of Cycle 3, a new command can begin. The WRITE is a pipelined operation. The WRITE Cycle appears at the SRAM Bus, however, with the same latency as that of a SEARCH Instruction, as measured from the second cycle of the WRITE command.

Figure 103. SRAM WRITE Access for One Device



SRAM WRITE with a Table of Up to Eight Devices

The following explains the SRAM WRITE operation done through a table(s) of up to eight devices with the following parameters (TLSZ = 01). The diagram of such a table is shown in Figure 104, page 141.

The following assumes that SRAM access is done through M7040N Device 0. Figure 105, page 142 and Figure 106, page 143 show the timing diagram for Device 0 and Device 7, respectively.

– **Cycle 1A:** The host ASIC applies the WRITE Instruction on CMD[1:0] using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. The host ASIC also supplies SADR[23:21] on CMD[8:6] in this cycle.

  Note: CMD[2] must be set to '0' for SRAM WRITE because Burst WRITEs into the SRAM are not supported.

– **Cycle 1B:** The host ASIC continues to apply the WRITE Instruction on CMD[1:0] using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address.

  Note: CMD[2] must be set to '0' for SRAM WRITE because Burst WRITEs into the SRAM are not supported.

– **Cycle 2:** The host ASIC continues to drive DQ[71:0]. The data in this cycle is not used by the M7040N device.

– **Cycle 3:** The host ASIC continues to drive DQ[71:0]. The data in this cycle is not used by the M7040N device.

At the end of cycle 3, a new command can begin. The WRITE is a pipelined operation. The WRITE Cycle appears at the SRAM Bus, however, with the same latency as that of a SEARCH Instruction, as measured from the second cycle of the WRITE command.

Figure 104. Table with Eight Devices

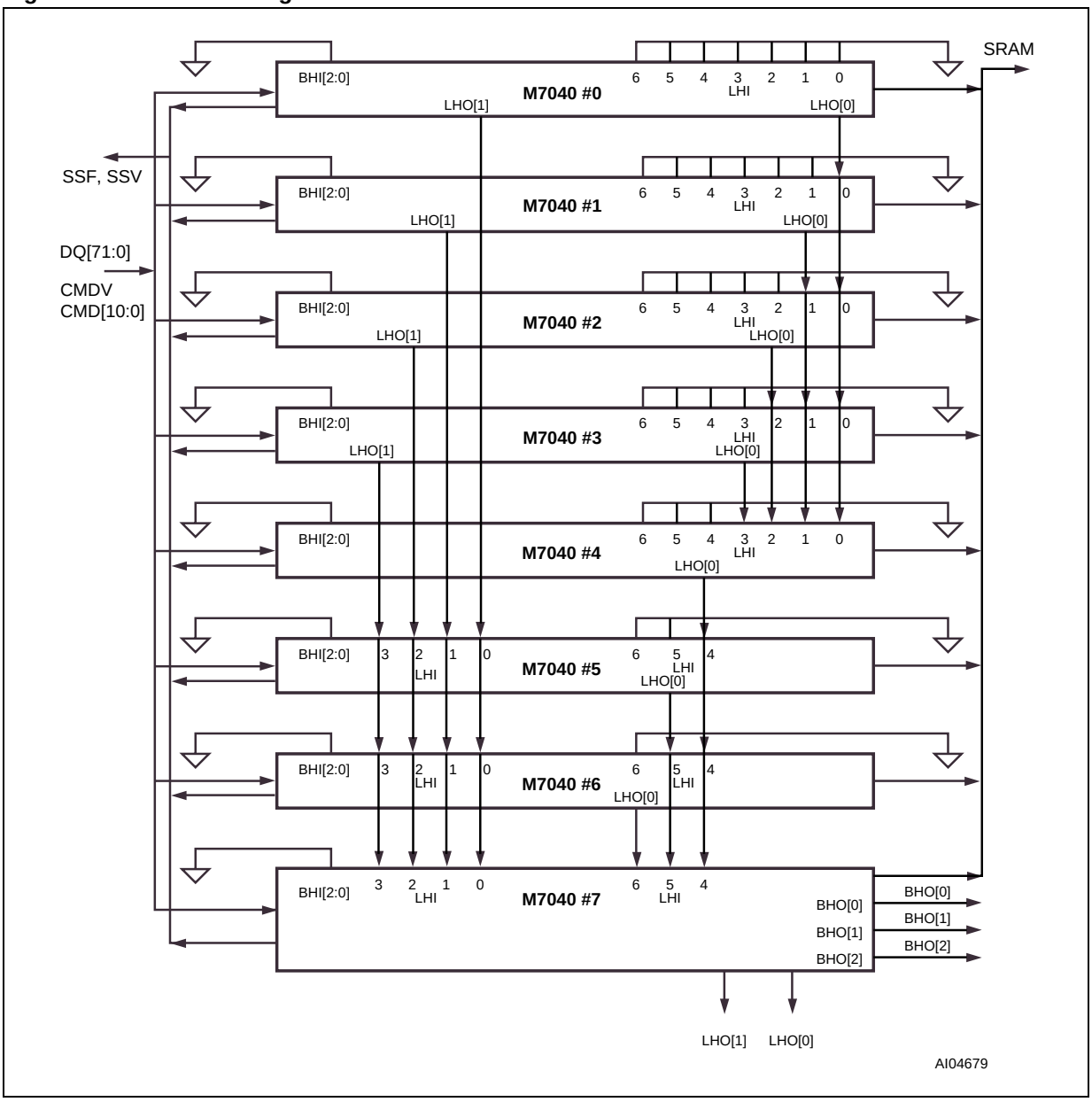


Figure 105. SRAM WRITE Through Device 0 in a Block of Eight Devices

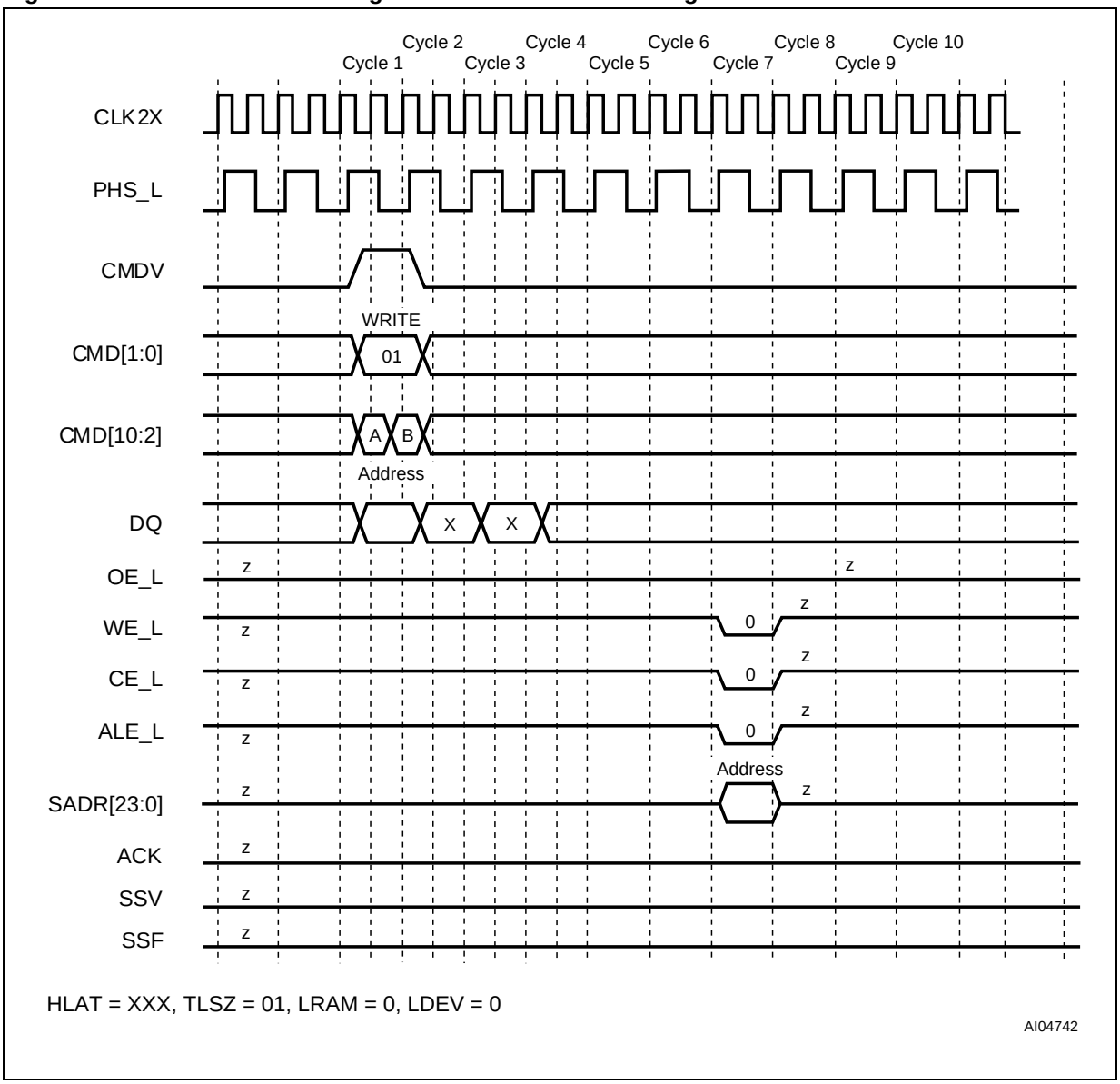
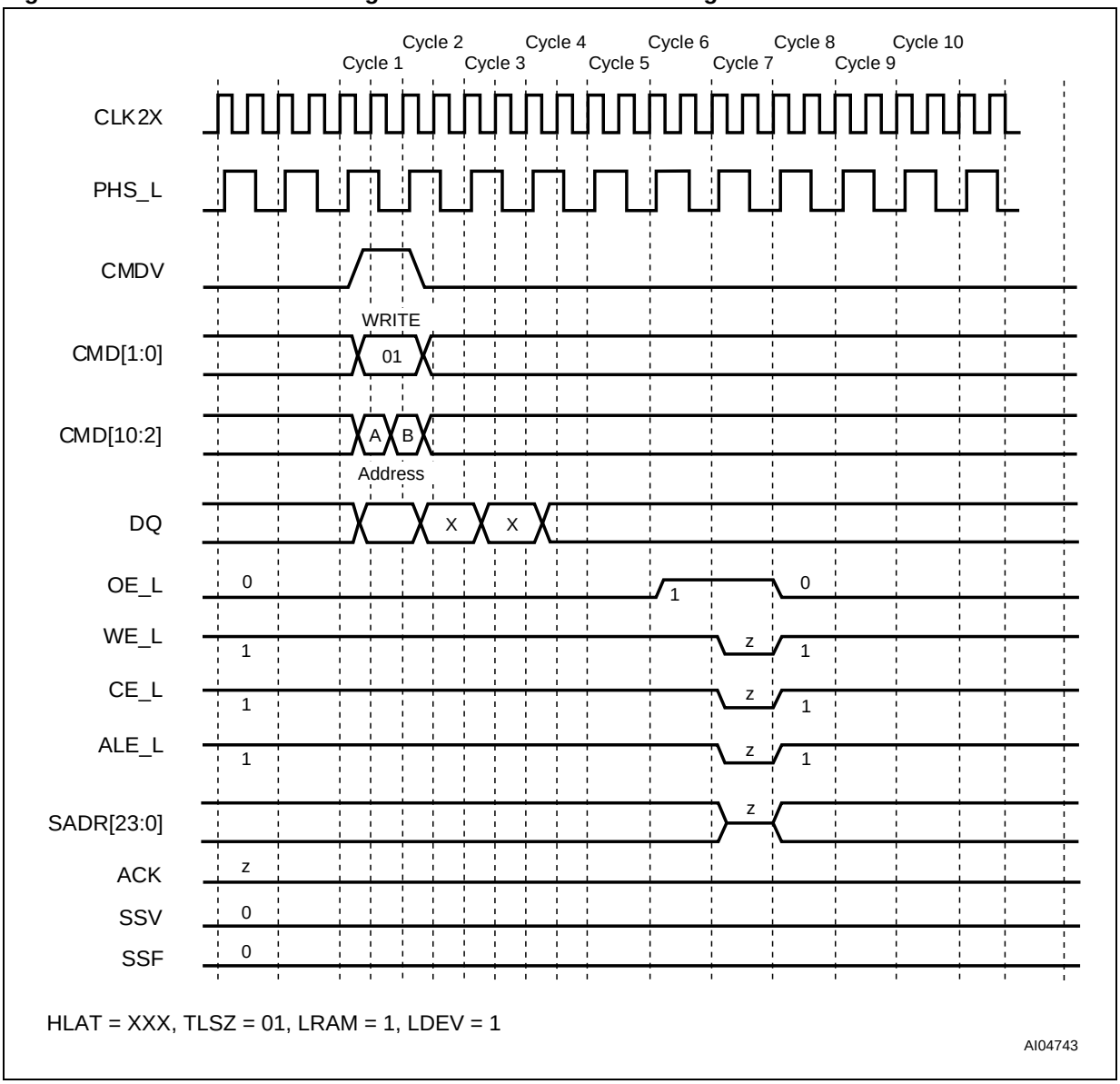


Figure 106. SRAM WRITE Timing for Device 7 in a Block of Eight Devices



SRAM WRITE with Table(s) of Up to 31 Devices

The following explains the SRAM WRITE operation done through a table(s) of up to 31 devices with the following parameters (TLSZ = 10). The diagram of such table(s) is shown in Figure 107, page 145. The following assumes that SRAM access is done through M7040N Device 0 – Device 0 is the selected device. Figure 108, page 146 and Figure 109, page 147 show the timing diagram for Device 0 and Device 30, respectively.

– **Cycle 1A:** The host ASIC applies the WRITE Instruction on CMD[1:0] using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. The host ASIC also supplies SADR[23:21] on CMD[8:6] in this cycle.

  Note: CMD[2] must be set to '0' for SRAM WRITE because Burst WRITEs into the SRAM are not supported.

– **Cycle 1B:** The host ASIC continues to apply the WRITE Instruction on CMD[1:0] using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address.

  Note: CMD[2] must be set to '0' for SRAM WRITE because Burst WRITEs into the SRAM are not supported.

– **Cycle 2:** The host ASIC continues to drive DQ[71:0]. The data in this cycle is not used by the M7040N device.

– **Cycle 3:** The host ASIC continues to drive DQ[71:0]. The data in this cycle is not used by the M7040N device.

At the end of Cycle 3, a new command can begin. The WRITE is a pipelined operation. The WRITE Cycle appears at the SRAM Bus, however, with the same latency as that of a SEARCH Instruction, as measured from the second cycle of the WRITE command

Figure 107. Table of 31 Devices (Four Blocks)

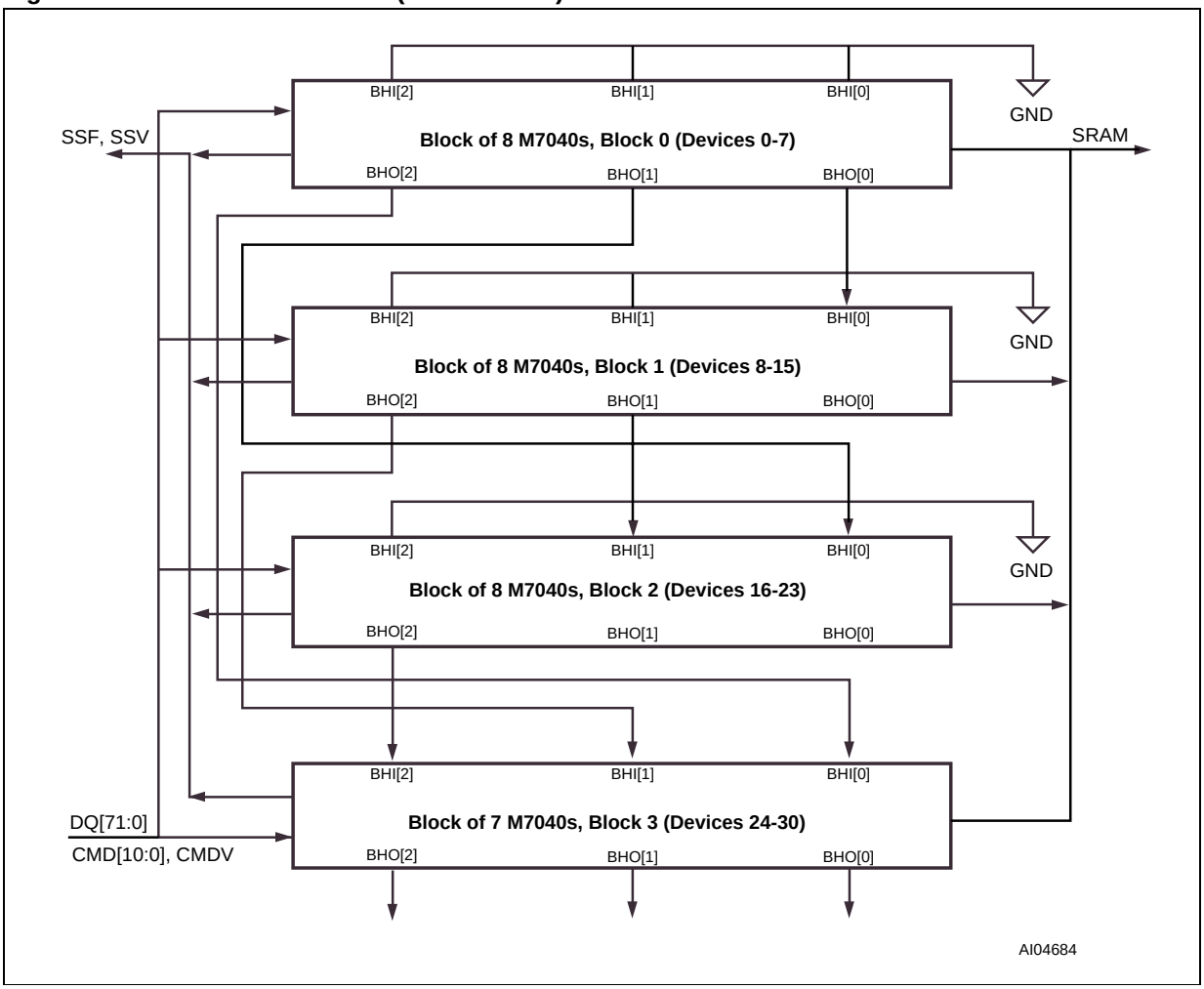


Figure 108. SRAM WRITE Through Device 0 in a Bank of 31 Devices (Device 0 Timing)

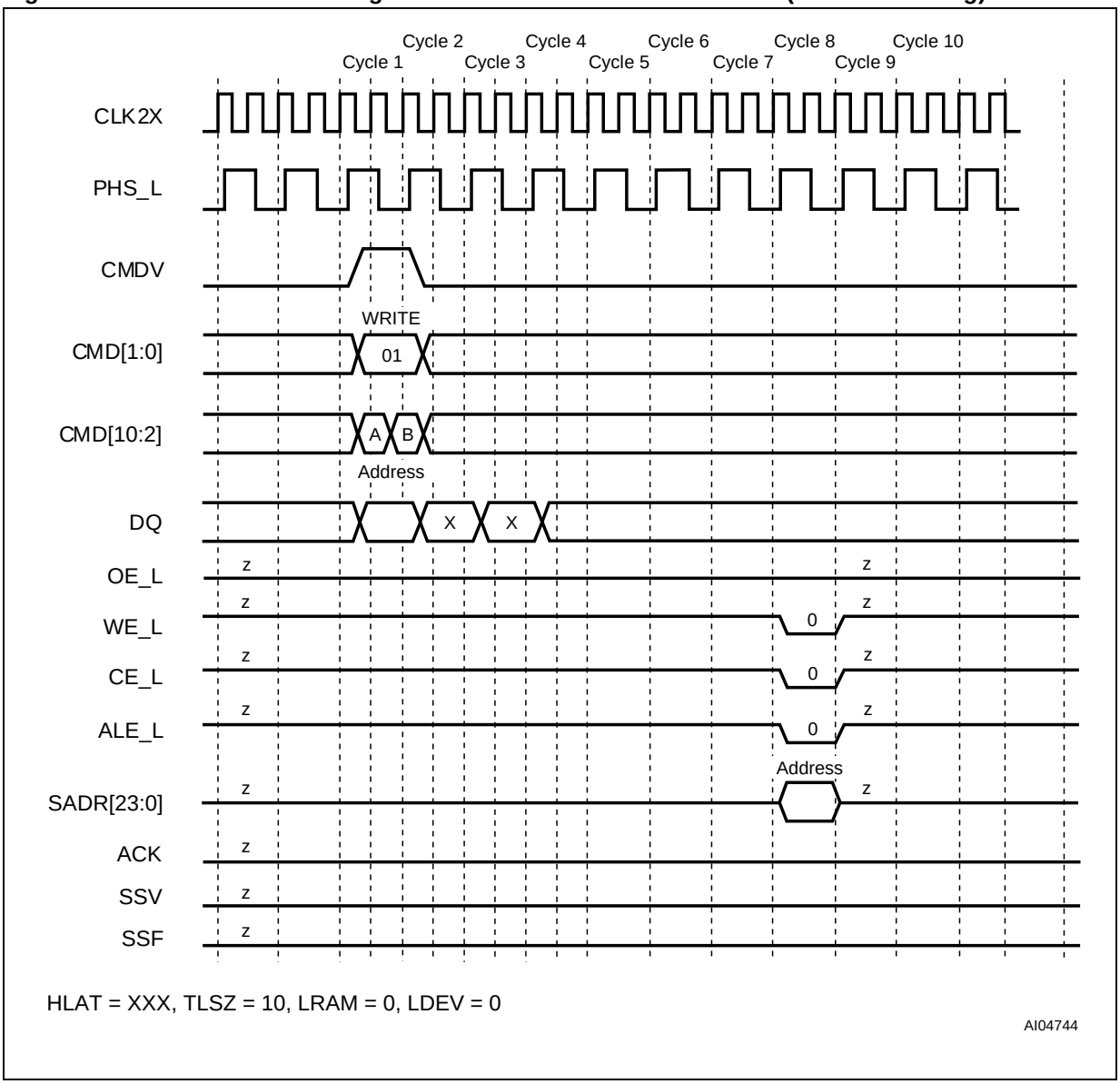
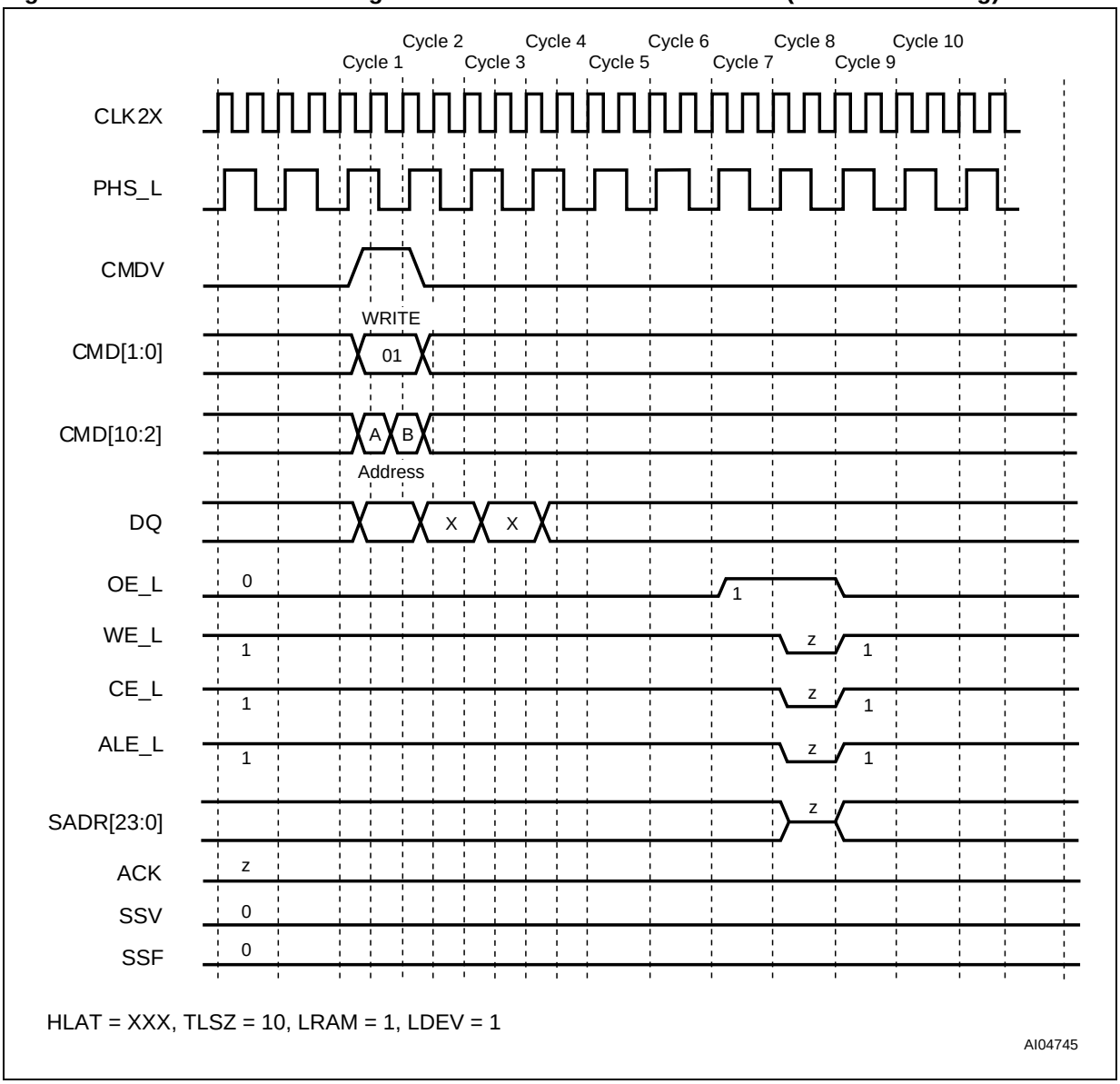


Figure 109. SRAM WRITE Through Device 0 in a Bank of 31 Devices (Device 30 Timing)



JTAG (1149.1) TESTING

The M7040N supports the Test Access Port and Boundary Scan Architecture as specified in the IEEE JTAG standard 1149.1. The pin interface to the chip consists of five signals with the standard definitions: TCK, TMS, TDI, TDO, and TRST_L. Table 53 describes the operations that the test access port controller supports and Table 54 describes the TAP Device ID Register.

Note: To disable JTAG functionality, connect the TCK, TMS, and TDI pins to Ground, and TRST_L to V_{DD}.

Table 53. Supported Operations

Instruction	Type	Description
SAMPLE/PRELOAD	Mandatory	**Sample/Preload.** Loads the values of signals going to and from IO pins into the boundary scan shift register to provide a snapshot of the normal functional operation.
EXTEST	Mandatory	**External Test.** Uses boundary scan values shifted in from TAP to test connectivity external to the device.
INTEST	Optional	**Internal Test.** Allows slow-speed, functional testing of the device using the boundary scan register to provide the I/O values.

Table 54. TAP Device ID Register

Field	Range	Initial Value	Description
Revision	[31:28]	0001	**Revision Number.** This is the current device revision number. Numbers start from one and increment by one for each revision of the device.
Part #	[27:12]	0000 0000 0000 0100	This is the part number for this device.
MFID	[11:1]	000_1101_1100	**Manufacturer ID.** This field is the same as the manufacturer ID used in the TAP controller.
LSB	[0]	1	Least Significant Bit

PART NUMBERING

Table 55. Ordering Information Scheme

Example: M70 40 N –100 ZA 1 T

Device Type

M70 Search Engine

Density

40 = 4.5Mb (64K x 72-bit Table Entries)

Operating Supply Voltage

N = V_{DD} = 1.5V for –066 and –083 speed grades

V_{DD} = 1.65V for –100 speed grade

Speed

–100 = 100 Million Searches per Second

–083 = 83 Million Searches per Second

–066 = 66 Million Searches per Second

Package

PBGA = 388-ball count, 35mm x 35mm(1), 1.27mm ball pitch

Temperature Range

1 = 0 to 70°C

Shipping Option

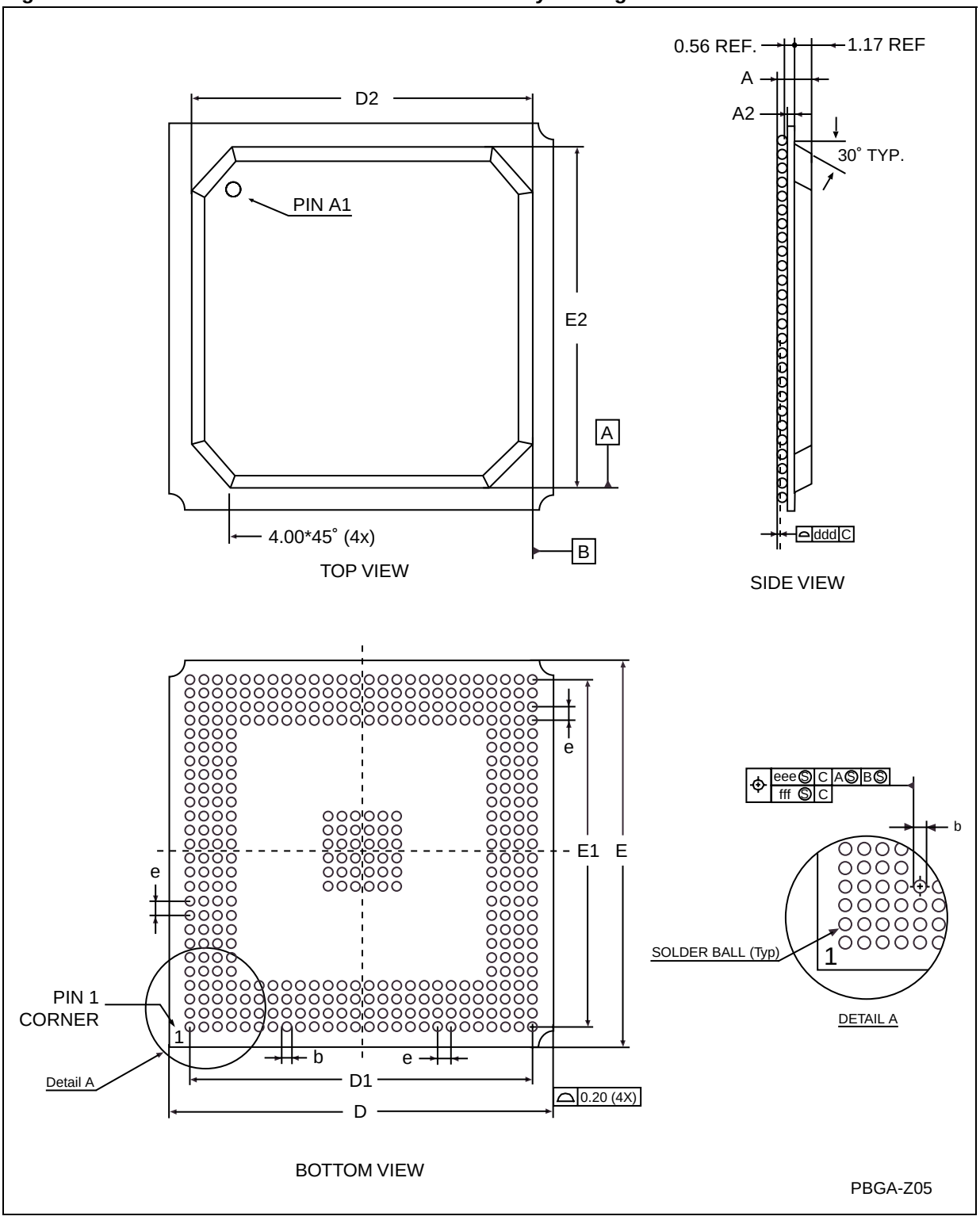
Tape & Reel Packing = T

Note: 1. Where “Z” is the symbol for BGA packages and “A” denotes 1.27mm ball pitch

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

PACKAGE MECHANICAL INFORMATION

Figure 110. PBGA-ZA – 388-ball Plastic Ball Grid Array Package Outline



Note: Drawing is not to scale.

Table 56. PBGA-ZA – 388-ball Plastic Ball Grid Array Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	2.33	2.20	2.46	0.095	0.090	0.100
A2	0.56			0.022		
b(1,2)	0.75	0.60	0.90	0.031	0.024	0.037
D(3,4)	35.00	34.80	35.20	1.429	1.420	1.437
D1	31.75			1.296		
D2	30.00			1.224		
E(3,4)	35.00	34.80	35.20	1.429	1.420	1.437
e	1.27			0.050		
E1	31.75			1.296		
E2	30.00			1.224		
n	388			388		
	Tolerance			Tolerance		
ddd			0.15			0.006
eee			0.30			0.012
fff			0.15			0.006

Note: 1. The terminal “b” corner must be identified on the top surface by using a corner chamfer, ink, or metallized markings, or other feature of package body or integral heatslug.
2. A distinguished feature is allowable on the bottom surface of the package to identify the terminal “b” corner.
3. Maximum mounted height is 2.45mm based on a 0.65mm ball pad diameter. Solder paste is 0.15mm thickness and 0.65mm in diameter.
4. Exact shape of each corner is optional.

APPENDIX

APPENDIX A. DESCRIPTIONS FOR CONNECTION DIAGRAM (FIGURE 3, PAGE 9)

Table 57. Connections

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
A1	CLK_TUNE[3](1)	Note 1	AA26	CMD[2]	Input
A10	DQ[43]	I/O	AA3	V_{DD}	1.5V
A11	DQ[41]	I/O	AA4	V_{SS}	Ground
A12	DQ[37]	I/O	AB1	FULL	Output-T
A13	DQ[35]	I/O	AB2	ACK	Output-T
A14	DQ[31]	I/O	AB23	VSS	Ground
A15	V_{DDQ}(2)	2.5/3.3V	AB24	V_{DD}	1.5V
A16	DQ[25]	I/O	AB25	CMD[5]	Input
A17	DQ[21]	I/O	AB26	CMD[4]	Input
A18	DQ[17]	I/O	AB3	V_{DD}	1.5V
A19	V_{DDQ}(2)	2.5/3.3V	AB4	V_{SS}	Ground
A2	DQ[71]	I/O	AC1	V_{SS}	Ground
A20	DQ[09]	I/O	AC10	V_{SS}	Ground
A21	DQ[05]	I/O	AC11	V_{DD}	1.5V
A22	DQ[03]	I/O	AC12	V_{DD}	1.5V
A23	TEST_FM	Ground	AC13	V_{DD}	1.5V
A24	V_{DDQ}(2)	2.5/3.3V	AC14	V_{DD}	1.5V
A25	HIGH_SPEED	Input	AC15	V_{DD}	1.5V
A26	CLK_TUNE[0](1)	Note 1	AC16	V_{DD}	1.5V
A3	V_{DDQ}(2)	2.5/3.3V	AC17	V_{SS}	Ground
A4	DQ[67]	I/O	AC18	V_{SS}	Ground
A5	DQ[63]	I/O	AC19	V_{SS}	Ground
A6	V_{DDQ}(2)	2.5/3.3V	AC2	EOT	Output-T
A7	DQ[57]	I/O	AC20	V_{SS}	Ground
A8	DQ[53]	I/O	AC21	V_{SS}	Ground
A9	DQ[51]	I/O	AC22	V_{SS}	Ground
AA1	FULO[1]	Output-T	AC23	V_{SS}	Ground
AA2	V_{DDQ}(2)	2.5/3.3V	AC24	V_{DD}	1.5V
AA23	VSS	Ground	AC25	CMD[6]	Input

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
AA24	V_{DD}	1.5V	AC26	V_{DDQ}(2)	2.5/3.3V
AA25	CMD[3]	Input	AC3	V_{DD}	1.5V
AC4	V_{SS}	Ground	AE10	DQ[44]	I/O
AC5	V_{SS}	Ground	AE11	DQ[42]	I/O
AC6	V_{SS}	Ground	AE12	DQ[38]	I/O
AC7	V_{SS}	Ground	AE13	V_{DDQ}(2)	2.5/3.3V
AC8	V_{SS}	Ground	AE14	DQ[32]	I/O
AC9	V_{SS}	Ground	AE15	DQ[28]	I/O
AD1	RST_L	Input	AE16	DQ[26]	I/O
AD10	DQ[46]	I/O	AE17	V_{DDQ}(2)	2.5/3.3V
AD11	V_{DD}	1.5V	AE18	DQ[18]	I/O
AD12	V_{DD}	1.5V	AE19	DQ[12]	I/O
AD13	V_{DD}	1.5V	AE2	V_{SS}	Ground
AD14	V_{DD}	1.5V	AE20	DQ[10]	I/O
AD15	V_{DD}	1.5V	AE21	DQ[06]	I/O
AD16	V_{DD}	1.5V	AE22	V_{DDQ}(2)	2.5/3.3V
AD17	DQ[20]	I/O	AE23	DQ[00]	I/O
AD18	DQ[16]	I/O	AE24	V_{DDQ}(2)	2.5/3.3V
AD19	NC4	No Connect	AE25	V_{SS}	Ground
AD2	V_{DDQ}(2)	2.5/3.3V	AE26	CLK_TUNE[1](1)	Note 1
AD20	V_{DD}	1.5V	AE3	DQ[70]	I/O
AD21	V_{DD}	1.5V	AE4	V_{DDQ}(2)	2.5/3.3V
AD22	V_{DD}	1.5V	AE5	DQ[64]	I/O
AD23	V_{DD}	1.5V	AE6	DQ[60]	I/O
AD24	V_{DD}	1.5V	AE7	DQ[58]	I/O
AD25	CMD[8]	Input	AE8	DQ[54]	I/O
AD26	CMD[7]	Input	AE9	DQ[50]	I/O
AD3	V_{DD}	1.5V	AF1	TEST_CO	No Connect
AD4	V_{DD}	1.5V	AF10	V_{DDQ}(2)	2.5/3.3V
AD5	V_{DD}	1.5 V	AF11	DQ[40]	I/O
AD6	V_{DD}	1.5V	AF12	DQ[36]	I/O
AD7	V_{DD}	1.5V	AF13	DQ[34]	I/O
AD8	NC3	No Connect	AF14	DQ[30]	I/O
AD9	V_{DDQ}(2)	2.5/3.3V	AF15	V_{DDQ}(2)	2.5/3.3V

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
AE1	TEST	Ground	AF16	DQ[24]	I/O
AF17	DQ[22]	I/O	B23	TEST_PB	Input
AF18	DQ[14]	I/O	B24	CFG_L	Input
AF19	V_{DDQ}(2)	2.5/3.3V	B25	V_{SS}	Ground
AF2	CLK_TUNE[2](1)	Note 1	B26	SADR[00]	Output
AF20	DQ[08]	I/O	B3	DQ[69]	I/O
AF21	DQ[04]	I/O	B4	DQ[65]	I/O
AF22	DQ[02]	I/O	B5	DQ[61]	I/O
AF23	SSV	Output-T	B6	DQ[59]	I/O
AF24	SSF	Output-T	B7	DQ[55]	I/O
AF25	CMD[10]	Input	B8	V_{DDQ}(2)	2.5/3.3V
AF26	CMD[9]	Input	B9	DQ[47]	I/O
AF3	DQ[68]	I/O	C1	TCK	Input
AF4	DQ[66]	I/O	C10	V_{DDQ}(2)	2.5/3.3V
AF5	DQ[62]	I/O	C11	V_{DD}	1.5V
AF6	V_{DDQ}(2)	2.5/3.3V	C12	V_{DD}	1.5V
AF7	DQ[56]	I/O	C13	V_{DD}	1.5V
AF8	DQ[52]	I/O	C14	V_{DD}	1.5V
AF9	DQ[48]	I/O	C15	V_{DD}	1.5V
B1	TDI	Input	C16	V_{DD}	1.5V
B10	DQ[45]	I/O	C17	DQ[19]	I/O
B11	DQ[39]	I/O	C18	DQ[13]	I/O
B12	V_{DDQ}(2)	2.5/3.3V	C19	NC7	No Connect
B13	DQ[33]	I/O	C2	TMS	Input
B14	DQ[29]	I/O	C20	V_{DD}	1.5V
B15	DQ[27]	I/O	C21	V_{DD}	1.5V
B16	DQ[23]	I/O	C22	V_{DD}	1.5V
B17	V_{DDQ}(2)	2.5/3.3V	C23	V_{DD}	1.5V
B18	DQ[15]	I/O	C24	V_{DD}	1.5V
B19	DQ[11]	I/O	C25	SADR[01]	Output
B2	V_{SS}	Ground	C26	V_{DDQ}(2)	2.5/3.3V
B20	DQ[07]	I/O	C3	V_{DD}	1.5V
B21	V_{DDQ}(2)	2.5/3.3V	C4	V_{DD}	1.5V
B22	DQ[01]	I/O	C5	V_{DD}	1.5V

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
C6	V_{DD}	1.5V	E24	V_{DD}	1.5V
C7	V_{DD}	1.5V	E25	SADR[05]	Output
C8	NC8	No Connect	E26	SADR[04]	Output
C9	DQ[49]	I/O	E3	V_{DD}	1.5V
D1	TRST_L	Input	E4	V_{SS}	Ground
D10	VSS	Ground	F1	ID[1]	Input
D11	V_{DD}	1.5V	F2	ID[2]	Input
D12	V_{DD}	1.5V	F23	V_{SS}	Ground
D13	V_{DD}	1.5V	F24	V_{DD}	1.5V
D14	V_{DD}	1.5V	F25	SADR[06]	Output
D15	V_{DD}	1.5V	F26	V_{DDQ}(2)	2.5/3.3V
D16	V_{DD}	1.5V	F3	V_{DD}	1.5V
D17	V_{SS}	Ground	F4	V_{SS}	Ground
D18	V_{SS}	Ground	G1	ID[3]	Input
D19	V_{SS}	Ground	G2	ID[4]	Input
D2	TDO	Output-T	G23	V_{SS}	Ground
D20	V_{SS}	Ground	G24	V_{DD}	1.5V
D21	V_{SS}	Ground	G25	SADR[08]	Output
D22	V_{SS}	Ground	G26	SADR[07]	Output
D23	V_{SS}	Ground	G3	V_{DD}	1.5V
D24	V_{DD}	1.5V	G4	V_{SS}	Ground
D25	SADR[03]	Output	H1	LHI[0]	Input
D26	SADR[02]	Output	H2	LHI[1]	Input
D3	V_{DD}	1.5V	H23	V_{SS}	Ground
D4	V_{SS}	Ground	H24	NC6	No Connect
D5	V_{SS}	Ground	H25	V_{DDQ}(2)	2.5/3.3V
D6	V_{SS}	Ground	H26	SADR[09]	Output
D7	V_{SS}	Ground	H3	NC1	No Connect
D8	V_{SS}	Ground	H4	V_{SS}	Ground
D9	V_{SS}	Ground	J1	LHI[2]	Input
E1	ID[0]	Input	J2	LHI[3]	Input
E2	V_{DDQ}(2)	2.5/3.3V	J23	V_{SS}	Ground
E23	V_{SS}	Ground	J24	SADR[11]	Output
J25	SADR[12]	Output	M2	BHI[0]	Input

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
J26	SADR[10]	Output	M23	V_{DD}	1.5V
J3	V_{DDQ}(2)	2.5/3.3V	M24	V_{DD}	1.5V
J4	V_{SS}	Ground	M25	V_{DDQ}(2)	2.5/3.3V
K1	LHI[6]	Input	M26	SADR[17]	Output
K2	LHI[4]	Input	M3	V_{DD}	1.5V
K23	V_{SS}	Ground	M4	V_{DD}	1.5V
K24	SADR[13]	Output	N1	BHI[1]	Input
K25	V_{DDQ}(2)	2.5/3.3V	N11	V_{SS}	Ground
K26	SADR[14]	Output	N12	V_{SS}	Ground
K3	LHI[5]	Input	N13	V_{SS}	Ground
K4	V_{SS}	Ground	N14	V_{SS}	Ground
L1	LHO[0]	Output-T	N15	V_{SS}	Ground
L11	V_{SS}	Ground	N16	V_{SS}	Ground
L12	V_{SS}	Ground	N2	BHI[2]	Input
L13	V_{SS}	Ground	N23	V_{DD}	1.5V
L14	V_{SS}	Ground	N24	V_{DD}	1.5V
L15	V_{SS}	Ground	N25	SADR[19]	Output
L16	V_{SS}	Ground	N26	SADR[18]	Output
L2	LHO[1]	Output-T	N3	V_{DD}	1.5V
L23	V_{DD}	1.5V	N4	V_{DD}	1.5V
L24	V_{DD}	1.5V	P1	BHO[0]	Output-T
L25	SADR[15]	Output	P11	V_{SS}	Ground
L26	SADR[16]	Output	P12	V_{SS}	Ground
L3	V_{DD}	1.5V	P13	V_{SS}	Ground
L4	V_{DD}	1.5V	P14	V_{SS}	Ground
M1	V_{DDQ}(2)	2.5/3.3V	P15	V_{SS}	Ground
M11	V_{SS}	Ground	P16	V_{SS}	Ground
M12	V_{SS}	Ground	P2	MULTI_HIT	Output-T
M13	V_{SS}	Ground	P23	V_{DD}	1.5V
M14	V_{SS}	Ground	P24	V_{DD}	1.5V
M15	V_{SS}	Ground	P25	SADR[21]	Output
M16	V_{SS}	Ground	P26	SADR[20]	Output
P3	V_{DD}	1.5V	U24	OE_L	Output-T
P4	V_{DD}	1.5V	U25	PHS_L	Input

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
R1	V_{DDQ}(2)	2.5/3.3V	U26	CLK1X/CLK2X	Input
R11	V_{SS}	Ground	U3	FULI[1]	Input
R12	V_{SS}	Ground	U4	V_{SS}	Ground
R13	V_{SS}	Ground	V1	FULI[2]	Input
R14	V_{SS}	Ground	V2	FULI[3]	Input
R15	V_{SS}	Ground	V23	V_{SS}	Ground
R16	V_{SS}	Ground	V24	CE_L	Output-T
R2	BHO[1]	Output-T	V25	V_{DDQ}(2)	2.5/3.3V
R23	V_{DD}	1.5V	V26	WE_L	Output-T
R24	V_{DD}	1.5V	V3	FULI[4]	Input
R25	SADR[22]	Output	V4	V_{SS}	Ground
R26	V_{DDQ}(2)	2.5/3.3V	W1	V_{DDQ}(2)	2.5/3.3V
R3	V_{DD}	1.5V	W2	FULI[5]	Input
R4	V_{DD}	1.5V	W23	V_{SS}	Ground
T1	BHO[2]	Output-T	W24	NC5	No Connect
T11	V_{SS}	Ground	W25	CMDV	Input
T12	V_{SS}	Ground	W26	ALE_L	Output-T
T13	V_{SS}	Ground	W3	NC2	No Connect
T14	V_{SS}	Ground	W4	V_{SS}	Ground
T15	V_{SS}	Ground	Y1	FULI[6]	Input
T16	V_{SS}	Ground	Y2	FULO[0]	Output-T
T2	V_{SS}	Ground	Y23	V_{SS}	Ground
T23	V_{DD}	1.5V	Y24	V_{DD}	1.5V
T24	V_{DD}	1.5V	Y25	CMD[1]	Input
T25	CLK_MODE	Input	Y26	CMD[0]	Input
T26	SADR[23]	Output	Y3	V_{DD}	1.5V
T3	V_{DD}	1.5V	Y4	V_{SS}	Ground
T4	V_{DD}	1.5V			
U1	FULI[0]	Input			
U2	V_{DDQ}(2)	2.5/3.3V			
U23	V_{SS}	Ground			

Note: 1. CLK_TUNE[3:0] should be programmed to 100%.
2. All V_{DDQ} pins should be set to 2.5 or 3.3V.

REVISION HISTORY

Table 58. Document Revision History

Date	Revision Details
April 2001	First Issue
07/23/01	Routine maintenance (based on recent data sheet review findings)
10/16/01	Addition of 1.8V data
10/29/01	Document promoted to “Preliminary Data;” V_{DDQ} corrected (Table 4)
04/03/02	Updates per engineering (Figure 3); (Table 1, 2, 3, 4, 6, 8, 55)
4/19/02	Improve Mechanical, Connection drawings (Figures 3, 110); change Register Overview (Table 9)
05/10/02	Modify Timing Diagrams (Figure 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 91, 99, 103)