

TV VERTICAL DEFLECTION BOOSTER

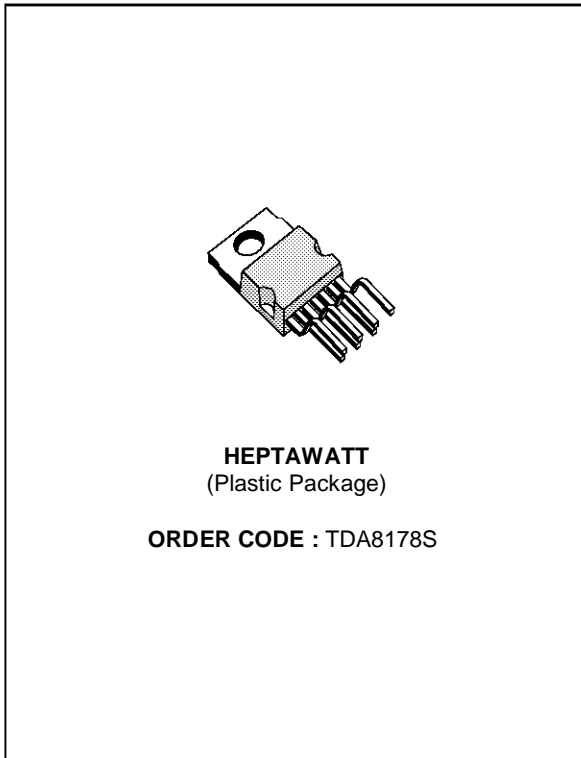
- POWER AMPLIFIER
- FLYBACK GENERATOR
- THERMAL PROTECTION
- REFERENCE VOLTAGE

DESCRIPTION

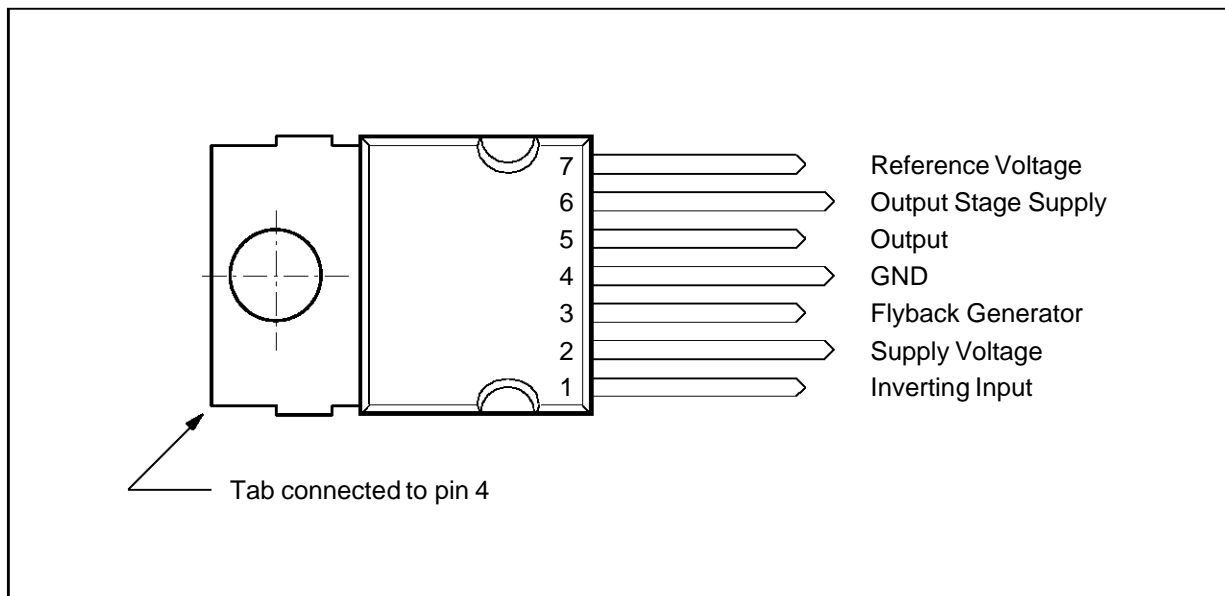
Designed for monitors and high performance TVs, the TDA8178S vertical deflection booster delivers flyback voltages up to 90V.

The TDA8178S operates with supplies up to 42V and provides up to 2App output current to drive to yoke.

The TDA8178S is offered in HEPTAWATT package



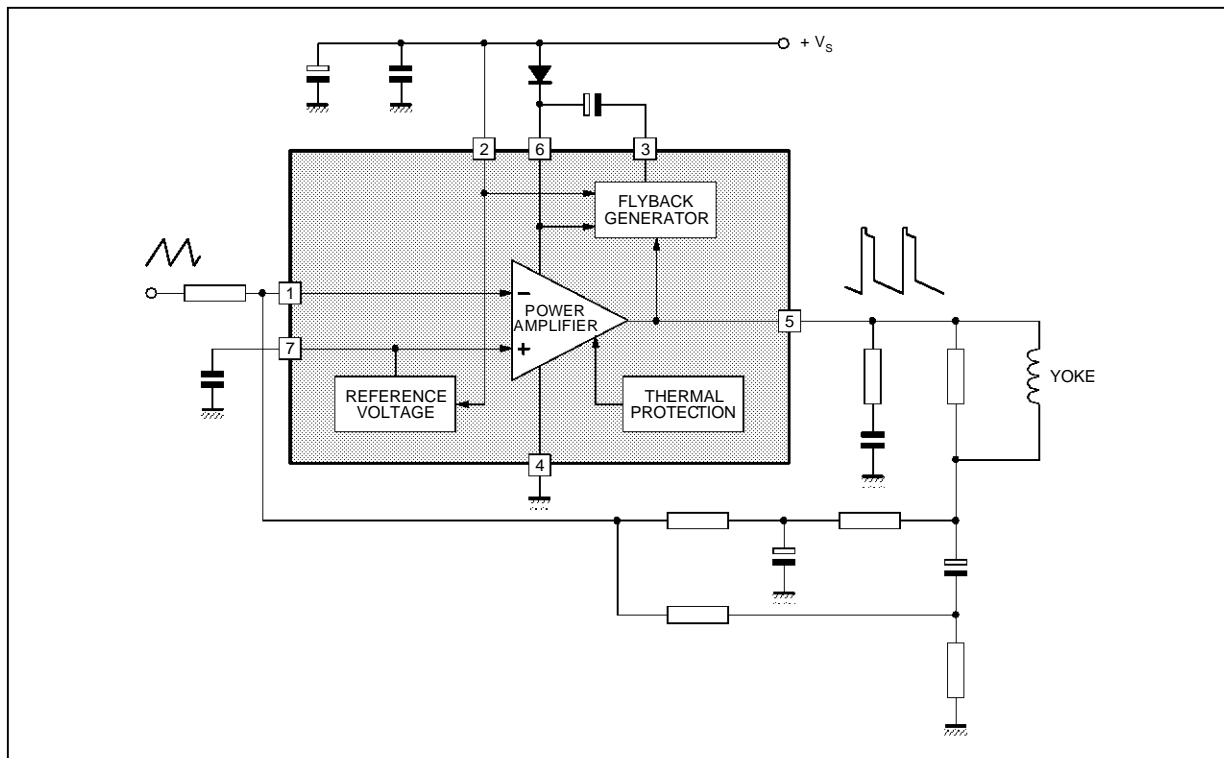
PIN CONNECTIONS



8178S-01.EPS

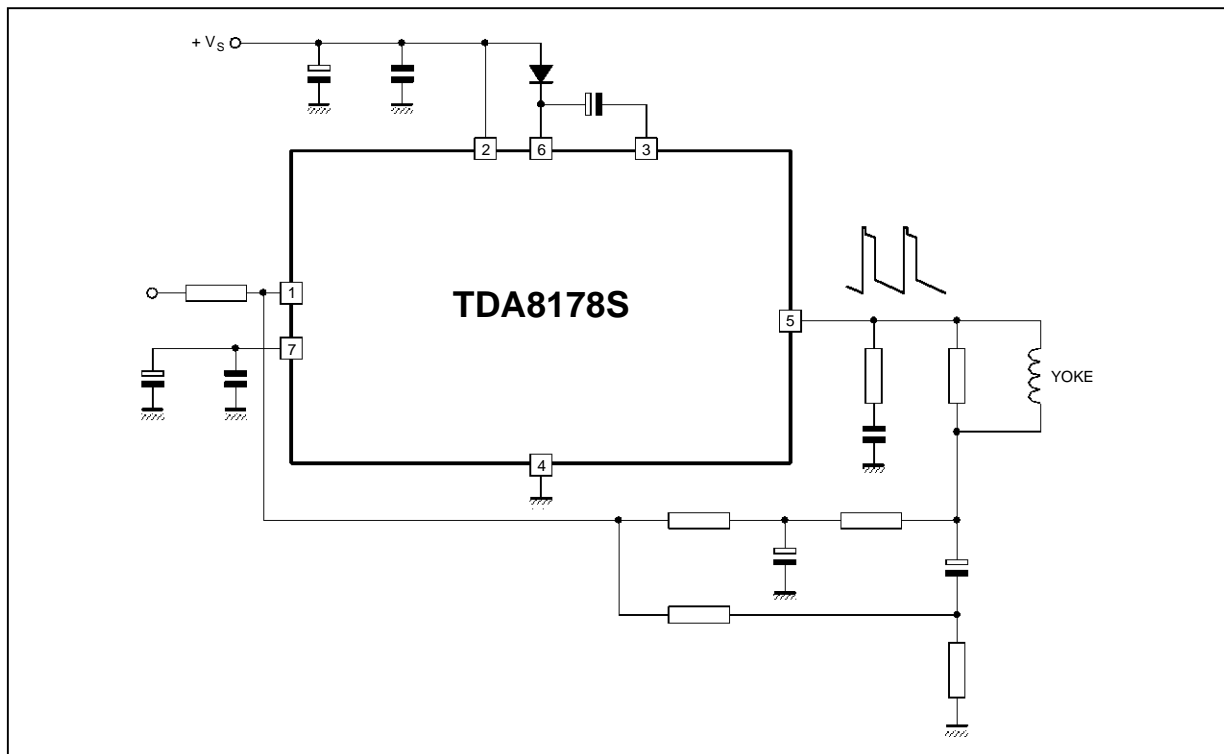
TDA8178S

BLOCK DIAGRAM



8178S-02.EPS

APPLICATION CIRCUIT ($V_s = 42V$)



8178S-03.EPS

Note : For values see "Easy Design of Vertical Deflection Stages" (software available from our sales offices)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _S	Supply Voltage (pin 2)	50	V
V ₅ , V ₆	Flyback Peak Voltage	100	V
V ₁ , V ₇	Amplifier Input Voltage	+ V _S	
I _O	Output Peak Current	2 2 1.8	A
I ₃	Pin 3 DC at V ₅ < V ₂ Pin 3 Peak Flyback Current at f = 50 or 60Hz, t _{fly} ≤ 1.5ms	100 1.8	mA A
P _{tot}	Total Power Dissipation at T _C = 70°C	20	W
T _{stg}	Storage Temperature	- 40, + 150	°C
T _j	Junction Temperature	0, +150	°C

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THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th(j-c)}	Junction-case Thermal Resistance	Max. 3	°C/W

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ELECTRICAL CHARACTERISTICS

(V_S = 42V, T_A = 25°C, unless otherwise specified) (refer to the test circuits - see Figure 1 next page)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _S	Operating Supply Voltage Range		10		42	V
I ₂	Pin 2 Quiescent Current	I ₃ = 0 I ₅ = 0		10	20	mA
I ₆	Pin 6 Quiescent Current	I ₃ = 0 I ₅ = 0		20	40	mA
I ₁	Amplifier Bias Current	V ₁ = 1V		- 0.2	- 1	µA
V _{3L}	Pin 3 Saturation to GND	I ₃ = 20mA		1.3	1.8	V
V ₅	Quiescent Output Voltage	V _S = 42V R _a = 3.9kΩ V _S = 35V R _a = 5.6kΩ	23.4 17	24.2 17.8	25 18.5	V
V _{5L}	Output Saturation Voltage to GND	I ₅ = 1A		1.2	1.5	V
V _{5H}	Output Saturation Voltage to Supply	- I ₅ = 1A		2.2	2.6	V
V _{D5-6}	Diode Forward Voltage between Pins 5-6	I _D = 1A		1.5	3	V
V _{D3-2}	Diode Forward Voltage between Pins 3-2	I _D = 1A		1.5	3	V
V ₇	Internal Reference		2.1	2.2	2.3	V
ΔV ₇ /ΔV _S	Reference Voltage Drift versus V _S	V _S = 24 to 42V		2	4	mV/V
K _T	Reference Voltage Drift versus T _j	T _j = 0 to 125°C $K_T = \frac{\Delta V_7 \cdot 10^6}{\Delta T_j \cdot V_7}$		100	150	ppm/°C
R ₁	Input Resistance			200		kΩ
T _j	Junction Temperature for Thermal Shutdown			140		°C

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TDA8178S

FIGURE 1 : DC Test Circuits

Figure 1a : Measurement of I_1 , I_2 , I_6 , V_7 , $\Delta V_7/\Delta V_s$

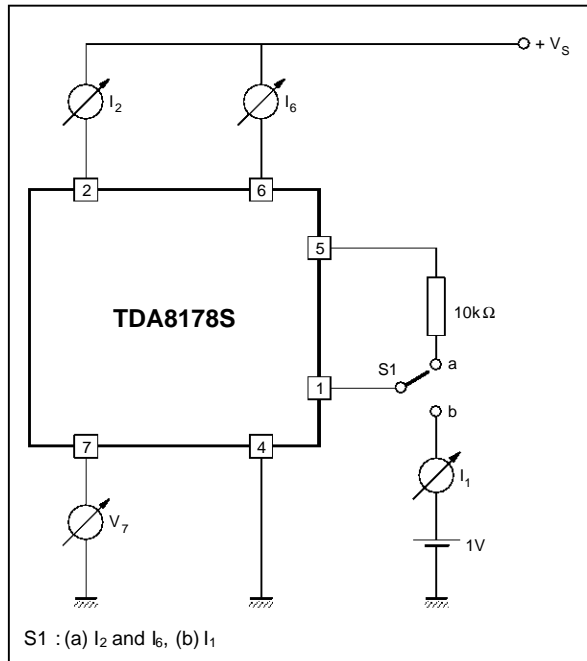


Figure 1b : Measurement of V_{5H}

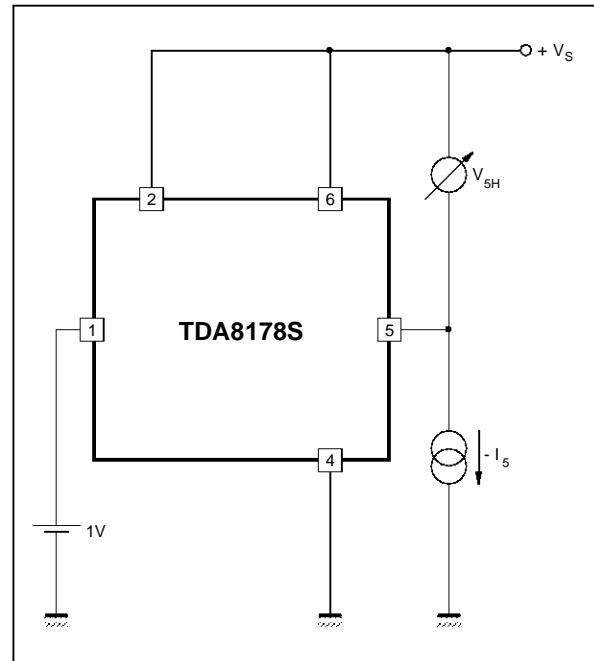


Figure 1c : Measurement of V_{3L} , V_{5L}

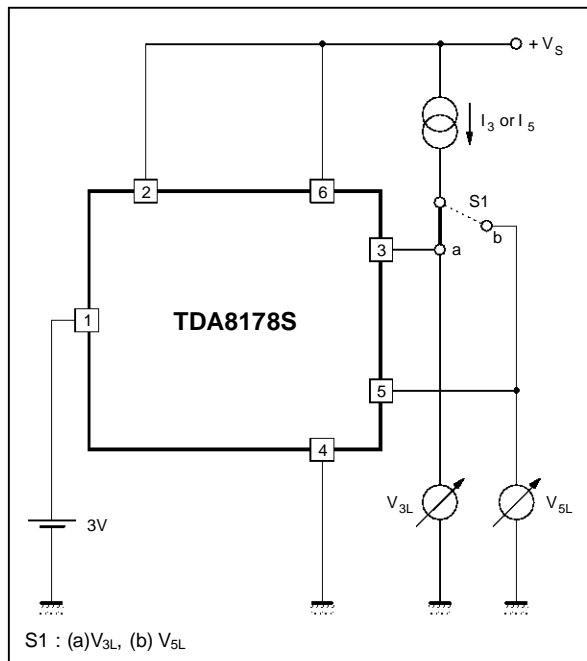


Figure 1d : Measurement of V_5

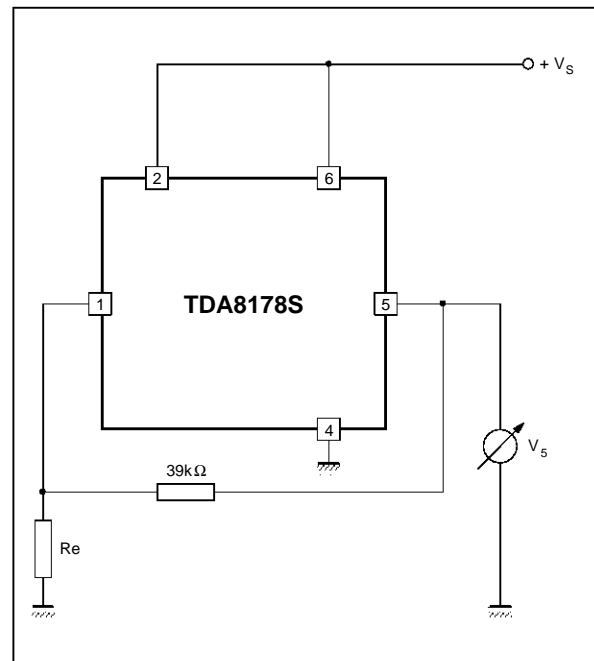
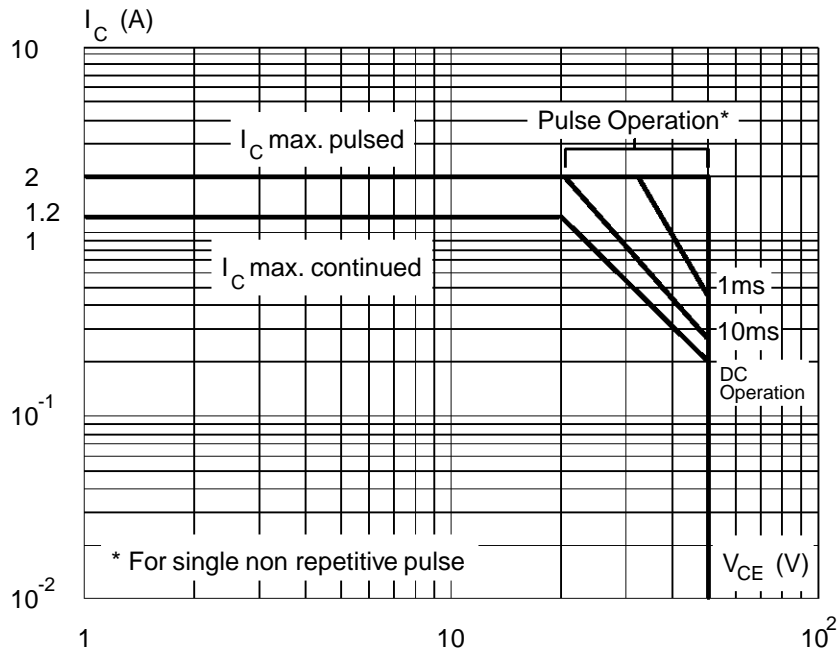
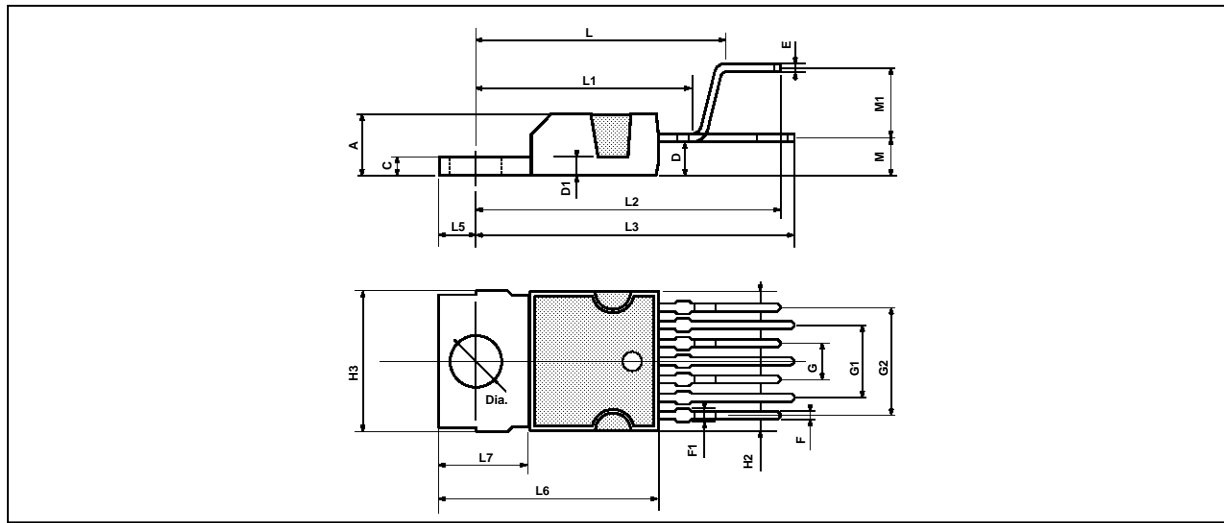


Figure 2 : SOA of Each Output Power Transistor at $T_A = 25^\circ\text{C}$



8178S-08.EPS

PACKAGE MECHANICAL DATA : HEPTAWATT



PM-HEPTV/EP5

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia.	3.65		3.85	0.144		0.152

HEPTV/TBL

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