

TS4985

2x1.2w Stereo Audio Power Amplifier with Dedicated Standby Pins PRODUCT PREVIEW

Pin Connections (top view)

- Operating from V_{CC}=2.2V to 5.5V
- 1.2W output power per channel @ V_{CC}=5V, THD+N=1%, RL=8Ω
- 10nA standby current
- 62dB PSRR @ 217Hz with Grounded inputs
- High SNR: 106dB(A) typ.
- Near Zero Pop & Click
- Lead-free 15 bumps flip-chip package

Description

The TS4985 has been designed for top of the class stereo audio applications. Thanks to its compact and power dissipation efficient flip-chip package, it suits various applications.

With a BTL configuration, this audio power amplifier is capable of delivering 1.2W per channel of continuous RMS Output Power into an 8Ω load @ 5V.

Each output channel (Left and Right), has an external controlled standby mode pin (STDBYL&STDBYR) to reduce the supply current to less than 10nA per channel. The device also features an internal thermal shutdown protection.

The gain of each channel can be configured by external gain setting resistors.

Applications

- Cellular mobile phones
- Notebook & PDA computers
- LCD monitors & TVs
- Portable audio devices

Order Codes

	Flip-C	Chip 15 bi	umps	
	Pin Con	nection (t	op view)	
(VCC1) (VO-L) (IN+L)	(VCc2) (V0+L) (IN+L)	STDBYL BYPASS STDBYR	(VO+R) (GND2)	(VO-R (VO-R)

Part Number Temperature Rang		Package	Packaging	Marking
TS4985EIJT ¹	40 495°C	Elin Chin	Tapa & Roal	
TS4985EIKJT ²	-40, 700 C	Flip-Chip	Tape & Reel	

1) **E** = Lead-free Flip-Chip

2) $K = Back \ coating \ option$

November 2004

Revision 1

This is preliminary information on a new product now in development. Details are subject to change without notice.

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1 Application Diagram

Figure 1 : Typical application schematics



Table 1: External Component Descriptions

Components	Functional Description
R _{IN L,R}	Inverting input resistors which sets the closed loop gain in conjunction with Rfeed. These resistors also form a high pass filter with C_{IN} (fc = 1 / (2 x Pi x R_{IN} x C_{IN}))
C _{IN L,R}	Input coupling capacitors which blocks the DC voltage at the amplifier input terminal
R _{FEED L,R}	Feedback resistors which sets the closed loop gain in conjunction with R_{IN}
C _S	Supply Bypass capacitor which provides power supply filtering
CB	Bypass pin capacitor which provides half supply filtering
A _{V L, R}	Closed loop gain in BTL configuration = $2 \times (R_{FEED} / R_{IN})$ on each channel

2 Absolute Maximum Ratings

Table 2: Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	Supply voltage ¹	6	V
Vi	Input Voltage ²	G_{ND} to V_{CC}	V
T _{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T _{stg}	Storage Temperature	-65 to +150	°C
Тj	Maximum Junction Temperature	150	°C
R _{thja}	Thermal Resistance Junction to Ambient	tba	°C/W
Pd	Power Dissipation	Internally Limited	
ESD	Human Body Model ³	2	kV
ESD	Machine Model	200	
	Latch-up Immunity	200mA	

1) All voltages values are measured with respect to the ground pin.

2) The magnitude of input signal must never exceed V_{CC} + 0.3V / G_{ND} - 0.3V.

3) All Voltage values are measured from each pin with respect to supplies.

Table 3: Operating Conditions

Symbol	Parameter	Value	Unit
VCC	Supply Voltage	2.2 to 5.5	V
V _{ICM}	Common Mode Input Voltage Range	1.2V to V _{CC}	V
VSTB	Standby Voltage Input: Device ON Device OFF	$1.35 \le V_{STB} \le V_{CC}$ GND $\le V_{STB} \le 0.4$	V
RL	Load Resistor	≥ 4	Ω
ROUT- GND	Resistor Output to GND (V _{STB} = GND)	≥ 1	MΩ
TSD	Thermal Shutdown Temperature	150	°C
RTHJA	Thermal Resistance Junction to Ambient Flip Chip ¹	tba	°C/W

1) When mounted on a 4-layer PCB.

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3 Electrical Characteristics

Table 4: V_{CC} = +5V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter		Тур.	Max.	Unit
I _{CC}	Supply Current No input signal, no load		7.4	12	mA
I _{STANDBY}	Standby Current ¹ No input signal, Vstdby = G_{ND} , RL = 8 Ω 10 1000		nA		
Voo	Output Offset Voltage No input signal, $RL = 8\Omega$ 110		mV		
Po	Output Power THD = 1% Max, F = 1kHz, RL = 8Ω	0.9	1.2		W
THD + N	Total Harmonic Distortion + Noise Po = 1Wrms, Av = 2, 20Hz \leq F \leq 20kHz, RL = 8 Ω		0.2	2 %	
PSRR	Power Supply Rejection Ratio ² RL = 8Ω , Av = 2, Vripple = 200mVpp, Input Grounded F = 217Hz F = 1kHz	55 55	62 64	dB	
Crosstalk	$ \begin{array}{c c} \mbox{Channel Separation, } R_L = 8\Omega \\ \mbox{F} = 1 \mbox{Hz} \\ \mbox{F} = 20 \mbox{Hz} \\ \end{array} \begin{array}{c} \mbox{tba} \\ \mbox{tba} \\ \mbox{tba} \\ \end{array} $			dB	
T _{WU}	Wake-Up Time (Cb = 1µF)		90 130 ms		ms
T _{STDB}	Standby Time (Cb = 1µF)		10		μs
V _{STDBH}	Standby Voltage Level High			1.3	V
V _{STDBL}	L Standby Voltage Level Low 0.4		V		
Φ_{M}	Phase Margin at Unity Gain $R_L = 8\Omega$, $C_L = 500pF$	65 Degrees		Degrees	
GM	$ \begin{array}{ c c c } \mbox{Gain Margin} & & & & \\ \mbox{R}_L = 8\Omega, C_L = 500 \mbox{pF} & & & \\ \end{tabular} $		dB		
GBP	Gain Bandwidth Product $R_L = 8\Omega$		1.5		MHz

1) Standby mode is activated when Vstdby is tied to Gnd.

All PSRR data limits are guaranteed by production sampling tests Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the sinusoidal signal superimposed upon Vcc.

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Table 5: V_{cc} = +3.3V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)	
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Symbol	Parameter		Тур.	Max.	Unit
I _{CC}	Supply Current 6.6 No input signal, no load 6.6		12	mA	
I _{STANDBY}	Standby Current ¹ No input signal, Vstdby = G_{ND} , RL = 8 Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, $RL = 8\Omega$ 110		10	mV	
Po	Output Power THD = 1% Max, F = 1kHz, RL = 8Ω	375	500	0 mW	
THD + N	Total Harmonic Distortion + Noise Po = 400mWrms, Av = 2, 20Hz \leq F \leq 20kHz, RL = 8 Ω		0.1	%	
PSRR	Power Supply Rejection Ratio ² RL = 8Ω , Av = 2, Vripple = 200mVpp, Input Grounded F = 217Hz F = 1kHz	55 55	61 63	dB	
Crosstalk	Channel Separation, $R_L = 8\Omega$ F = 1kHz F = 20Hz to 20kHz		tba tba	tba dB tba	
Τ _{WU}	Wake-Up Time (Cb = 1µF)		110	140 ms	
T _{STDB}	Standby Time (Cb = 1μ F)		10	μs	
V _{STDBH}	Standby Voltage Level High			1.2	V
V _{STDBL}	Standby Voltage Level Low			0.4	V
Φ_{M}	Phase Margin at Unity Gain $R_L = 8\Omega, C_L = 500pF$		65 Degrees		Degrees
GM	Gain Margin $R_L = 8\Omega$, $C_L = 500 pF$	15 dB			
GBP	Gain Bandwidth Product $R_L = 8\Omega$ 1.5		MHz		
GBP	Gain Bandwidth Product $R_L = 8\Omega$		1.5		MHz

1) Standby mode is activated when Vstdby is tied to Gnd.

All PSRR data limits are guaranteed by production sampling tests Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the sinusoidal signal superimposed upon Vcc.

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Symbol	Parameter		Тур.	Max.	Unit
I _{cc}	Supply Current 6.2 12		12	mA	
I _{STANDBY}	YStandby Current 1 No input signal, Vstdby = G _{ND} , RL = 8Ω101000		nA		
Voo	Output Offset Voltage No input signal, $RL = 8\Omega$		1	10	mV
Po	Output Power THD = 1% Max, F = 1kHz, RL = 8Ω	220	300	mW	
THD + N	Total Harmonic Distortion + Noise Po = 200mWrms, Av = 2, 20Hz \leq F \leq 20kHz, RL = 8 Ω		0.1).1 %	
PSRR	Power Supply Rejection Ratio ² RL = 8Ω , Av = 2, Vripple = 200mVpp, Input Grounded F = 217Hz F = 1kHz	55 55	60 62	dB	
Crosstalk	$ \begin{array}{ c c c c } \hline Channel Separation, R_L = 8\Omega \\ \hline F = 1 kHz \\ F = 20 Hz to 20 kHz \\ \hline tt \\ tt \\ \hline tt \\ tt \\ \hline tt \\ tt \\ $		tba tba		dB
T _{WU}	Wake-Up Time (Cb = 1μ F)		125	150	ms
T _{STDB}	Standby Time (Cb = 1µF)		10		μs
V _{STDBH}	Standby Voltage Level High			1.2	V
V _{STDBL}	L Standby Voltage Level Low 0.4		V		
Φ_{M}	Phase Margin at Unity Gain $R_L = 8\Omega, C_L = 500 pF$ 65		Degrees		
GM	Gain Margin $R_L = 8\Omega, C_L = 500 pF$ 15		dB		
GBP	Gain Bandwidth Product $R_L = 8\Omega$		1.5 MHz		MHz

Table 6: V_{CC} = +2.6V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

1) Standby mode is activated when Vstdby is tied to Gnd.

All PSRR data limits are guaranteed by production sampling tests Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the sinusoidal signal superimposed upon Vcc.

4.1 TS4985EIJT Pinout and Package Mechanical Data



4.1.1 Pinout (top view)

4.1.2 Marking (top view)



4.1.3 Package mechanical data for 15-bump flip-chip







4.1.4 Tape & reel specification (top view)

5 Revision History

Date	Revision	Description of Changes
01 Nov 2004	1	First Release

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