

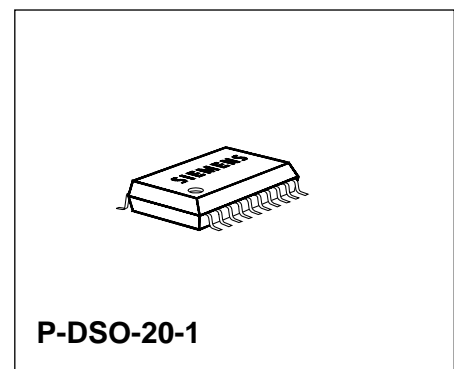
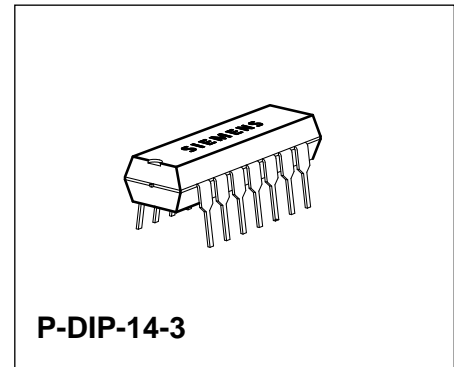
Decoder for Program Delivery Control and Video Program System PDC / VPS Decoder

**SDA 5648
SDA 5648X**

CMOS IC

Features

- Single-chip receiver for PDC data, broadcast either
 - in Broadcast Data Service Packet (BDSP) 8/30/2 according to CCIR teletext system B, or
 - in dedicated line no. 16 of the vertical blanking interval (VPS)
- Reception of Unified Date and Time (UDT) broadcast in BDSP 8/30/1
- Low external components count
- On-chip data and sync slicer
- I²C-Bus interface for communication with external microcontroller
- Selection of PDC/VPS operating mode software controlled by I²C-Bus register
- Pin and software compatible to VPS Decoder SDA 5642
- Supply voltage: 5 V ± 10 %
- Video input signal level: 0.7 V_{pp} to 1.4 V_{pp}
- Technology: CMOS
- Package: P-DIP-14-3 and P-DSO-20-1
- Operating temperature range: 0 to 70 °C



| Type | Ordering Code | Package |
|-----------|---------------|------------------------|
| SDA 5648 | Q67000-A5186 | P-DIP-14-3 |
| SDA 5648X | Q67006-A5198 | P-DSO-20-1 Tape & Reel |

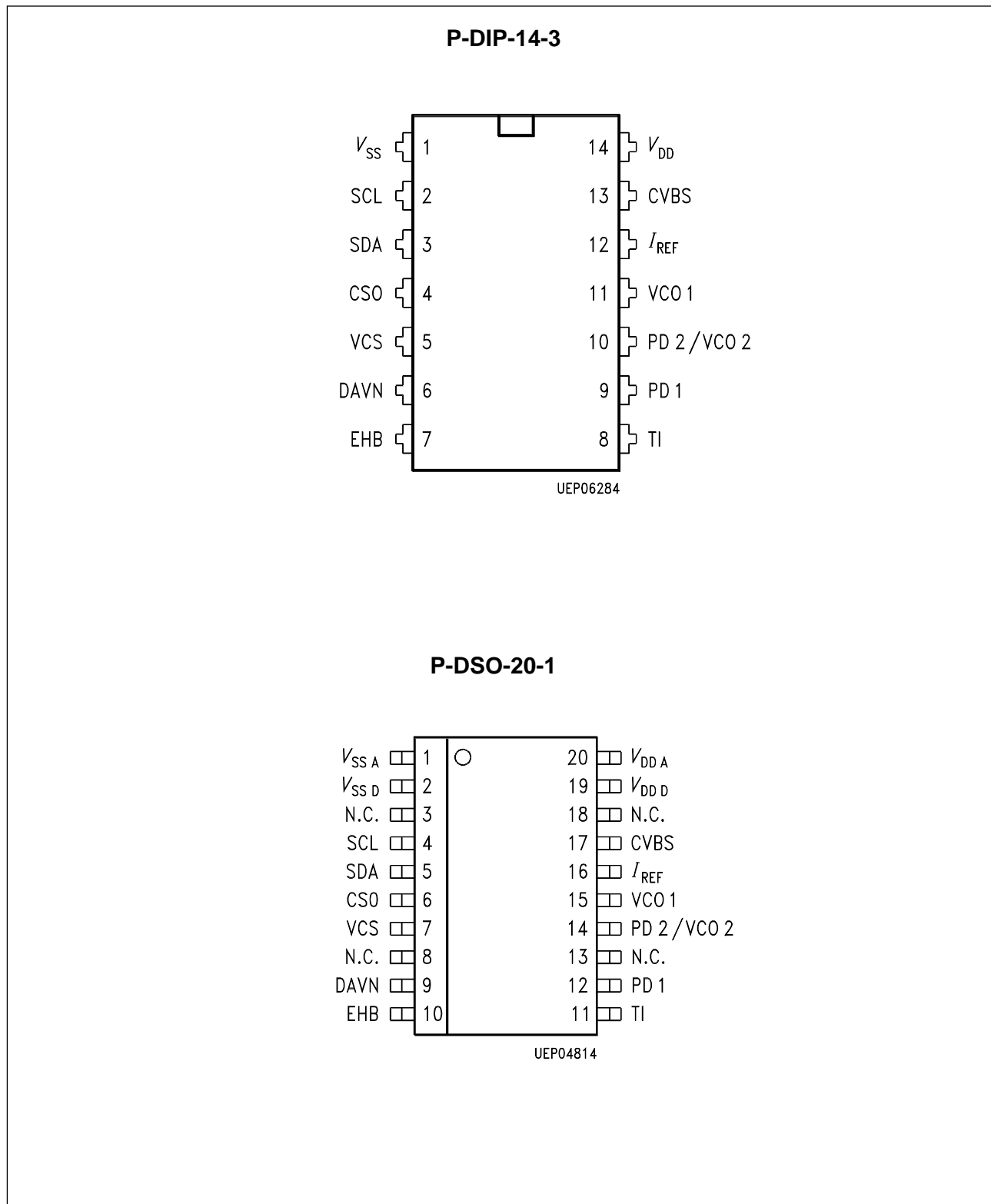
Functional Description

The CMOS circuit SDA 5648 is intended for use in video cassette recorders to retrieve control data of the PDC system from the data lines broadcast during the vertical blanking interval of a standard video signal.

The SDA 5648 is devised to handle PDC data transported either in Broadcast Data Service Packet (BDSP) 8/30 format 2 (bytes no. 13 through 25) of CCIR teletext system B or in the dedicated data line no. 16 in the case of VPS.

Furthermore it is able to receive the Unified Date and Time (UDT) information transmitted in bytes no. 15 through 21 of packet 8/30 format 1.

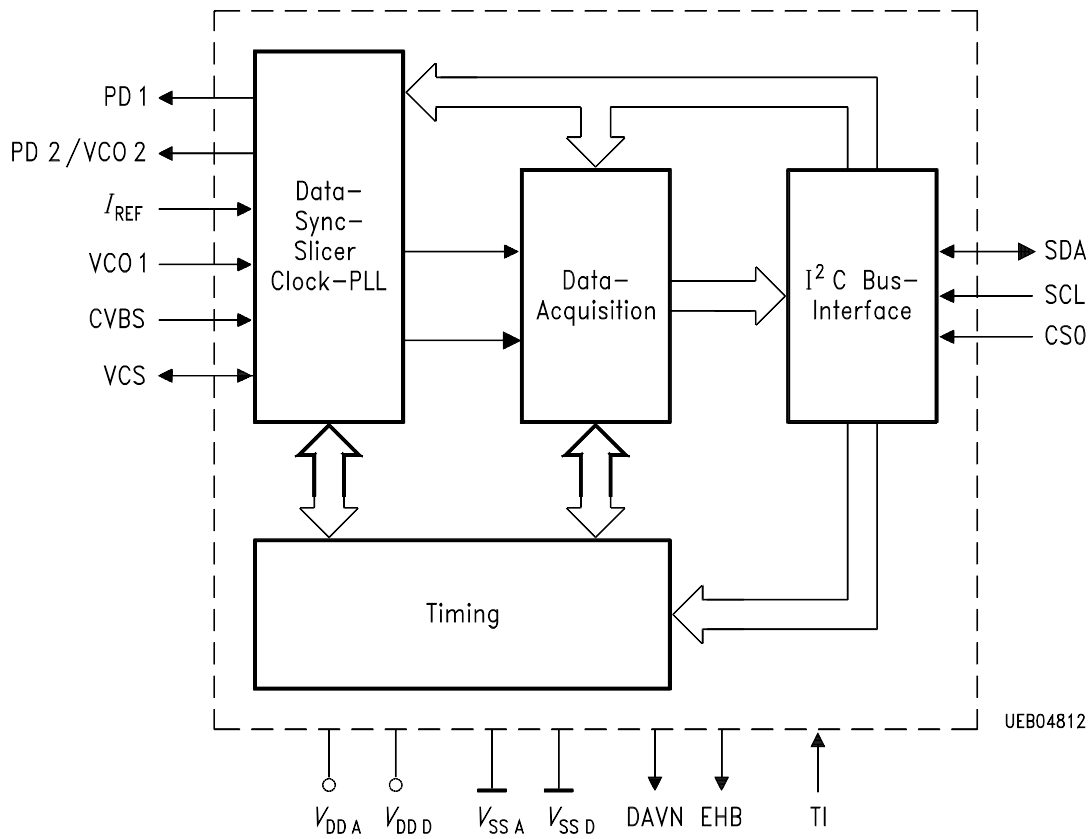
Pin Configuration (top view)



Operating mode (PDC/VPS) is selected by a control register which can be written to via the I²C-Bus interface.

Pin Definitions and Functions

| Pin No. P-DIP-14-3 | Pin No. P-DSO-20-1 | Symbol | Function |
|-----------------------|-----------------------|-----------|---|
| 1 | | V_{SS} | Ground (0 V) |
| | 1 | V_{SSA} | Analog ground (0 V) |
| | 2 | V_{SSD} | Digital ground (0 V) |
| | 3 | N.C. | Not connected |
| 2 | 4 | SCL | Serial clock input of I ² C-Bus. |
| 3 | 5 | SDA | Serial data input of I ² C-Bus. |
| 4 | 6 | CS0 | Chip select input determining the I ² C-Bus addresses: 20 _H / 21 _H , when pulled low 22 _H / 23 _H , when pulled high. |
| 5 | 7 | VCS | Video Composite Sync output from sync slicer used for PLL based clock generation. |
| | 8 | N.C. | Not connected |
| 6 | 9 | DAVN | Data available output active low, when PDC/VPS data is received. |
| 7 | 10 | EHB | Output signaling the presence of the first field active high. |
| 8 | 11 | TI | Test input; activates test mode when pulled high. |
| 9 | 12 | PD1 | Phase detector/charge pump output of data PLL (DAPLL). |
| | 13 | N.C. | Not connected |
| 10 | 14 | PD2/VCO2 | Connector of the loop filter for the SYSPLL. |
| 11 | 15 | VCO1 | Input to the voltage controlled oscillator #1 of the DAPLL. |
| 12 | 16 | I_{REF} | Reference current input for the on-chip analog circuit. |
| 13 | 17 | CVBS | Composite video signal input. |
| | 18 | N.C. | Not connected |
| 14 | | V_{DD} | Positive supply voltage (+ 5 V nom.). |
| | 19 | V_{DDD} | Positive supply voltage for the digital circuits (+ 5 V nom.). |
| | 20 | V_{DDA} | Positive supply voltage for the analog circuits (+ 5 V nom.). |



Block Diagram

Circuit Description

Referring to the functional block diagram of the PDC / VPS decoder, the composite video signal with negative going sync pulses is coupled to the pin CVBS through a capacitor which is used for clamping the bottom of the sync pulses to an internally fixed level. The signal is passed on to the slicer, an analog circuitry separating the sync and the data parts of the CVBS signal, thus yielding the digital composite sync signal VCS and a digital data signal for further processing by comparing those signals to internally generated slicing levels.

The output of the sync separator is forwarded, on one hand, to the output pin VCS, and on the other hand, to the clock generator and the Timing block. The VCS signal represents a key signal that is used for deriving a system clock signal by means of a PLL.

The data slicer separates the data signal from the CVBS signal by comparing the video voltage to an internally generated slicing level which is found by averaging the data signal during TV line no. 16 in the VPS mode or by averaging the data signal during the clock run-in period of the teletext lines during the data entry window (DEW) in PDC mode.

The clock generator delivers the system clock needed for the basic timing as well as for the regeneration of the data clock. It is based on two phase locked loops (PLL's) all parts of which are integrated on chip with the exception of the loop filter components. Each of the PLL's is composed of a voltage controlled oscillator (VCO), a phase/frequency detector (PFD), and a charge pump which converts the digital output signals of the PFD to an analog current. That current is transformed to a control voltage for the VCO by the off-chip loop filter. The generated VCO frequencies are 10 MHz and 13.875 MHz for VPS mode and PDC mode, respectively.

All signals necessary for the control of sync and data slicing as well as for the data acquisition are generated by the Timing block.

In PDC mode, only teletext rows 8/30 containing Broadcast Data Service Package (BDSP) information are acquired. The relevant bytes of 8/30 format 1 (8/30/1) and 8/30 format 2 (8/30/2) are extracted. The 8/30/1-bytes are stored in the acquisition register in a transparent way without any bit manipulation, whereas the Hamming coded bytes of packet 8/30/2 are Hamming-checked and bytes with one bit error are corrected. The storage of error free or corrected 8/30/2-data bytes in the transfer register to the I²C-Bus is signalled by the DAVN output going low. The reception and storage of 8/30/1- data, however, is not indicated by the DAVN output. The presence of 8/30/1 data can only be checked by polling the data register via the I²C-Bus.

In VPS mode, the extracted data bits of TV line no. 16 are checked for biphasic errors. With no biphasic errors encountered, the acquired bytes are stored in the transfer register to the I²C-Bus. That transfer is signalled by a H/L transition of the DAVN output, as well.

In both operating modes data are updated when a new data line has been received, provided that the chip is not accessed via the I²C-Bus at the same time.

A micro controller can read the stored bytes via the I²C-Bus interface at any time. However, one must be aware that the storage of new data from the acquisition interface is inhibited as long as the PDC decoder is being accessed via the I²C-Bus. At the end of an I²C-Bus reading the transfer registers are set to FF (hex) until they are updated by the reception of new data packet contained in the CVBS signal.

I²C-Bus

General Information

The I²C-Bus interface implemented on the PDC decoder is a slave transmitter/receiver, i.e., both reading from and writing to the PDC / VPS decoder is possible. The clock line SCL is controlled only by the bus master usually being a micro controller, whereas the SDA line is controlled either by the master or by the slave. A data transfer can only be initiated by the bus master when the bus is free, i.e., both SDA and SCL lines are in a high state. As a general rule for the I²C-Bus, the SDA line changes state only when the SCL line is low. The only exception to that rule are the Start Condition and the Stop Condition. Further details are given below. The following abbreviations are used:

START : Start Condition generated by master
AS : Acknowledge by slave
AM : Acknowledge by master
NAM : No Acknowledge by master
STOP : Stop Condition generated by master

Chip Address

There are two pairs of chip addresses, which are selected by the CS0-input pin according to the following table

| CS0 Input | Write Mode | Read Mode |
|-----------|------------|-----------|
| Low | 20 (hex) | 21 (hex) |
| High | 22 (hex) | 23 (hex) |

Write Mode

For writing to the PDC decoder, the following format has to be used:

| | | | | | |
|-------|-----------------------|----|---------------------------|----|------|
| START | Chipadress White Mode | AS | Byte Set Control Register | AS | STOP |
|-------|-----------------------|----|---------------------------|----|------|

Data Transfer (Write Mode)

- Step 1:* In order to start a data transfer the master generates a Start Condition on the bus by pulling the SDA line low while the SCL line is held high.
- Step 2:* The bus master puts the chip address on the SDA line during the next eight SCL pulses.
- Step 3:* The master releases the SDA line during the ninth clock pulse. Thus the slave can generate an acknowledge (AS) by pulling the SDA line to a low level.
- Step 4:* The controller transmits the data byte to set the Control register.
- Step 5:* The slave acknowledges the reception of the byte.
- Step 6:* The master concludes the data communication by generating a Stop Condition.

The write mode is used to set the I²C-Bus control register which determines the operating mode:

Control Register

| | | | | | | | | |
|------------|----|----|----|----|----|-----|-------------|---------------|
| Bit Number | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | T4 | T3 | T2 | T1 | T0 | DIS | PDC/ VPS | FOR1/ FOR2 |

Default: All bits are set to 0 on power-up.

Bit 0: Determines, which kind of data is accessed via the I²C-Bus when PDC mode is active.

| Value | |
|-------------------------------------|---|
| 0 | 1 |
| BDSP 8/ 30/ 2 data accessible | BDSP 8/ 30/ 1 or header row data accessible (refer to description of Bit 2) |

Bit 1: Determines the operating mode.

| Value | |
|-----------------|-----------------|
| 0 | 1 |
| VPS mode active | PDC mode active |

Bits 2 through 7 are used for test purposes.

DIS: Don't care.

Bits 3 through 7 must not be changed for normal operation by user software!

Read Mode

For reading from the PDC decoder, the following format has to be used.

| | | | | | | | | | |
|-------|-------------|-----------|----|----------|----|-----|--------------|-----|------|
| START | Chipaddress | Read Mode | AS | 1st Byte | AM | ... | Last Byte | NAM | STOP |
|-------|-------------|-----------|----|----------|----|-----|--------------|-----|------|

Data Transfer (Read Mode)

- Step 1:* To start a data transfer the master generates a Start Condition on the bus by pulling the SDA line low while the SCL line is held high. The byte address counter in the decoder is reset and points to the first byte to be output.
- Step 2:* The bus master puts the chip address on the SDA line during the next eight SCL pulses.
- Step 3:* The master releases the SDA line during the ninth clock pulse. Thus the slave can generate an acknowledge (AS) by pulling the SDA line to a low level. At this moment, the slave switches to transmitting mode.
- Step 4:* During the next eight clock pulses the slave puts the addressed data byte onto the SDA line.
- Step 5:* The reception of the byte is acknowledged by the master device which, in turn, pulls down the SDA line during the next SCL clock pulse. By acknowledging a byte, the master prompts the slave to increment its internal address counter and to provide the output of the next data byte.
- Step 6:* Steps no. 4 and no. 5 are repeated, until the desired amount of bytes have been read.
- Step 7:* The last byte is output by the slave since it will not be acknowledged by the master.
- Step 8:* To conclude the read operation, the master doesn't acknowledge the last byte to be received. A No Acknowledge by the master (NAM) causes the slave to switch from transmitting to receiving mode. Note that the master can prematurely cease any reading operation by not acknowledging a byte.
- Step 9:* The master gains control over the SDA line and concludes the data transfer by generating a Stop Condition on the bus, i. e., by producing a low/high transition on the SDA line while the SCL line is in a high state. With the SDA and the SCL lines being both in a high state, the I²C-Bus is free and ready for another data transfer to be started.

The contents of up to 7 registers (bytes) can be read starting with byte 1 bit 7 (refer to the following table).

Order of Data Output on the I²C-Bus and Bit Allocation of the 3 Different Operating Modes

| I ² C-Bus | | PDC Packet 8/30 | | | | VPS Mode | | |
|----------------------|--------|-----------------|---------|---------------------|---------|---------------------|---------|---------------------|
| | | Format 1 | | Format 2 | | | | |
| t ↓ | Byte 1 | bit 7 | byte 15 | bit 0 ²⁾ | byte 16 | bit 0 ¹⁾ | byte 11 | bit 0 ²⁾ |
| | | 6 | | 1 | | 1 | | 1 |
| | | 5 | | 2 | | 2 | | 2 |
| | | 4 | | 3 | | 3 | | 3 |
| | | 3 | | 4 | byte 17 | bit 0 | | 4 |
| | | 2 | | 5 | | 1 | | 5 |
| | | 1 | | 6 | | 2 | | 6 |
| | | 0 | | 7 | | 3 | | 7 |
| | Byte 2 | bit 7 | byte 16 | bit 0 | byte 18 | bit 0 | byte 12 | bit 0 |
| | | 6 | | 1 | | 1 | | 1 |
| | | 5 | | 2 | | 2 | | 2 |
| | | 4 | | 3 | | 3 | | 3 |
| | | 3 | | 4 | byte 19 | bit 0 | | 4 |
| | | 2 | | 5 | | 1 | | 5 |
| | | 1 | | 6 | | 2 | | 6 |
| | | 0 | | 7 | | 3 | | 7 |
| | Byte 3 | bit 7 | byte 17 | bit 0 | byte 20 | bit 0 | byte 13 | bit 0 |
| | | 6 | | 1 | | 1 | | 1 |
| | | 5 | | 2 | | 2 | | 2 |
| | | 4 | | 3 | | 3 | | 3 |
| | | 3 | | 4 | byte 21 | bit 0 | | 4 |
| | | 2 | | 5 | | 1 | | 5 |
| | | 1 | | 6 | | 2 | | 6 |
| | | 0 | | 7 | | 3 | | 7 |
| | Byte 4 | bit 7 | byte 18 | bit 0 | byte 22 | bit 0 | byte 14 | bit 0 |
| | | 6 | | 1 | | 1 | | 1 |
| | | 5 | | 2 | | 2 | | 2 |
| | | 4 | | 3 | | 3 | | 3 |
| | | 3 | | 4 | byte 23 | bit 0 | | 4 |
| | | 2 | | 5 | | 1 | | 5 |
| | | 1 | | 6 | | 2 | | 6 |
| | | 0 | | 7 | | 3 | | 7 |

1) Message bit numbers according to EBU specification of PDC system.
2) Transmission bit number

Order of Data Output on the I²C-Bus and Bit Allocation of the 3 Different Operating Modes
(cont'd)

| I ² C-Bus | | PDC Packet 8/30 | | | | VPS Mode | | |
|----------------------|-------|-----------------|-------|----------|--------------|--------------|--------------|---|
| | | Format 1 | | Format 2 | | | | |
| Byte 5 | bit 7 | byte 19 | bit 0 | byte 14 | bit 0 | byte 5 | bit 0 | |
| | 6 | | 1 | | 1 | | 1 | |
| | 5 | | 2 | | 2 | | 2 | |
| | 4 | | 3 | | 3 | | 3 | |
| | 3 | | 4 | | byte 15 | | bit 0 | 4 |
| | 2 | | 5 | | | | 1 | 5 |
| | 1 | | 6 | | | | 2 | 6 |
| | 0 | | 7 | | | | 3 | 7 |
| Byte 6 | bit 7 | byte 20 | bit 0 | byte 24 | bit 0 | byte 15 | bit 0 | |
| | 6 | | 1 | | 1 | | 1 | |
| | 5 | | 2 | | 2 | | 2 | |
| | 4 | | 3 | | 3 | | 3 | |
| | 3 | | 4 | | byte 25 | | bit 0 | 4 |
| | 2 | | 5 | | | | 1 | 5 |
| | 1 | | 6 | | | | 2 | 6 |
| | 0 | | 7 | | | | 3 | 7 |
| Byte 7 | bit 7 | byte 21 | bit 0 | byte 13 | bit 0 | – set to “1” | | |
| | 6 | | 1 | | 1 | – set to “1” | | |
| | 5 | | 2 | | 2 | – set to “1” | | |
| | 4 | | 3 | | 3 | – set to “1” | | |
| | 3 | | 4 | | – set to “1” | | – set to “1” | |
| | 2 | | 5 | | – set to “1” | | – set to “1” | |
| | 1 | | 6 | | – set to “1” | | – set to “1” | |
| | 0 | | 7 | | – set to “1” | | – set to “1” | |

Description of DAVN and EHB Outputs

DAVN (Data Valid active low)

EHB (First Field active high)

| Signal Output | VPS Mode | PDC Mode | |
|------------------------------|---|---|--|
| | | 8/30/2 | 8/30/1 |
| DAVN | | | |
| H/L-transition (set low) | in line 16 when valid VPS data is received | in the line carrying valid 8/30/2 data | in the line carrying valid 8/30/1 data |
| L/H-transition (set high) | at the start of line 16 | at the beginning of the next field i.e., at the start of the next data entry window | |
| always set high | on power-up or during I ² C-Bus accesses when the bus master doesn't acknowledge in order to generate the stop condition | | |
| EHB | | | |
| L/H-transition | at the beginning of the first field | | |
| H/L-transition | at the beginning of the second field | | |

In test mode (i.e. TI = high), both DAVN and EHB are controlled by the CS0 pin and reproduce the state of the CS0 input.

Electrical Characteristics

Absolute Maximum Ratings

$T_A = 25\text{ °C}$

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|------------------------------|--------------|--------------|------|------|------|----------------|
| | | min. | typ. | max. | | |
| Ambient temperature | T_A | 0 | | 70 | °C | in operation |
| Storage temperature | T_{stg} | - 40 | | 125 | °C | by storage |
| Total power dissipation | P_{tot} | | | 300 | mW | |
| Power dissipation per output | P_{DQ} | | | 10 | mW | |
| Input voltage | V_{IM} | - 0.3 | | 6 | V | |
| Supply voltage | V_{DD} | - 0.3 | | 6 | V | |
| Thermal resistance | $R_{th\ SU}$ | | | 80 | K/W | |

Operating Range

| | | | | | | |
|---------------------------|----------|-----|---|-----|----|--|
| Supply voltage | V_{DD} | 4.5 | 5 | 5.5 | V | |
| Supply current | I_{DD} | | 5 | 15 | mA | |
| Ambient temperature range | T_A | 0 | | 70 | °C | |

Characteristics

$T_A = 25\text{ °C}$

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|-----------|--------|--------------|------|------|------|----------------|
| | | min. | typ. | max. | | |

Input Signals SDA, SCL, CS0

| | | | | | | |
|-------------------|----------|---------------------|--|---------------------|----|--|
| H-input voltage | V_{IH} | $0.7 \times V_{DD}$ | | V_{DD} | V | |
| L-input voltage | V_{IL} | 0 | | $0.3 \times V_{DD}$ | V | |
| Input capacitance | C_I | | | 10 | pF | |
| Input current | I_{IM} | | | 10 | μA | |

Input Signal TI

| | | | | | | |
|-------------------|----------|---------------------|--|---------------------|----|--|
| H-input voltage | V_{IH} | $0.9 \times V_{DD}$ | | V_{DD} | V | |
| L-input voltage | V_{IL} | 0 | | $0.1 \times V_{DD}$ | V | |
| Input capacitance | C_I | | | 10 | pF | |
| Input current | I_{IM} | | | 10 | μA | |

Characteristics (cont'd)

$T_A = 25\text{ °C}$

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|-----------|--------|--------------|------|------|------|----------------|
| | | min. | typ. | max. | | |

Input Signals CVBS

(pos. Video, neg. Sync)

| | | | | | | |
|--|------------|-------------------------------|-------|-------|---------------|----------------------|
| Video input signal level | V_{CVBS} | 0.7 | 1.0 | 2.0 | V | |
| Synchron signal amplitude | V_{SYNC} | 0.15 | 0.3 | 1.0 | V | |
| Data amplitude | V_{DAT} | 0.25 $1.5 \times V_{SYNC}$ | 0.5 | 1.0 | V | VPS mode PDC mode |
| Coupling capacitor | C_C | | 33 | | nF | |
| H-input current | I_{IH} | | | 10 | μA | $V_I = 5\text{ V}$ |
| L-input current | I_{IL} | - 1000 | - 400 | - 100 | μA | $V_I = 0\text{ V}$ |
| Source impedance | R_S | | | 250 | Ω | |
| Leakage resistance at coupling capacitor | R_C | 0.91 | 1 | 1.2 | M Ω | |

Output Signals DAVN, EHB, VCS

| | | | | | | |
|------------------|----------|----------------|--|-----|---|----------------------------|
| H-output voltage | V_{QH} | $V_{DD} - 0.5$ | | | V | $I_Q = - 100\ \mu\text{A}$ |
| L-output voltage | V_{QL} | | | 0.4 | V | $I_Q = 1.6\ \text{mA}$ |

Output Signals SDA (Open-Drain-Stage)

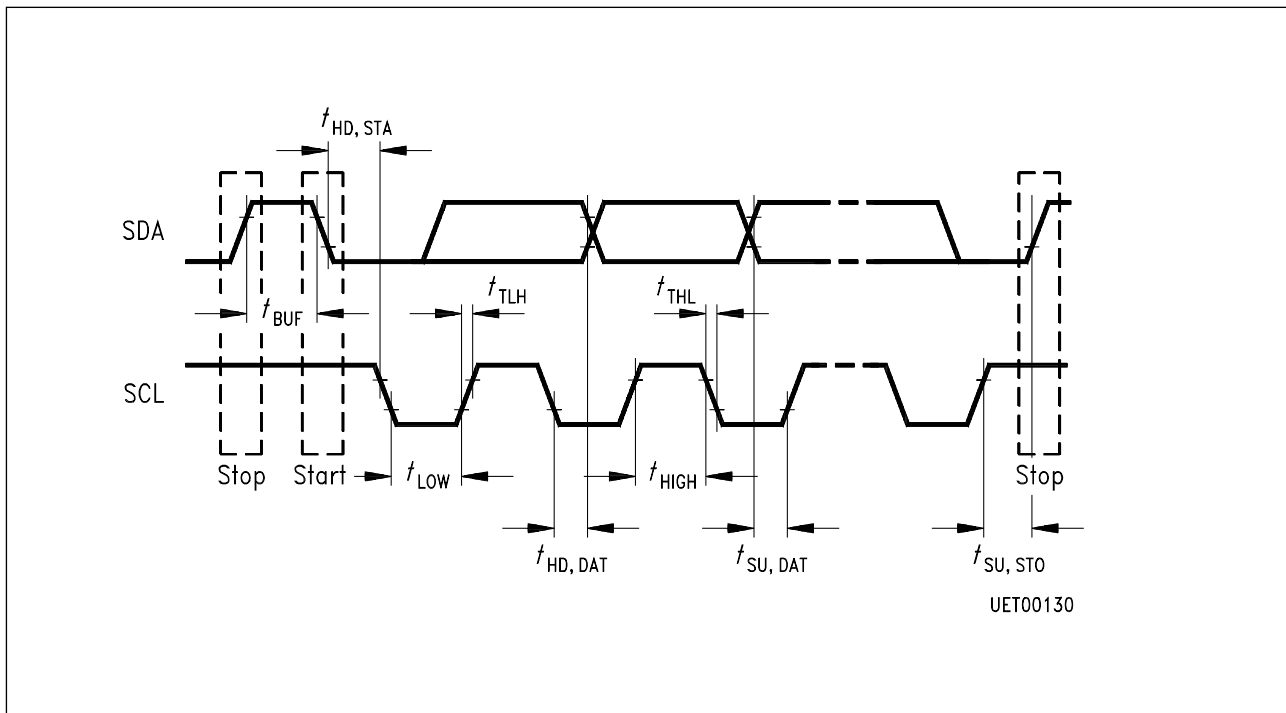
| | | | | | | |
|----------------------------|----------|--|--|-----|---|------------------------|
| L-output voltage | V_{QL} | | | 0.4 | V | $I_Q = 3.0\ \text{mA}$ |
| Permissible output voltage | | | | 5.5 | V | |

PLL-Loop Filter Components (see application circuit)

| | | | | | | |
|------------------------|-------|--|------|--|------------|--|
| Resistance at PD2/VCO2 | R_1 | | 6.8 | | k Ω | |
| Resistance at VCO1 | R_2 | | 1200 | | k Ω | |
| Attenuation resistance | R_3 | | 6.8 | | k Ω | |
| Resistance at PD2/VCO2 | R_5 | | 1200 | | k Ω | |
| Integration capacitor | C_1 | | 2.2 | | nF | |
| Integration capacitor | C_3 | | 33 | | nF | |

VCO – Frequency Range Adjustment

| | | | | | | |
|--|-------|--|-----|--|------------|--|
| Resistance at IREF (for bias current adjustment) | R_4 | | 100 | | k Ω | |
|--|-------|--|-----|--|------------|--|

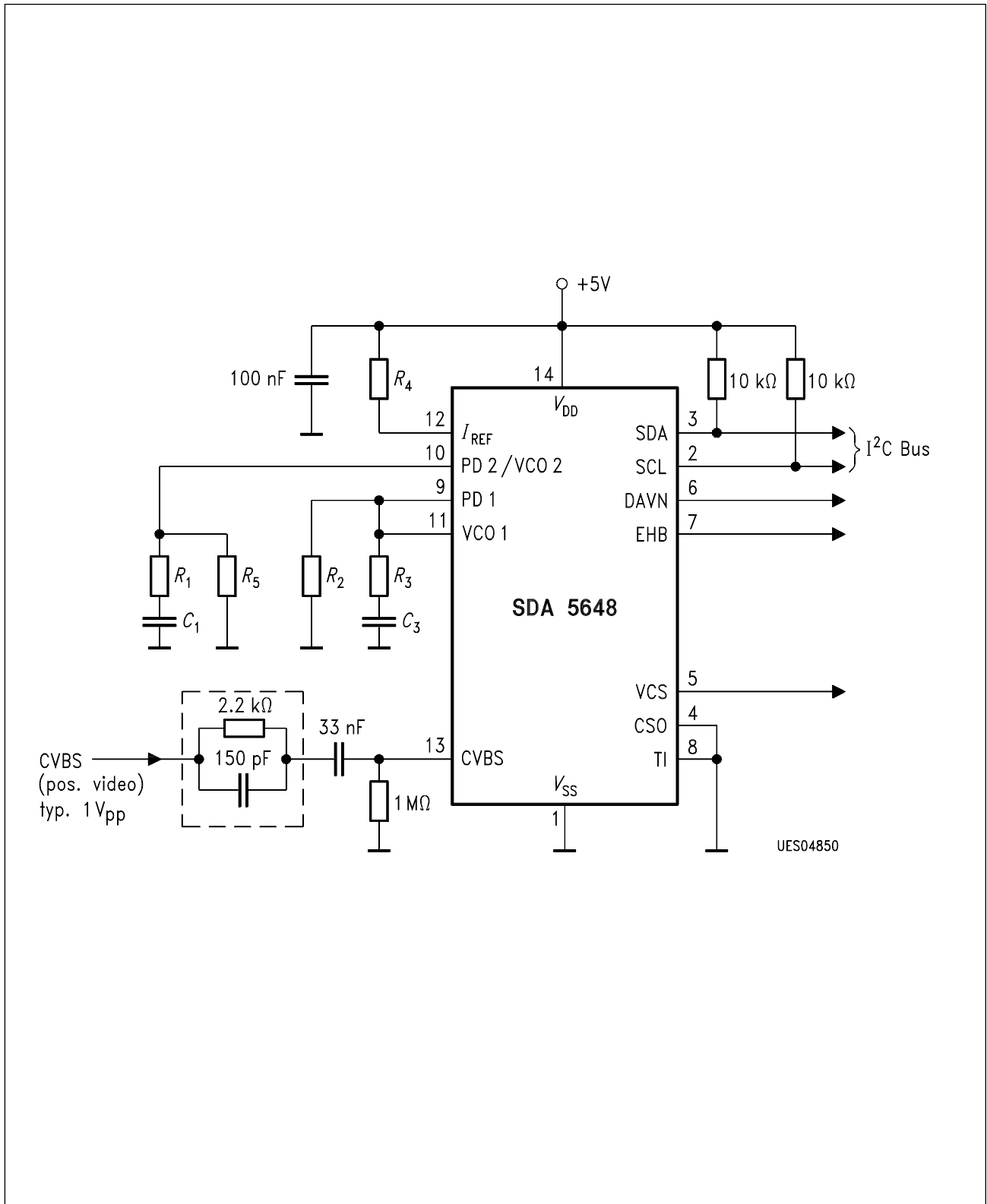


I²C-Bus Timing

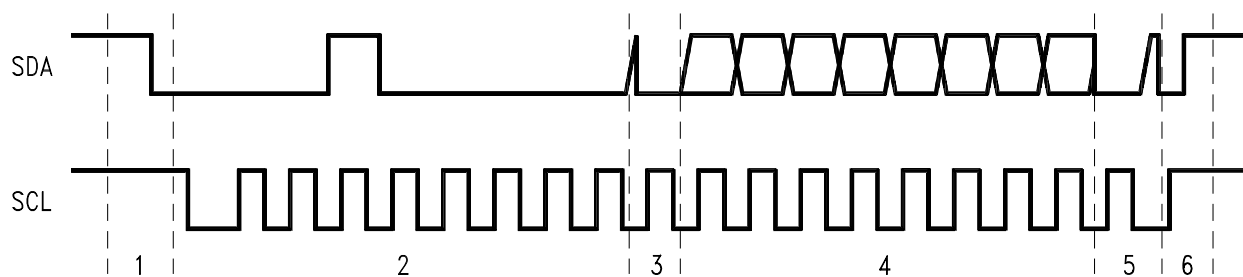
| Parameter | Symbol | Limit Values | | Unit |
|--|---------------|--------------|------|---------|
| | | min. | max. | |
| Clock frequency | f_{SCL} | 0 | 100 | kHz |
| Inactive time prior to new transmission start-up | t_{BUF} | 4.7 | | μ s |
| Hold time during start condition | $t_{HD, STA}$ | 4.0 | | μ s |
| Low-period of clock | t_{LOW} | 4.7 | | μ s |
| High-period of clock | t_{HIGH} | 4.0 | | μ s |
| Set-up time for data | $t_{SU, DAT}$ | 250 | | ns |
| Rise time for SDA and SCL signal | t_{TLH} | | 1 | μ s |
| Fall time for SDA and SCL signal | t_{THL} | | 300 | ns |
| Set-up time for SCL clock during stop condition | $t_{SU, STO}$ | 4.7 | | μ s |

All values referred to V_{IH} and V_{IL} levels.

PDC/VPS-Receiver



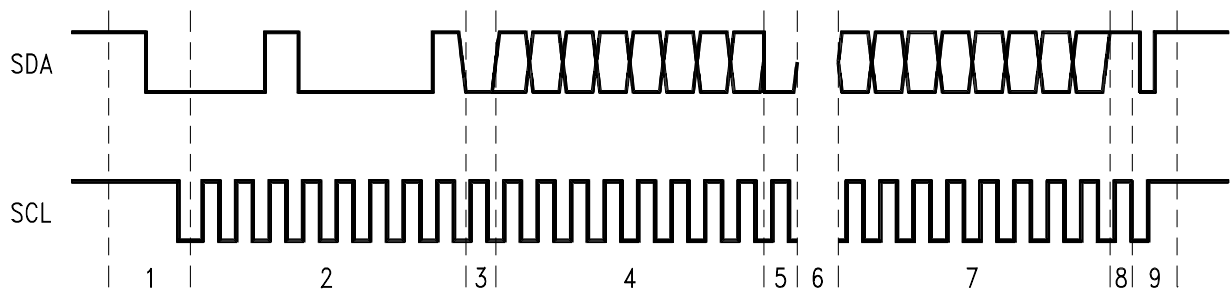
Application Circuit



- 1 Start Condition
- 2 Chip Address Write Mode
- 3 Acknowledge by Slave
- 4 Data byte for Control Register
- 5 Acknowledge by Slave
- 6 Stop Condition

UET06178

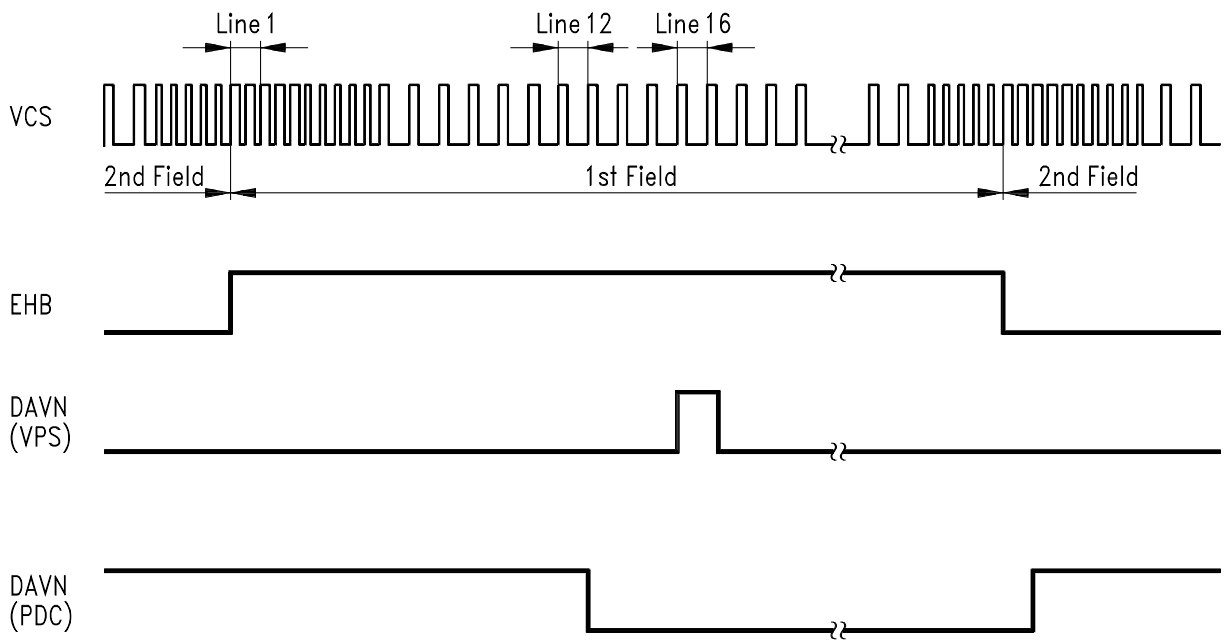
I²C-Bus Signals During Write Operations



- 1 Start Condition
- 2 Chip Address
- 3 Acknowledge by Slave
- 4 Output of 1st Data byte from Slave to Master
- 5 Acknowledge by Master
- 6 Output of further bytes
- 7 Output of last byte
- 8 No Acknowledge by Master
- 9 Stop Condition

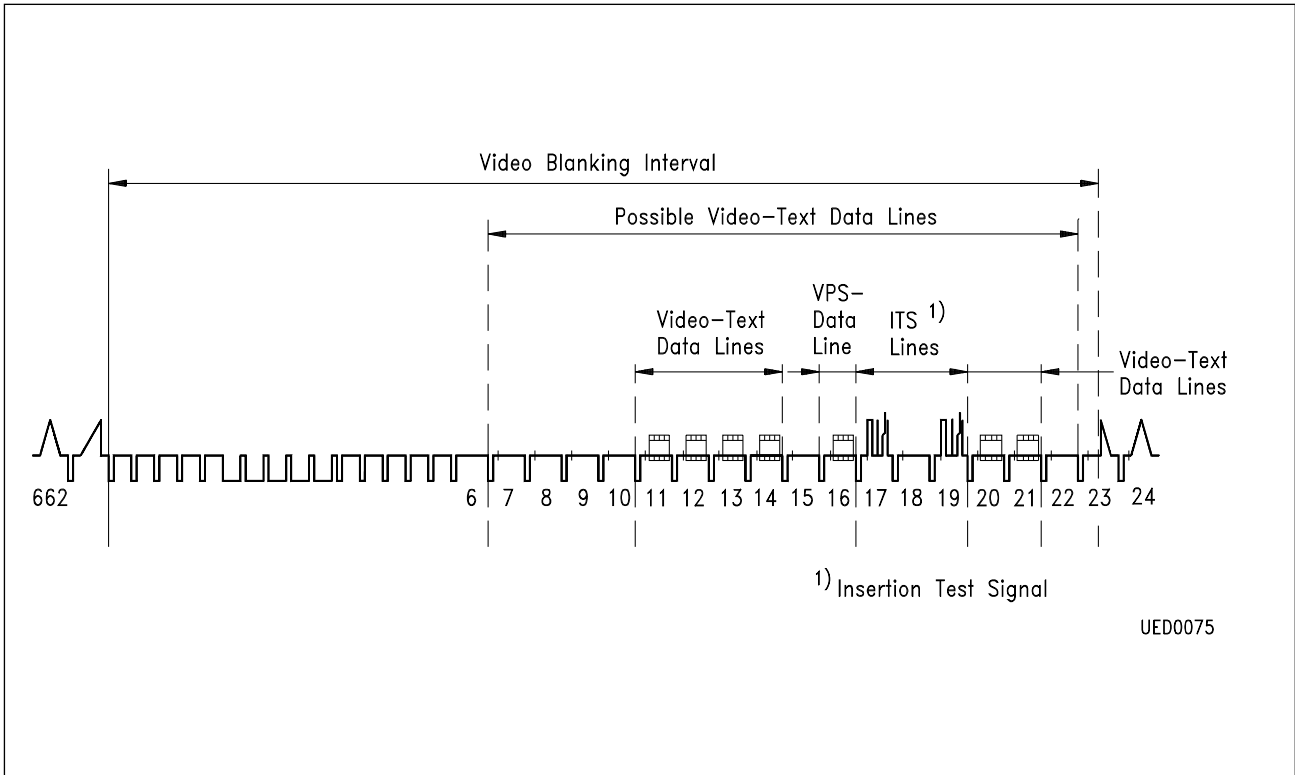
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I²C-Bus Signals During Read Operations

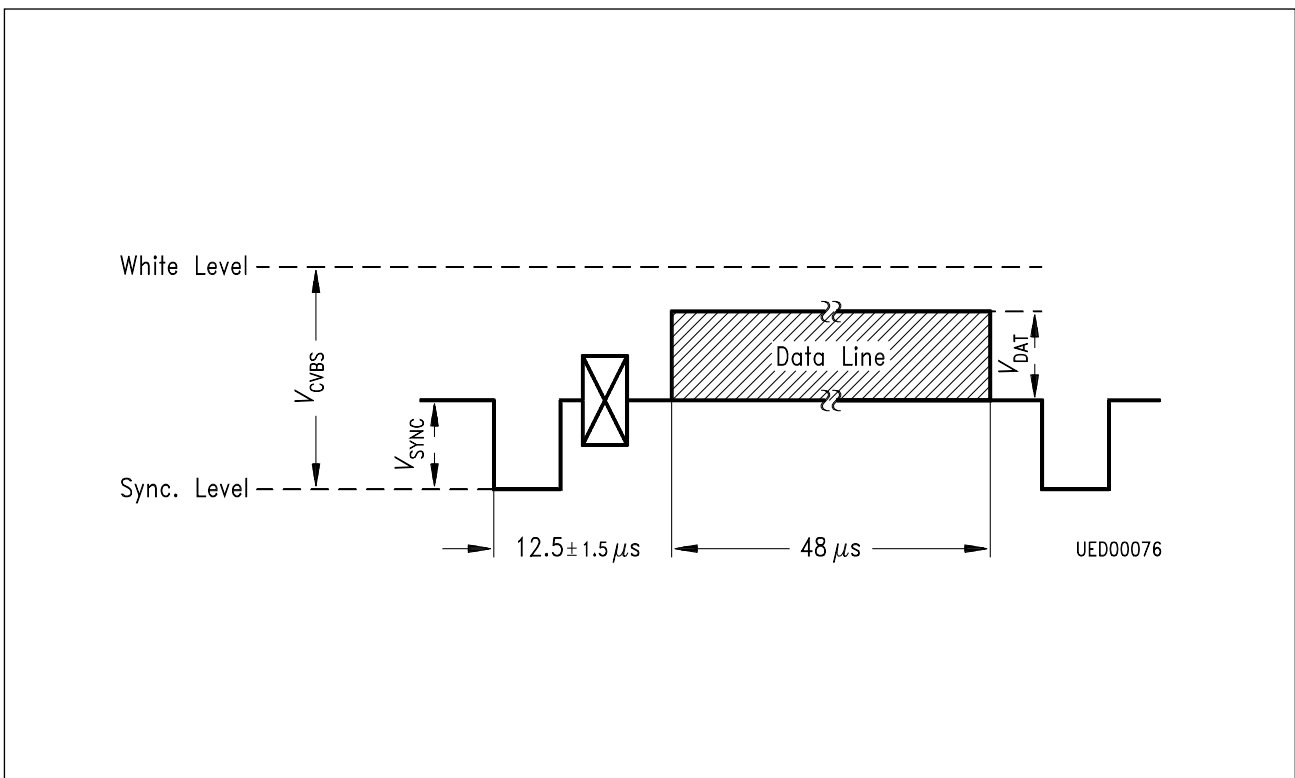


In this example: 8/30/2 packet is received in line 12

UET06180



Position of Teletext and VPS Data Lines within the Vertical Blanking Interval
(shown for first field)



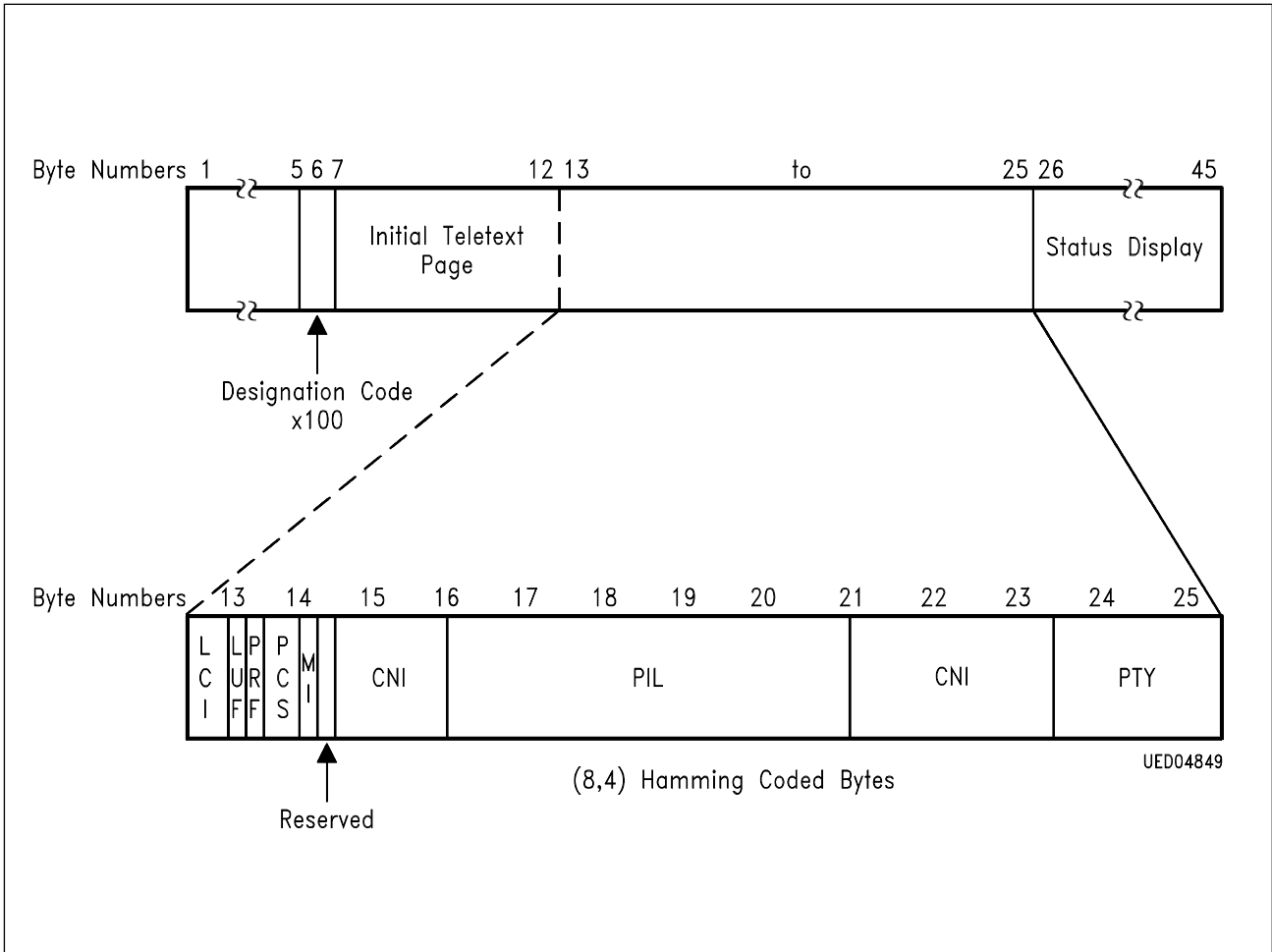
Definition of Voltage Levels for VPS Data Line

BDSP 8/30 Format 1 Bit Allocation

| Byte No. | Bit No. | | | | | | | | Contents | |
|----------|----------------------------|---|----------|-------|----------------------------|---|-------|-------|----------------|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | |
| 15 | Weight 2^{-2} | | 2^{-1} | 2^0 | Weight 2^1 | | 2^2 | 2^3 | Sign 0 1 | Time Offset Code |
| 16 | MJD Digit Weight 10^4 | | | | 1 | 1 | 1 | 1 | | Modified Julian Date (MJD) 1. Byte |
| 17 | MJD Digit Weight 10^2 | | | | MJD Digit Weight 10^3 | | | | | Modified Julian Date 2. Byte |
| 18 | MJD Digit Weight 10^0 | | | | MJD Digit Weight 10^1 | | | | | Modified Julian Date (MJD) 3. Byte |
| 19 | UTC Hours Units | | | | UTC Hours Tens | | | | | Universal Time Coordinated (UTC) 1. Byte |
| 20 | UTC Minutes Units | | | | UTC Minutes Tens | | | | | Universal Time Coordinated 2. Byte |
| 21 | UTC Seconds Units | | | | UTC Seconds Tens | | | | | Universal Time Coordinated 3. Byte |

This corresponds to the coding adopted in CCIR teletext system B BDSP 8/30 format 1.

NB: The received bytes are output on the I²C-bus in a transparent way, i.e., on a bit-first-in-first-out basis. No bit manipulation is performed on the chip in this operating mode. When evaluating the numbers, note that each 4-bit-digit has been incremented by one prior to transmission, and the least significant bits are transmitted first.



Structure of the Teletext Data Packet 8/30 Format 2

BDSP 8/30 Format 2 Bit Allocation

The four message bits of byte 13 are used as follows:

byte 13 bit 0 – LCI b_1) label channel identifier
 1 – LCI b_2)
 2 – LUF label update flag
 3 – reserved but as yet undefined

The message bits of bytes 14 – 25 are used in a way similar to the coding of the label in the dedicated television line as follows:

| | | |
|---------------------------------------|------------------------------|-------------|
| byte 14 bit 0 PCS b_1) status of | byte 20 bit 0 PIL b_{15}) | |
| 1 PCS b_2) analogue sound | 1 PIL b_{16}) | |
| | 2 PIL b_{17}) | minute |
| 2) reserved but yet | 3 PIL b_{18}) | |
| 3) undefined | byte 21 bit 0 PIL b_{19}) | |
| | 1 PIL b_{20}) | |
| byte 15 bit 0 CNI b_1) | | |
| 1 CNI b_2) country | 2 CNI b_5) | |
| 2 CNI b_3) | 3 CNI b_6) | country |
| 3 CNI b_4) | byte 22 bit 0 CNI b_7) | |
| | 1 CNI b_8) | |
| byte 16 bit 0 CNI b_9) network (or | | |
| 1 CNI b_{10}) program provider) | 2 CNI b_{11}) | |
| | 3 CNI b_{12}) | |
| 2 PIL b_1) | byte 23 bit 0 CNI b_{13}) | network (or |
| 3 PIL b_2) | 1 CNI b_{14}) | program |
| byte 17 bit 0 PIL b_3) day | 2 CNI b_{15}) | provider) |
| 1 PIL b_4) | 3 CNI b_{16}) | |
| 2 PIL b_5) | | |
| | byte 24 bit 0 PTY b_1) | |
| 3 PIL b_6) | 1 PTY b_2) | |
| byte 18 bit 0 PIL b_7) month | 2 PTY b_3) | |
| 1 PIL b_8) | 3 PTY b_4) | program |
| 2 PIL b_9) | byte 25 bit 0 PTY b_5) | type |
| | 1 PTY b_6) | |
| 3 PIL b_{10}) | 2 PTY b_7) | |
| byte 19 bit 0 PIL b_{11}) | 3 PTY b_8) | |
| 1 PIL b_{12}) hour | | |
| 2 PIL b_{13}) | | |
| 3 PIL b_{14}) | | |

Data Format of the Program Delivery Data in the Dedicated TV Line

| Parameter → | PCS | | | | CNI | | | | PIL | | | | CNI | | | | PTY | | | |
|---|----------------|----------------------|---------------------|--|---------------------|--------------------|-----------------|-----------------|-----------------|---------------|----------------|------------------------------------|---------------------|----|----|----|-----|----|----|----|
| | 1 | 2 | 3 & 4 | 5 | 6 to 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | |
| Byte No. → | | | | | | | | | | | | | | | | | | | | |
| Parameter bits b _i , I = → | | | | | | | | | | | | | | | | | | | | |
| Transmission bit No. → | | | | | | | | | | | | | | | | | | | | |
| Content → | Clock run-in | Start code | Not relevant to PDC | Reserved for enhancement of VPS M L | Not relevant to PDC | Net. or prov. bin. | Day binary | Month binary | Hour binary | Minute binary | Country binary | Network or program provider binary | Program type binary | | | | | | | |
| | | | | | | | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 |
| Reserved code values for receiver control (service codes) | | Timer control code | | N.....N | | N N 0 0 0 0 0 0 | 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 | N | N.....N | A | A | | | | | | | |
| | | Record inhibit/term. | | N.....N | | N N 0 0 0 0 0 0 | 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 | N | N.....N | A | A | | | | | | | |
| | | Interruption code | | N.....N | | N N 0 0 0 0 0 0 | 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 | N | N.....N | A | A | | | | | | | |
| | | Continuation code | | N.....N | | N N 0 0 0 0 0 0 | 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 | 1 1 1 1 1 1 1 1 | N | N.....N | A | A | | | | | | | |
| | | Unenhanced VPS | | 1 1 1 1 | | N N P | | | | | N | N.....P | A | A | | | | | | |
| | PTY not in use | | N.....N | | N N P | | | | | N | N.....P | A | 1 1 1 1 1 1 1 1 | | | | | | | |

Abbreviations: CNI = Country and Network Identification
 PCS = Program Control Status
 PIL = Program Identification Label
 PTY = Program Type

A = Bit value is that of the current PTY code
 N = Bit value is that of the current CNI code
 P = Bit value is that of the current PIL code

M = Most-significant bit
 L = Least-significant bit