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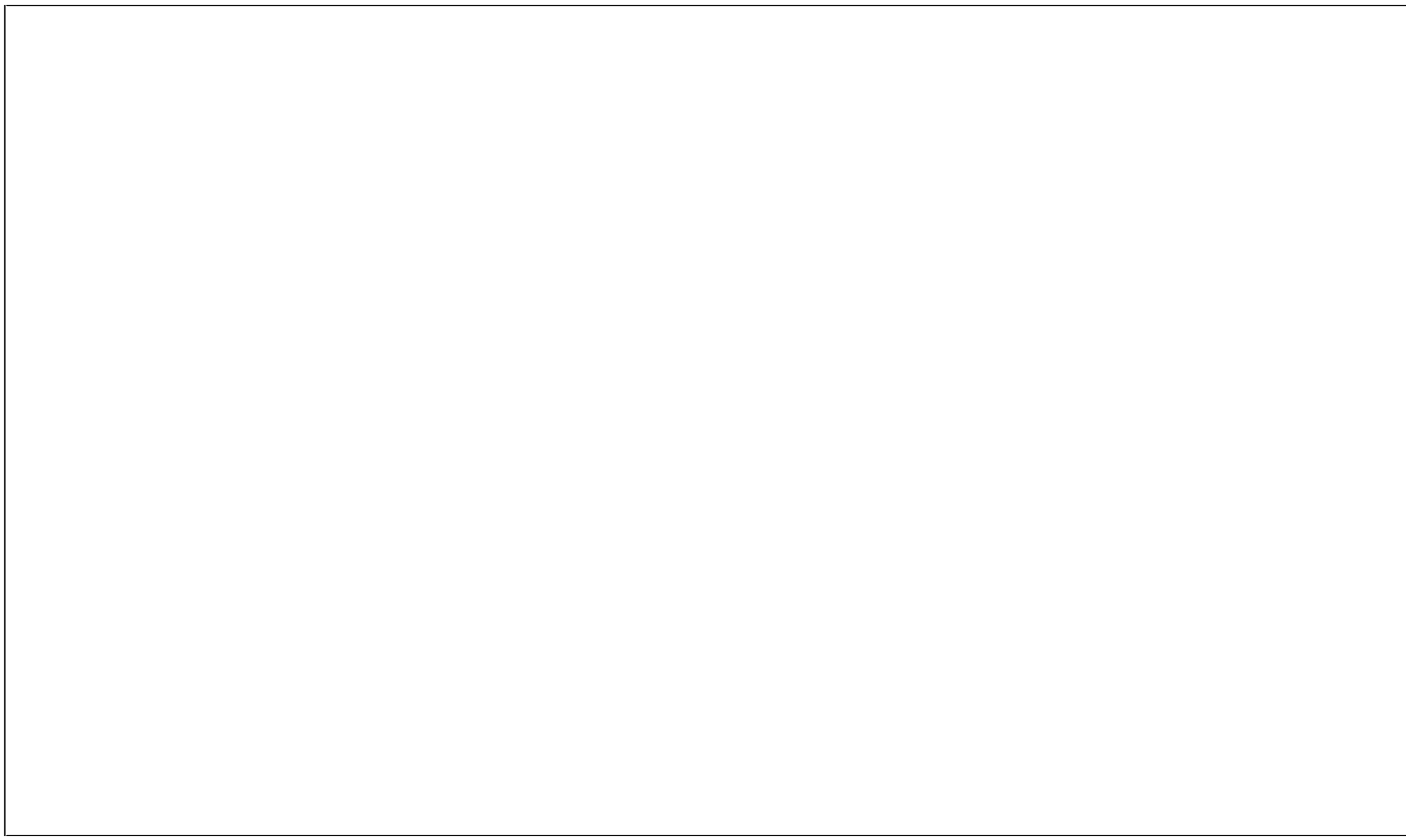

ICs for Consumer Electronics

Single Chip PIP System

SDA 9288X (A141)

PIP 2

Data Sheet 03.96

Edition 03.96

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SDA 9288X **Revision History:**		**Current Version: 03.96**
Previous Version:		
Page (in previous Version)	Page (in new Version)	Subjects (major changes since last revision)
		25.1.1994: Preliminary Specification V1.1
	22; 23; 24	25.1.1994: warnings
	24	25.1.1994: additional bits VSIISQ, VSPISQ at subad. 07/08
	25	25.1.1994: additional bits DACONDE, DACONST at subad. 0D
	26	25.1.1994: supply voltage range
	32	25.1.1994: values DAC
	35	25.1.1994: diagram
	43	25.1.1994: influence HSIDEL to VSIDEL adjustment
	19; 21	19.4.1994: additional note PLL switch READ27
	43	19.4.1994: timing of ADC clamping
	15	20.6.1994: warning subaddr. 02
	20; 25	20.6.1994: additional bit SELDOWN at subaddr. 0B
	23	20.6.1994: value V_{OL} outputs SEL, SELD added
	All	18.7.1994: pages no. shifted
	10; 15; 18	18.7.1994: improvement: additional bits D5, D6 (CLPS; CLPFIX) at subaddr. 06
	15; 19	18.7.1994: bit D0 of subaddress 0D deleted
	17	18.7.1994: new: examples for adjustment of frame colors
	17	18.7.1994: text bits IMOD, PMOD
	22	18.7.1994: additional remark at subaddress 02
	25	18.7.1994: clamping current. Additional values
	28; 29	18.7.1994: application board layout and application circuit new
	30	18.7.1994: timing of ADC clamping changed
	32	18.7.1994: values DAC output current

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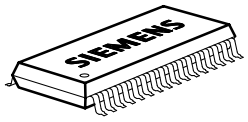
I²C Bus

Purchase of Siemens I²C components conveys the license under the Philips I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips.

1 General Description

The Picture-in-Picture Processor SDA 9288X A141 generates a picture of reduced size of a video signal (inset channel) for the purpose of combining it with another video signal (parent channel). The easy implementation of the IC in an existing system needs only a few additional external components. There is a great variety of application facilities in professional and consumer products (TV sets, supervising monitors, multi-media, …)

1.1 Features



P-DSO-32-2

- **Single chip solution**
  Clamping, AD conversion, filtering, field memory, RGB matrix, DA-conversion and clock generation integrated on one chip
- **2 picture sizes**
  1/9 or 1/16 of normal size
- **High resolution display**
  13.5 MHz/27 MHz display clock frequency
  212 luminance and 53 chrominance pixels per inset line for picture size 1/9
  6-bit amplitude resolution for each incoming signal component
  Field and frame mode display
  Horizontal and vertical filtering
  Special antialias filtering for the luminance signal
- **16:9 compatibility**
  Operation in 4:3 and 16:9 sets
  4:3 inset signals on 16:9 displays or v.v. with picture size 1/9 and 1/16, respectively
- **Analog inputs**
  Y, + (B-Y), + (R-Y) or Y, -(B-Y), -(R-Y)
- **Analog outputs**
  Y, + (B-Y), + (R-Y) or Y, – (B-Y), – (R-Y) or RGB
  3 RGB matrices: EBU, NTSC (Japan), NTSC (USA)
- **Free programmable position of inset picture**
  Steps of 1 pixel and 1 line
  All PIP and POP positions are possible
- **Programmable framing**
  4096 frame colors
  Variable frame width

Type	Ordering Code	Package
SDA 9288X	on request	P-DSO-32-2

- **Freeze picture**
- **I^2C Bus control**
- **Threefold PIP/POP facility**
  Three different I^2C-addresses (pin-programmable)
  Tri-State outputs
- **Numerical PLL circuit for high stability clock generation**
- **No necessity of PAL/SECAM delay lines**
  (using suitable color decoders i.e. TDA 8310)
- **Multistandard applications**
  625 lines/525 lines standard (inset and parent channel)
  Scan conversion systems as flickerfree display systems (parent channel)
  HDTV (parent channel)
- **P-DSO-32-2 package/350 mil (SMD)**
- **5 V supply voltage**

1.2 Pin Configuration

(top view)

P-DSO-32-2

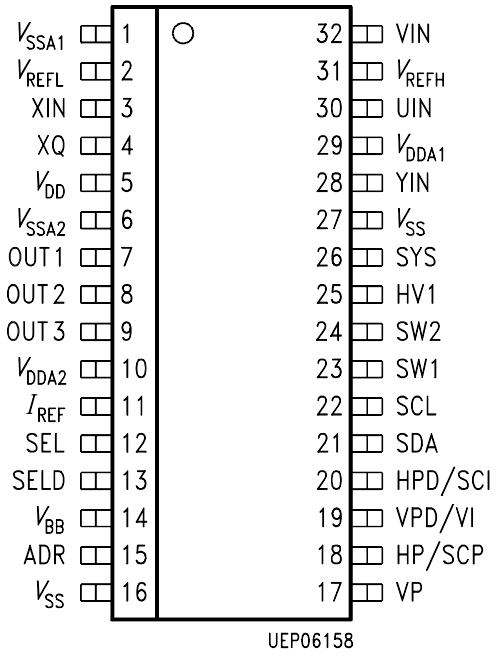


Figure 1

1.3 Pin Definitions and Functions

Pin No.	Symbol	Function[1)]	Descriptions
1	V_{SSA1}	S	Analog voltage supply (V_{SS}) for ADC
2	V_{REFL}	I	Lower reference voltage for AD converters
3	XIN	I	Quartz oscillator (input) or quartz clock (from another PIP IC) or line locked clock (27 MHz, from a digital parent channel)
4	XQ	Q	Quartz oscillator (output)
5	V_{DD}	S	Digital voltage supply (V_{DD})
6	V_{SSA2}	S	Analog voltage supply (V_{SS}) for DAC and PLL
7	OUT1	Q/ana	Analog output: chrominance signal + (R-Y) or – (R-Y) or R
8	OUT2	Q/ana	Analog output: luminance signal Y or G
9	OUT3	Q/ana	Analog output: chrominance signal + (B-Y) or – (B-Y) or B
10	V_{DDA2}	S	Analog voltage supply (V_{DD}) for DAC and PLL
11	I_{REF}	Q/ana	Reference current for DA-converters
12	SEL	Q	Single frequency fast PIP switching output (tristate)
13	SELD	Q	Double frequency fast PIP switching output (tristate)
14	V_{BB}	S	Capacitor connection for smoothing internally generated substrate bias
15	ADR	$I_{3\text{-}L}$	I^2C Bus address control
16,27	V_{SS}	S	Digital voltage supply (V_{SS})
17	VP	I	Multifrequency vertical sync for parent channel
18	HP/SCP	I	Multifrequency horizontal sync for parent channel
19	VPD/VI	I	Double frequency vertical sync for parent channel or vertical sync input for inset channel
20	HPD/SCI	I	Double frequency horizontal sync for parent channel or horizontal sync input for inset channel
21	SDA	I/Q	I^2C Bus data
22	SCL	I	I^2C Bus clock
23	SW1	$Q_{3\text{-}L}$	I^2C Bus controlled output1
24	SW2	$Q_{3\text{-}L}$	I^2C Bus controlled output2

[1)] I : input, Q : output, ana : analog, TTL : digital (TTL), 3-L : 3-level, S : supply voltage

1.3 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function[1)]	Descriptions
25	HVI	$I_{3\text{-}L}$	Special 3-level hor. and vert. sync signal for inset channel
26	SYS	$I_{3\text{-}L}$	Input for standard depending internal switching (LOW (L) = PAL, MID (M) = NTSC, HIGH (H) = SECAM)
28	YIN	I/ana	Analog input: luminance signal Y
29	VDDA1	S	Analog voltage supply (V_{DD}) for ADC
30	UIN	I/ana	Analog input: chrominance signal + (B-Y) or – (B-Y)
31	VREFH	I	Upper reference voltage for AD converters
32	VIN	I/ana	Analog input: chrominance signal + (R-Y) or – (R-Y)

I : input, Q : output, ana : analog, TTL : digital (TTL), 3-L : 3-level, S : supply voltage

1.4 Functional Block Diagram

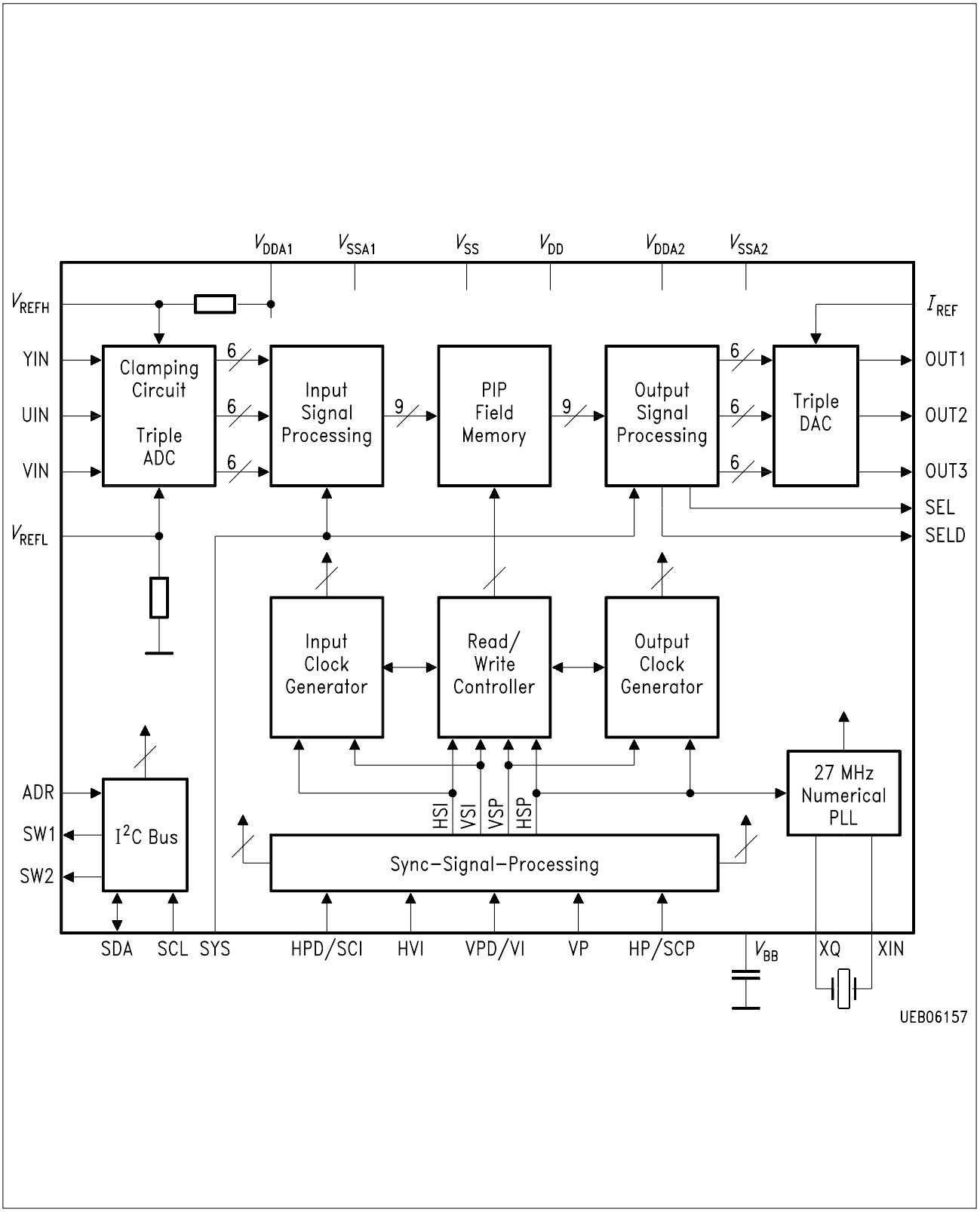


Figure 2

2 System Description

2.1 AD Conversion, Inset Synchronization

The inset video signal is fed to the SDA 9288X A141 as analog luminance and chrominance components[1]. The polarity of the chrominance signals is programmable. After clamping the video components are AD-converted with an amplitude resolution of 6 bit. The conversion is done using a 13.5 MHz clock for the luminance signal and a 3.375 MHz clock for the chrominance signals.

For the adaption to different application the clamp timing for the analog inputs can be chosen (CLPS; CLPFIX). Setting this bits to '1' can be useful for non-standard input signals.

For inset synchronization it is possible to feed either a special 3-level signal via pin HVI (detection of horizontal and vertical pulses) or separate signals via pins SCI for horizontal and VI for vertical synchronization. SCI is the horizontal synchron signal of the inset channel. If the burst gate pulse of the sandcastle is used it must be adapted to TTL compatible levels by a simple external circuit. Centering of the displayed picture area is possible by a programmable delay for the horizontal synchronization signal (HSIDEL).

The inset horizontal synchronization signals are sampled with 27 MHz. This 27 MHz clock and the AD converter clocks are derived from the parent horizontal synchronization pulse (see **chapter 2.6**) or from the quartz frequency converted by a factor of 4/3.

Delay differences between luminance and chrominance signals at the input of the IC caused by chroma decoding are compensated by a programmable luminance delay line (YDEL) of about – 290 ns … 740 ns (at decimation input; see **Application Information**).

By analyzing the synchronization pulses the line standard of the inset signal source is detected and interference noise on the vertical sync signal is removed. For applications with fixed line standard (only 625 lines or 525 lines) the automatic detection can be switched off.

The phase of the vertical sync pulse is programmable (VSIDEL; VSPDEL). By this way a correct detection of the field number is possible, an important condition for frame mode display.

*Note: The adjustment of VSIDEL is influenced by HSIDEL (see **chapter 4.3**), vertical synchronization via pin HVI causes an additional internal delay for the vertical sync pulse of about 16 µs.*

[1] To improve the signal-to-noise ratio the amplitude of the input signals should be as large as possible.

2.2 Input Signal Processing

This stage performs the decimation of the inset signal by horizontal and vertical filtering and sub-sampling. A special antialias filter improves the frequency response of the luminance channel. It is optimized for the use of the horizontal decimation factor 3:1.

A window signal, derived from the sync pulses and the detected line standard, defines the part of the active video area used for decimation. For HSIDEL = ‘0’ the decimation window is opened about 104 clock periods (13.5 MHz) after the horizontal synchronization pulse. For the 625 lines standard the 36th video line is the first decimated line, for the 525 lines standard decimation starts in the 26th video line.

The following filters are implemented:

Horizontal Decimation	Component	Filter
3:1	Luminance	$1 + z^{-1} + z^{-2}$
3:1	Chrominance	$1 + 2 \times z^{-1} + z^{-2}$
4:1	Luminance	$1 + z^{-1} + z^{-2} + z^{-3}$
4:1	Chrominance	$1 + z^{-1} + z^{-2} + z^{-3}$

Vertical Decimation	Component	Filter
3:1	Luminance	$1 + z^{-L} + z^{-2L}$
3:1	Chrominance	$1 + 2 \times z^{-L} + z^{-2L}$
4:1	Luminance	$1 + z^{-L} + z^{-2L} + z^{-3L}$
4:1	Chrominance	$1 + z^{-L} + z^{-2L} + z^{-3L}$

$z = e^{j\omega T}$, T = 1/13.5 MHz for luminance T = 1/3.375 MHz for chrominance
L = samples per line for luminance respectively chrominance

The realized chrominance filtering allows omitting the color decoder delay line for PAL and SECAM demodulation if the color decoder supplies the same output voltages independent of the kind of operation. In case of SECAM signals an amplification of the chrominance signals by a factor of 2 is necessary because just every second line a signal is present. This chrominance amplification is programmable via pin SYS or I^2C Bus (AMSEC).

The horizontal and vertical decimation factors are free programmable (DECHOR, DECVER). Using different decimations horizontal and vertical 16:9 applications become realizable:

DECHOR = ‘1’, DECVER = ‘0’: picture size 1/9 for 4:3 inset signals on 16:9 displays

DECHOR = ‘0’, DECVER = ‘1’: picture size 1/16 for 16:9 inset signals on 4:3 displays

2.3 PIP Field Memory

The on-chip memory stores one decimated field of the inset picture. Its capacity is 169 812 bits. The picture size depends on the horizontal and vertical decimation factors.

Horizontal Decimation	PIP PIXELS per Line		
	Y	(B-Y)	(R-Y)
3:1	212	53	53
4:1	160	40	40

Vertical Decimation	Line Standard	PIP Lines
3:1	625	88
3:1	525	76
4:1	625	66
4:1	525	57

In field mode display just every second inset field is written into the memory, in frame mode display the memory is continuously written. Data are written with the lower inset clock frequency depending on the horizontal decimation factor (4.5 MHz or 3.375 MHz). Normally the read frequency is 13.5 MHz and 27 MHz for scan conversion systems. For progressive scan conversion systems and HDTV displays a line doubling mode is available (LINEDBL). Every line of the inset picture is read twice.

Memory writing can be stopped by program (FREEZE), a freeze picture display results (one field).

Having no scan conversion and the same line numbers in inset and parent channel (625 lines or 525 lines both) frame mode display is possible. The result is a higher vertical and time resolution because of displaying every incoming field. For this purpose the standards are internally analysed and activating of frame mode display is blocked automatically when the described restrictions are not fulfilled.

As in the inset channel a field number detection is carried out for the parent channel. Depending on the phase between inset and parent signals a correction of the display raster for the read out data is performed by omitting or inserting lines when the read address counter outruns the write address counter.

The display position of the inset picture is free programmable (POSHOR, POSVER). The first possible picture position (without frame) is 54 clock periods (13.5 MHz or 27 MHz) after the horizontal and 4 lines after the vertical synchronization pulses. Starting at this position the picture can be moved over the whole display area. Even POP-positions (Picture Outside Picture) at 16:9 applications are possible.

Having different line standards in inset and parent channels we have a so called mixed mode display. It causes deformations in the aspect ratio of the inset picture. A special mixed mode display is available for the picture size 1/9 (MIXDIS):

– Parent channel 625 lines, inset channel 525 lines: The inset picture is shifted down by 6 lines. By performing this shifting the centers of the inset pictures have the same position for both line standards.
– Parent channel 525 lines, inset channel 625 lines: The inset picture gets a reduced line number of 76. The first and the last 6 lines are omitted. This way the inset picture size is the same as for 525 lines inset signals. The display shows the center part of the original picture.

Synchronization of memory reading with the parent channel is achieved by processing the parent horizontal and vertical synchronization signals in the same way as described for the inset channel. The synchronization signals are fed to the IC at pin HP/SCP for horizontal synchronization and pin VP for vertical synchronization. In the same way as described for the inset channel the burst gate of the sandcastle signal can be used for horizontal synchronization. In scan conversion systems also the inputs HPD/SCI and VPD/VI are available if the input HVI is activated for inset synchronization.

2.4 Output Signal Processing

At the memory output the chrominance components are demultiplexed and linearly interpolated to the luminance sample rate.

Different output formats are available: luminance signal Y with inverted or non-inverted chrominance signals (B-Y), (R-Y) or RGB. For the RGB conversion 3 matrices are integrated:

Standard	B-Y	R-Y	G-Y	B-Y	R-Y	G-Y
EBU	1	0.558	0.345	0°	90°	237°
NTSC (Japan)	1	0.783	0.31	0°	95°	240°
NTSC (USA)	1	1.013	0.305	0°	104°	252°

Matrix selection is done by pin SYS or I^2C Bus. The matrices are designed for the following input voltages (100 % white, 75 % color saturation):

Component	Input Voltage (without sync) in % of Full Scale Input Range of ADC
Y	75
B-Y	100
R-Y	100

2.4.1 Matrix Equations

EBU

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ 0 & 0.78125 & 1 \\ -0.1875 & -0.40625 & 1 \end{bmatrix} \begin{bmatrix} B-Y \\ R-Y \\ Y \end{bmatrix}$$

NTSC (Japan)

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -0.0625 & 1.09375 & 1 \\ -0.15625 & -0.375 & 1 \end{bmatrix} \begin{bmatrix} B-Y \\ R-Y \\ Y \end{bmatrix}$$

NTSC (USA)

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -0.25 & 1.375 & 1 \\ -0.09375 & -0.40625 & 1 \end{bmatrix} \begin{bmatrix} B-Y \\ R-Y \\ Y \end{bmatrix}$$

2.4.2 Frame Insertion

A colored frame is added to the inset picture. 4096 frame colors are programmable, 4 bits for each component Y, (B-Y), (R-Y) (bits FRY, FRU, FRV). The horizontal and

vertical width of the frame are independently programmable. Width = 0 means display without frame.

Examples for the Adjustment of Frame Colors

Frame Color	FRY D3 … D0 of Subaddress 09	FRU D3 … D0 of Subaddress 0A	FRV D7 … D4 of Subaddress 0A
Blue	0100	0110	1010
Green	0100	1000	1010
White	1100	0000	0000
Red	0100	1000	0111
Yellow	1100	1000	0100
Cyan	1100	0010	1010
Magenta	0100	0110	0100

2.4.3 Select Signal

For controlling an external switch (for example an RGB processor) a select signal is supplied. Pin SEL is active in normal 13.5 MHz reading mode, pin SELD is active using 27 MHz. The phases of these signals are programmable for adaption to different external output signal processing.

2.5 DA Conversion

The SDA 9288X A141 includes three 6-bit DA converters. Each converter supplies a current through an external resistor that is connected between V_{SSA} and OUT1, OUT2, OUT3 respectively. The current is controlled by a digital control circuit. Each command DACONST or PIPON starts the adjustment cycle.

2.6 PLL

A numerical PLL circuit supplies a clock of about 27 MHz with high stability. The generated clock is locked to the parent horizontal synchronization pulse. Its frequency depends linearly on the frequency of the sync signal and the quartz frequency. The recommended quartz frequencies are listed under 'Recommended Operation Conditions'. Using up to three SDA 9288X A141 ICs in one application only a single quartz is necessary. Four time constants are programmable via I²C Bus. If the PLL is switched off an external 27 MHz parent line locked clock can be fed to the IC.

The inset clock generation is possible in two ways:

1. Synchron with the parent horizontal synchronization pulse (bit CLISW = '0')
2. Synchron with the quartz frequency (bit CLISW = '1'; $f_{cli} = 4/3 \times f_{quartz}$). In this mode the aspect ratio is independent on the parent sync frequency but depends on the used resonator type. It is only possible to use one of the two modes.

Note: Before setting bit D3 of subaddress 00 (READ27) noise reduction of the VSP pulse must be switched off (D5 of subaddress 08 = '1').

2.7 I²C Bus

2.7.1 I²C Bus Addresses

Three different I²C addresses are programmable via pin ADR.

Pin ADR	Address (bin.)	Address (hex.)
Low level (V_{SS} or V_{SSA})	11010110	D6
Mid level (open)	11011100	DC
High level (V_{DD} or V_{DDA})	11011110	DE

2.7.2 I²C Bus Receiver Format

S	Address	A	Subaddress	A	Data Byte	A	****	A	P

S: start condition A: acknowledge P: stop condition

Only write operation is possible. An automatically address increment function is implemented.

2.7.3 I²C Bus Commands

Sub-addr.	Data Bytes							
Hex	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00	0	SYSACT	FREEZE	PLLOFF	READ27	LINEDBL	FRAME	PIPON
01	0	SELDEL3	SELDEL2	SELDEL1	SELDEL0	MIXDIS	POSHOR9	POSHOR8
02	POSHOR7	POSHOR6	POSHOR5	POSHOR4	POSHOR3	POSHOR2	POSHOR1	POSHOR0
03	POSVER7	POSVER6	POSVER5	POSVER4	POSVER3	POSVER2	POSVER1	POSVER0
04	0	SW21	SW20	SW11	SW10	YDEL2	YDEL1	YDEL0
05	DECVER	DECHOR	INSHVI	CHRINS	PMOD1	PMOD0	IMOD1	IMOD0
06	0	CLPS	CLPFIX	CLISW	HSIDEL3	HSIDEL2	HSIDEL1	HSIDEL0
07	AMSEC	0	VSIISQ	VSIDEL4	VSIDEL3	VSIDEL2	VSIDEL1	VSIDEL0
08	PARSYND	0	VSPISQ	VSPDEL4	VSPDEL3	VSPDEL2	VSPDEL1	VSPDEL0
09	CON3	CON2	CON1	CON0	FRY5	FRY4	FRY3	FRY2
0A	FRV5	FRV4	FRV3	FRV2	FRU5	FRU4	FRU3	FRU2
0B	0	0	SELDOWN	FRWIDV1	FRWIDV0	FRWIDH2	FRWIDH1	FRWIDH0
0C	0	0	0	MAT2	MAT1	MAT0	CHRPIP	OUTFOR
0D	DACONST	PLLTC1	PLLTC2	0	0	0	0	0

After switching on the IC the data bytes of all registers are set to ‘0’, the bit PLLOFF is set to ‘1’.

Bit	Name	Function
Subaddress 00		
D0	PIPON	0: PIP insertion OFF 1: PIP insertion ON
D1	FRAME	0: field display 1: frame display (under special restrictions). Correct adjustment of bits VSIDEL, VSPDEL required (see **chapter 4.3**)
D2	LINEDBL	0: each line of the PIP memory is read once (normal operation) 1: each line of the PIP memory is read twice (line doubling for progressive scan conversion systems in parent channel)
D3	READ27	0: PIP display with single read frequency (13.5 MHz) 1: PIP display with double read frequency (27 MHz) (see **note page 19**).
D4	PLLOFF	0: internal PLL ON 1: internal PLL OFF (external clock generation)
D5	FREEZE	0: live picture 1: freeze picture
D6	SYSACT	0: pin SYS inactive: selection of decimation amplification and RGB-matrix is done via I^2C Bus 1: pin SYS active: selection of decimation amplification and RGB-matrix is done via pin SYS
Subaddress 01		
D1 … D0	POSHOR	2 MSBs of POSHOR (see also subaddress 02)
D2	MIXDIS	0: PIP picture height depends just upon inset line standard, position upon POSHOR 1: modified PIP picture height and position for different inset and parent line standards (mixed display mode)
D6 … D3	SELDEL	Delay of output signal SELECT at pins SEL respectively SELD (– 8 … 7 periods of read frequency clock, programmable in 2's complement code). SELDEL = '0': SELECT signal has the same phase as the PIP picture signal referenced to the IC output.

Bit	Name	Function
Subaddress 02		
D7 … D0	POSHOR	Horizontal position of PIP picture (raster: 1 pixel) *Note: The 2 MSBs of POSHOR are located at subaddress 01* **Warning:** It is not allowed to adjust positions < 2 and > 740. *Note: To avoid horizontal jumping of the picture by changing POSHOR from '00 1111 1111' to '01 0000 0000' its necessary to transfer the bits of **both** subaddresses during the same field period.*
Subaddress 03		
D7 … D0	POSVER	Vertical position of PIP picture (raster: 1 line) **Warning:** It is not allowed to adjust positions > 220 (50 Hz) or > 182 (60 Hz).
Subaddress 04		
D2 … D0	YDEL	Delay of luminance input signal 000: minimum delay 111: maximum delay; see **chapter 4.2**
D4 … D3	SW1	Direct control of output pin SW1 (3 levels) 00: low level 01: mid level 10: high level 11: high level
D6 … D5	SW2	Direct control of output pin SW2 (3 levels) 00: low level 01: mid level 10: high level 11: high level

Bit	Name	Function
Subaddress 05		
D1 … D0	IMOD	00: automatic detection of line standard (inset signal) 01: fixed adjustment 625 lines[1)] 10: fixed adjustment 525 lines[1)] 11: freeze last line standard
D3 … D2	PMOD	00: automatic detection of line standard (parent signal) 01: fixed adjustment 625 lines[1)] 10: fixed adjustment 525 lines[1)] 11: freeze last line standard
D4	CHRINS	0: chrominance input signals + (B-Y), + (R-Y) 1: inverted chrominance input signals – (B-Y), – (R-Y)
D5	INSHVI	0: inset synchronization signals via pins HPD/SCI and VPD/VI 1: inset synchr. signals via pin HVI (3-I. sand-castle signal)
D6	DECHOR	0: horizontal decimation 3 to 1 1: horizontal decimation 4 to 1
D7	DECVER	0: vertical decimation 3 to 1 1: vertical decimation 4 to 1
Subaddress 06		
D3 … D0	HSIDEL	Delay of horizontal synchronization pulse (inset signal) Raster: 6 clock periods of 13.5 MHz. **Warning:** Adjustment of HSIDEL will influence the adjustment of VSIDEL (subaddr. 07); see **chapter 4.3**
D4	CLISW	0: inset clock synchronized with parent clock 1: inset clock synchronized with quartz frequency *Note: Only one of the two modes can be used. Switching back from '1' to '0' is not possible!*
D5	CLPFIX	0: clamp pulses of ADC are dependent on the adjustment of HSIDEL 1: clamp pulses fixed; no influence of HSIDEL
D6	CLPS	0: three clamp cycles per line (timing see diagram) 1: two clamp cycles per line

[1)] Fixed adjustments for IMOD and PMOD result in undefined working conditions when signal standards are used which are different from the programmed values.

Bit	Name	Function
Subaddress 07		
D4 … D0	VSIDEL	Delay of vertical synchronization pulse (inset signal) in steps of 2.37 µs. **Warning:** Correct adjustment value is influenced by the adjustment of HSIDEL (subaddr. 06); see **chapter 4.3**.
D5	VSIISQ	Noise reduction of the VSI pulse (set to '0' under normal conditions)
D7	AMSEC	0: unity amplification of decimation filters (normal mode) 1: amplification by a factor of 2 (SECAM signals without delay line in the chroma decoder)
Subaddress 08		
D4 … D0	VSPDEL	Delay of vertical synchronization pulse (parent signal) in steps of 2.37 µs/1.68 s (50/100 Hz)
D5	VSPISQ	Noise reduction of the VSP pulse (should be set to '0' under normal conditions); in case changing from standard mode to line or frame conversion modes '1' should be set during the changement of line frequency
D7	PARSYND	0: parent synchronization signals for double frequency read via pins HP/SCP and VP 1: parent synchronization signals for double frequency read via pins HPD/SCI and VPD/VI (INSHVI = '1' required)
Subaddress 09		
D3 … D0	FRY	Luminance component of frame color (4 MSBs of 6 bit)
D7 … D4	CON	Contrast adjustment of PIP picture; steps and adjustment range depending on the external output resistors. Proposed value see **chapter 3.3**
Subaddress 0A		
D3 … D0	FRU	Chrominance component (B-Y) of frame color (4 MSBs of 6 bit)
D7 … D4	FRV	Chrominance component (R-Y) of frame color (4 MSBs of 6 bit)

Bit	Name	Function
Subaddress 0B		
D2 … D0	FRWIDH	Horizontal width of PIP frame (0 … 7 pixels)
D4 … D3	FRWIDV	Vertical width of PIP frame (0 … 3 lines)
D5	SELDOWN	0: open source output at pins SEL, SELD 1: TTL output at pins SEL, SELD
Subaddress 0C		
D0	OUTFOR	0: format of output signals: Y, (B-Y), (R-Y) 1: format of output signals: R G B
D1	CHRPIP	0: chrominance output signals: + (B-Y), + (R-Y) 1: inverted chrominance output signals: – (B-Y), – (R-Y)
D2	MAT0	0: EBU RGB-matrix 1: NTSC RGB-matrix
D3	MAT1	0: preselection of NTSC RGB matrix (USA) 1: preselection of NTSC RBG matrix (Japan)
D4	MAT2	0: matrix selection by bit MAT0 1: automatic matrix selection depending on inset line standard
Subaddress 0D		
D0	DACONDE	Set to ‘0’
D5 D6	PLLTC2 PLLTC1	Time constant of internal PLL: 00: medium damping, low resonance frequency 01: medium damping, high resonance frequency 10: high damping, low resonance frequency 11: high damping, high resonance frequency *Note: After power ON PLLTC must remain at 00 until the system is locked.*
D7	DACONST	Changing from ‘0’ to ‘1’ starts automatic adjustment of OUT1 … 3 output current (switching PIPON gives the same result).

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
Ambient temperature	T_A	0	70	°C	
Storage temperature	T_{stg}	– 55	125	°C	
Junction temperature	T_j		125	°C	
Soldering temperature	T_{SOLD}		260	°C	Duration < 10 s
Input voltage	V_I	– 0.5 V	V_{DD} + 0.5 V	1	Analog inputs (YIN, UIN, VIN, I_{REF})
	V_I	– 1	7	V	All other pins
Output voltage	V_Q	– 0.5 V	V_{DD} + 0.5 V	1	Pins OUT1, OUT2, OUT3, XQ, SW1, SW2
	V_Q	– 1	7	V	All other pins
Supply voltages	V_{DD}	– 1	7	V	
Supply voltage differentials	$V_{DD\ D}$	– 0.25	0.25	V	
Total power dissipation	P_{tot}		900	mW	
Latch-up protection		– 100	100	mA	Except pins OUT1, OUT2, OUT3, I_{REF}, XQ, XQ, YIN, UIN, VIN

Note: All voltages listed are referenced to ground (0 V, V_{SS}) except where noted. Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 Operational Range

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Supply voltages	V_{DDxx}	4.75	5	5.5	V	
Ambient temperature	T_A	0	25	70	°C	
All TTL Inputs						
Low-level input voltage	V_{IL}	– 1		0.8	V	
High-level input voltage	V_{IH}	2.0		6	V	
All Three Level Inputs (3-L) (see figure)						
High-level input voltage	V_{IH}	3.5		6	V	
Low-level input voltage	V_{IL}	– 1		0.8	V	
Medium-level voltage	V_{IM}					Open input, see **chapter 3.3**
All 3-L Outputs (see figure)						
High-level output current	I_{OH}	– 500		0	µA	
Low-level output current	I_{OL}	0		1.6	mA	
Inset Horizontal Sync TTL and 3-L Inputs: HPD/SCI, HVI[1)]						
Horizontal frequency		14.53		16.72	kHz	
Signal rise time				100	ns	Noisefree L/M-to-H transition
Signal high time		100			ns	
Signal medium or low time		900			ns	

[1)] All values are referred to the corresponding min (V_{IH}), max (V_{IM}) and max (V_{IL})

3.2 Operational Range (cont'd)

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Inset Vertical Sync TTL and 3-L Inputs: VPD/VI, HVI[1)]						
Signal medium or high time		17			µs	Necessary for vertical sync detection
Signal low time		200			ns	
Parent Horizontal Sync TTL Inputs: HP/SCP, HPD/SCI[2)]						
Sync frequency in single frequency display mode		14.53		16.72	kHz	Quartz frequency 20.480 MHz
		15		17.19	kHz	Quartz frequency 21.090 MHz
Sync frequency in double frequency display mode		29.06		33.44	kHz	Quartz frequency 20.480 MHz
		30		34.375	kHz	Quartz frequency 21.090 MHz
Signal rise time				100	ns	Noisefree transition
Signal high time		100			ns	
Signal low time		900			ns	
Parent Vertical Sync TTL Input VDP/VI[2)]						
Signal HIGH time		200			ns	
Signal LOW time		200			ns	

[1)] All values are referred to the corresponding min (V_{IH}), max (V_{IM}) and max (V_{IL})
[2)] All values are referred to the corresponding min (V_{IH}) and max (V_{IL})

3.2 Operational Range (cont'd)

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Quartz/Ceramic Resonator[2)]						
Recommended frequency		20.25	20.48	21.3	MHz	21.09 MHz for MUSE
Series resistance				10	Ω	C_1, $C_2 \leq 33$ pF
				20	Ω	C_1, $C_2 \leq 22$ pF
				30	Ω	C_1, $C_2 \leq 15$ pF
				40	Ω	C_1, $C_2 \leq 10$ pF (total series capacitance)
Optional TTL Clock Input: XIN[1)]						
Clock input cycle time		35		40	ns	External line locked; 27 MHz clock (I^2C: internal PLL OFF)
Clock input rise time				5	ns	
Clock input fall time				5	ns	
Clock input low time		10			ns	
Clock input high time		10			ns	
Fast I^2C Bus[1) 3)]						
SCL clock frequency	f_{SCL}	0		400	kHz	
Inactive time before start of transmission	t_{BUF}	1.3			µs	
Setup time start condition	$t_{SU;\,STA}$	0.6			µs	
Hold time start condition	$t_{HD;\,STA}$	0.6			µs	
SCL low time	t_{LOW}	1.3			µs	

1) All values are referred to min (V_{IH}) and max (V_{IL}).

2) There is no internal protection for the crystal driver against oscillation at harmonic frequencies.

3) This specification of the bus lines does not have to be identical with the I/O stages specification because of optional series resistors between bus lines and I/O pins.

3.2 Operational Range (cont'd)

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
SCL high time	t_{HIGH}	0.6			µs	
Setup time data	$t_{SU;\,DAT}$	100			ns	
Hold time data	$t_{HD;DAT}$	0		0.9	µs	
SDA/SCL rise/fall times	t_R, t_F	20 + $		300	ns	$ = 0.1C_b/pF
Setup time stop condition	$t_{SU;\,STO}$	0.6			µs	
Capacitive load/bus line	C_b			400	pF	
I²C Bus Inputs/Output: SDA, SCL						
High-level input voltage	V_{IH}	3		V_{DD} + 0.5	V	Also for SDA/SCL input stages
Low-level input voltage	V_{IL}	– 0.5		1.5	V	
Spike duration at inputs		0	0	50	ns	
Low-level output current	I_{OL}			6	mA	
Analog to Digital Converters (6 bit)						
Input coupling capacitors		10	100		nF	Necessary for proper clamping
Y, U, V source resistance				1	kΩ	
Reference voltage low	V_{REFL}	0.5	1.0	1.5	V	Min and max values only with optional external resistors, see also **chapter 3.3**.
Reference voltage high	V_{REFH}	1.5	2.0	2.5	V	
Reference voltage difference	$V_{REFH} - V_{REFL}$	0.5	1.0	2	V	

3.2 Operational Range (cont'd)

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Digital-to-Analog Converters (6 bit)						
Full range output voltage	V_{OFR}		1	2	V	Peak to peak
Reference resistance	R_{REF1}	4.2	5.1	6.3	kΩ	Bits CON = '0000'; no contrast adjustment used
	R_{REF2}	6.0	6.8	7.5	kΩ	Contrast adjustment via I^2C Bus

Note: In the operational range the functions given in the circuit description are fulfilled.

3.3 Characteristics

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
Average total supply current	I_{DDtot}		160	mA	$I_{DDtot} = I_{DD} + I_{DDA1} + I_{DDA2}$
Average digital supply current	I_{DD}		120	mA	*Note: The maxima do not necessarily coincide.*
Average analog supply current	I_{DDA1}		40	mA	
Average analog supply current	I_{DDA2}		20	mA	
All Digital Inputs (TTL, I²C)					
Input capacitance	C_I		7	pF	Not tested
Input leakage current		– 10	10	µA	Including leakage current of SDA output stage
All Three Level Inputs (3-L) (see figure)					
Input capacitance	C_I		7	pF	Not tested
Medium-level open input voltage	V_{IM}	2.1	2.5	V	$\|I_{IN}\| \leq 1$ µA, $V_{DD} = 5$ V
Differential input resistance	R_{IN}	8	14	kΩ	Not tested
SEL, SELD					
High-level output voltage	V_{OH}	2.4 V	V_{DD}	V	$I_{OH} = -200$ µA
High-level output voltage	V_{OH}	1.5 V	V_{DD}	V	$I_{OH} = -4.5$ mA
Low-level output voltage	V_{OL}		0.4	V	$I_{OL} = 1.6$ mA, only valid if bit SELDOWN = ‘1’
Leakage current		– 10		A	$V_O = 0$ V … V_{DD}
Output capacitance			7	pF	Not tested
All 3-L Outputs					
High-level output voltage	V_{OH}	4		V	$I_{OH} = -100$ µA
High-level output voltage	V_{OH}	3.9		V	$I_{OH} = -500$ µA
Low-level output voltage	V_{OL}		0.4	V	I_{OL} = max

3.3 Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
Medium-level output leakage current	I_{OM}	– 1	1	µA	Tristate
Output capacitance			7	pF	Not tested
I²C Inputs: SDA/SCL					
Schmitt trigger hysteresis	V_{hys}	0.2		V	Not tested
I²C Input/Output: SDA (referenced to SCL; open drain output)					
Low-level output voltage	V_{OL}		0.4	V	I_{OL} = 3 mA
Low-level output voltage	V_{OL}		0.6	V	I_{OL} = max
Output fall time from min (V_{IH}) to max (V_{IL})	t_{OF}	20 + 0.1 × C_b/pF	250	ns	10 pF ≤ C_b ≤ 400 pF
Analog-to-Digital Converters (6 bit)					
Y, U, V input leakage current		– 100	100	nA	
Y, U, V input capitance			7	pF	Not tested
Input clamping error		– 1	1	LSB	Settled state
Input clamping current	$\|I_{CLP}\|$	15 40 70	50 90 150	µA µA µA	Deviation < 1 LSB Deviation 1 … 2 LSB Deviation > 2 LSB
Reference voltage difference	V_{REFH} – V_{REFL}	0.98	1.02	V	V_{DDA} = nom, (V_{REFH} – V_{REFL} ≅ V_{DDA1}/5)
Digital-to-Analog Converters (6 bit): Current Source Outputs OUT1, OUT2, OUT3[1)]					
D.C. differential nonlinearity	DNLE	– 0.5	0.5	LSB	R_{REF} = 5.1 kΩ
Full range output current	I_O	– 1.4 2	– 1.7 3	mA	V_{DDA} = max, T_A = nom, R_{REF} = 5.1 kΩ, R_L = 680 Ω, after adjustment

3.3 Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
Output voltage (V_{ON} 1.6 × V_{DDA} × R_L/R_{REF})	V_O	0.96	1.18	V	V_{DDA} = max, T_A = nom, R_L = 680 Ω, R_{REF} = 5.1 kΩ, after adjustment
Tracking		– 3	3	%	V_{DDA} = max, T_A = nom, R_{REF} = 5.1 kΩ, R_L = 680 Ω
Contrast increase		30		%	V_{DDA} = nom, T_A = nom, R_L = 680 Ω, R_{REF} = 6.8 kΩ, contrast bits change from '0000' to '1111' for typical values see **chapter 4**
Supply voltage dependence of DAC output current					For typical values see **chapter 4**
Temperature dependence of DAC output current					For typical values see **chapter 4**
Dependence of DAC output current on external reference resistor					For typical values see **chapter 4**

[1] I^2C: Contrast bits set to zero unless otherwise noted.

Note: The listed characteristics are ensured over the operating range of the integrated circuit unless restricted to nominal operating conditions (all voltages refer to V_{SS}). The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

4 Diagrams

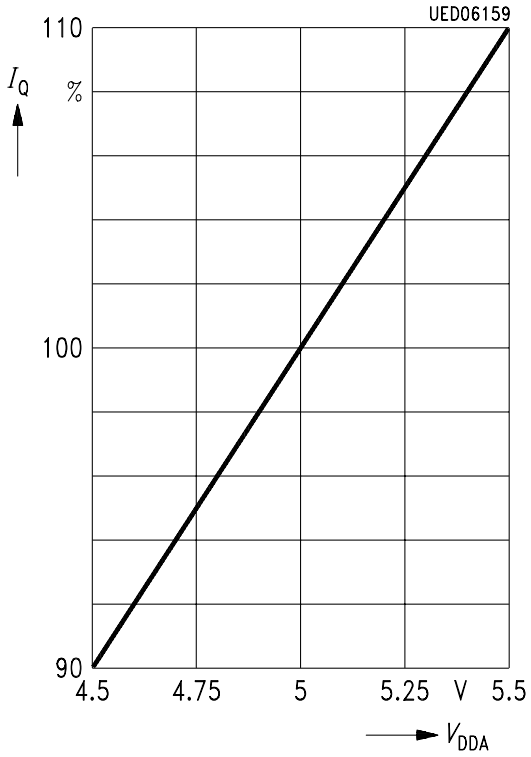
4.1 Output Current of DA Converters

Nominal values: V_{DDA} = 5 V; V_{REF} = 5.1 kΩ; T = 25 °C

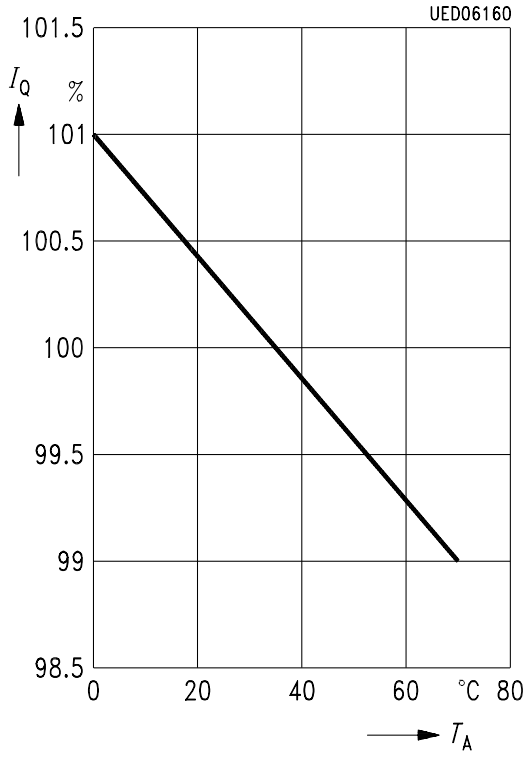
Measurements after adjustment via bit d7 of I²C Bus address 0D for each step

Note: The output currents are controlled in digital way, so inaccuracy of 1 LSB (ca. 2 %) is always possible.

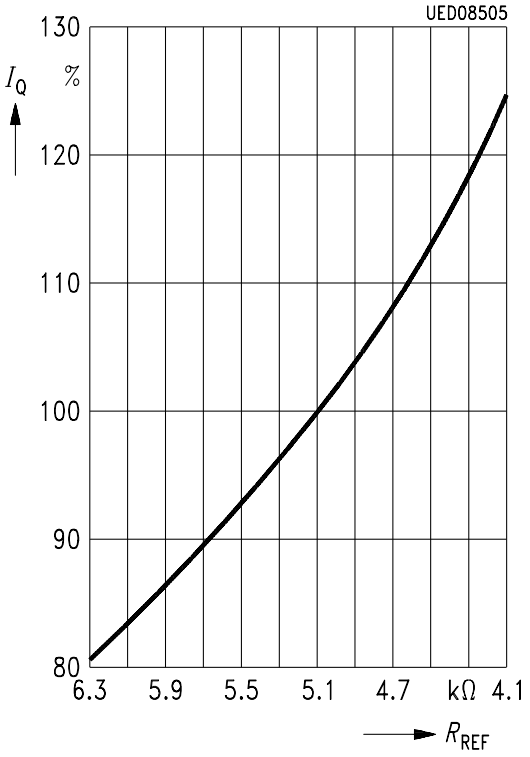
Output current = f (V_{DDA})



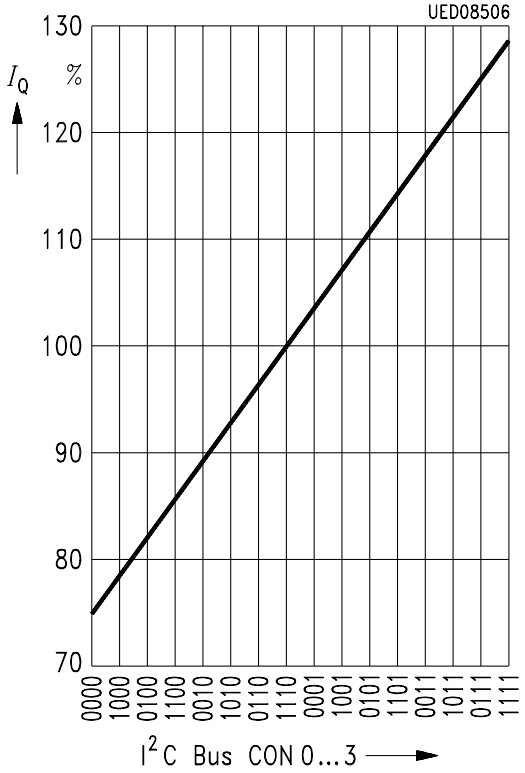
Output current = f (T_A)



Output current = f (R_{REF})



Current = f (CON 0 … 3)



4.2 Application Information

4.2.1 Reference Voltage Generation for ADC

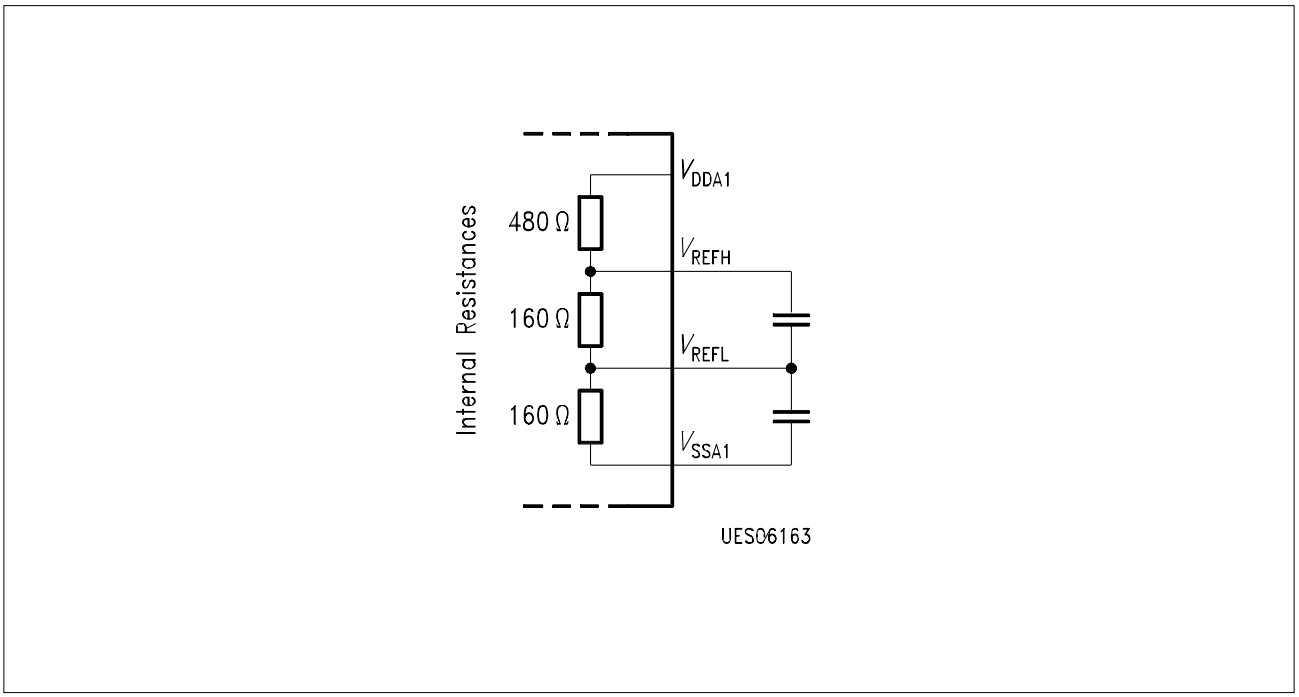


Figure 3
Signal Input Range 1 Vpp at Y, U, V

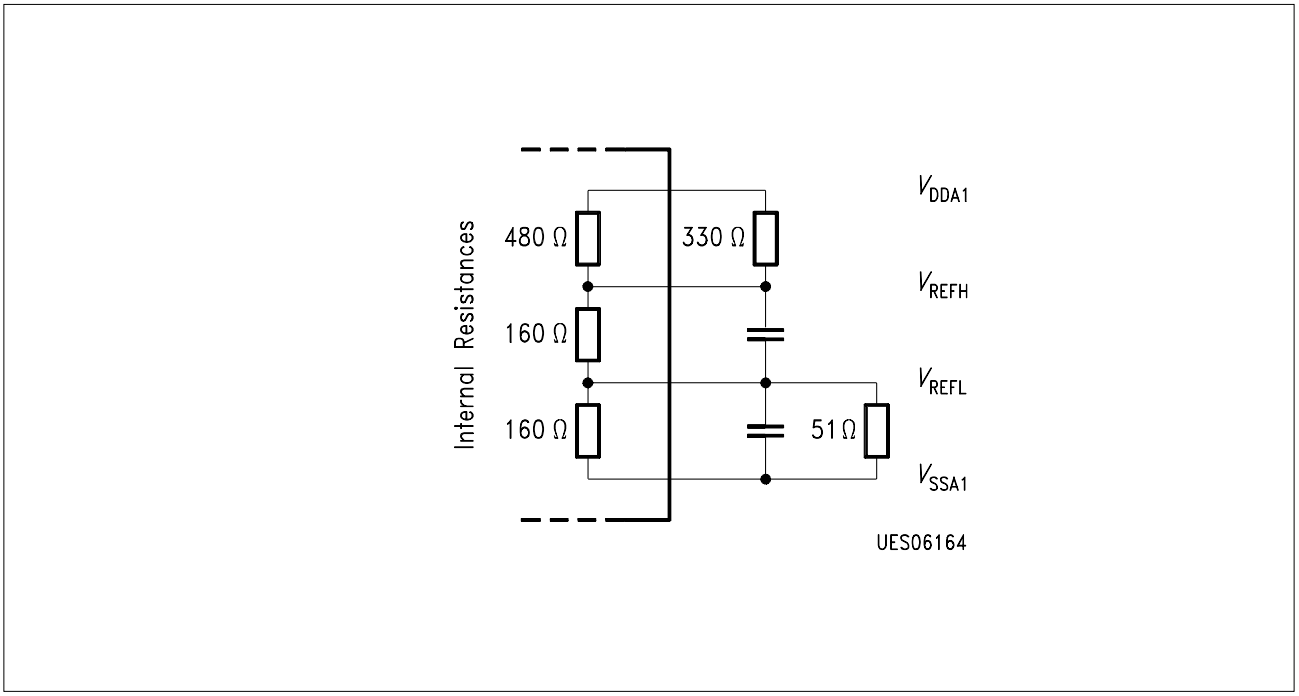


Figure 4
Signal Input Range 2 Vpp at Y, U, V

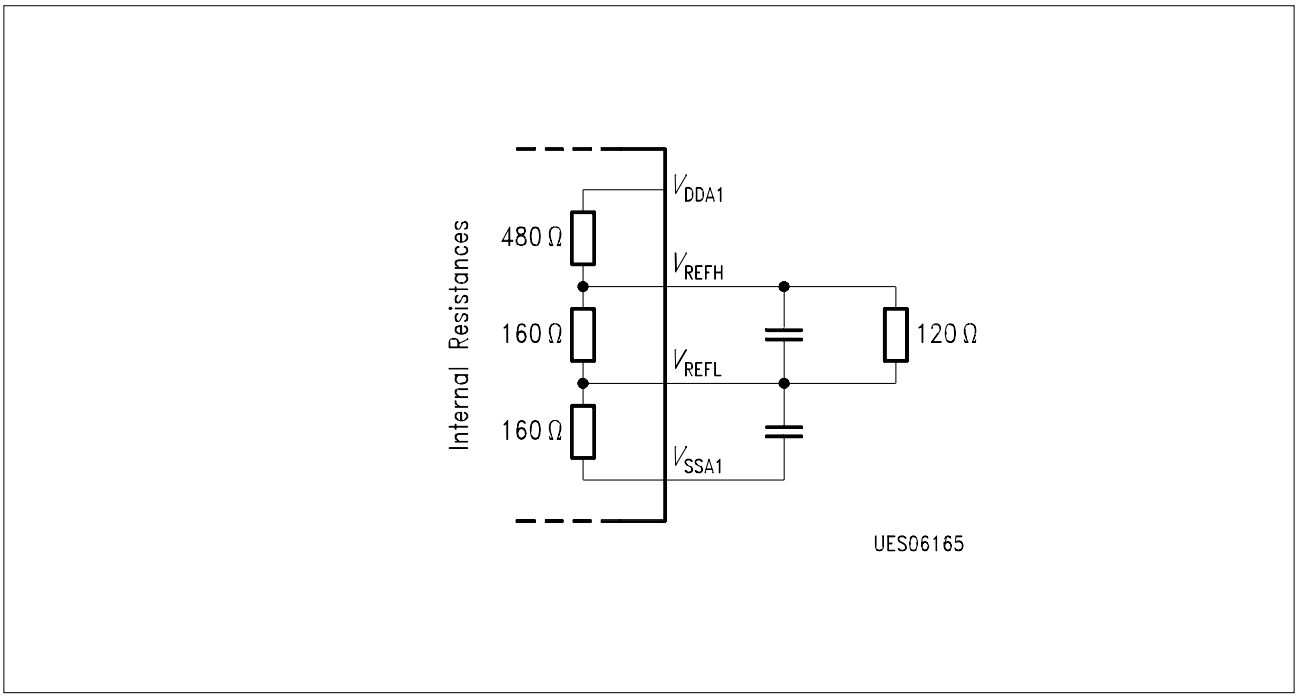


Figure 5
Signal Input Range 0.5 Vpp at Y, U, V

4.2.2 Adjustment of YDEL

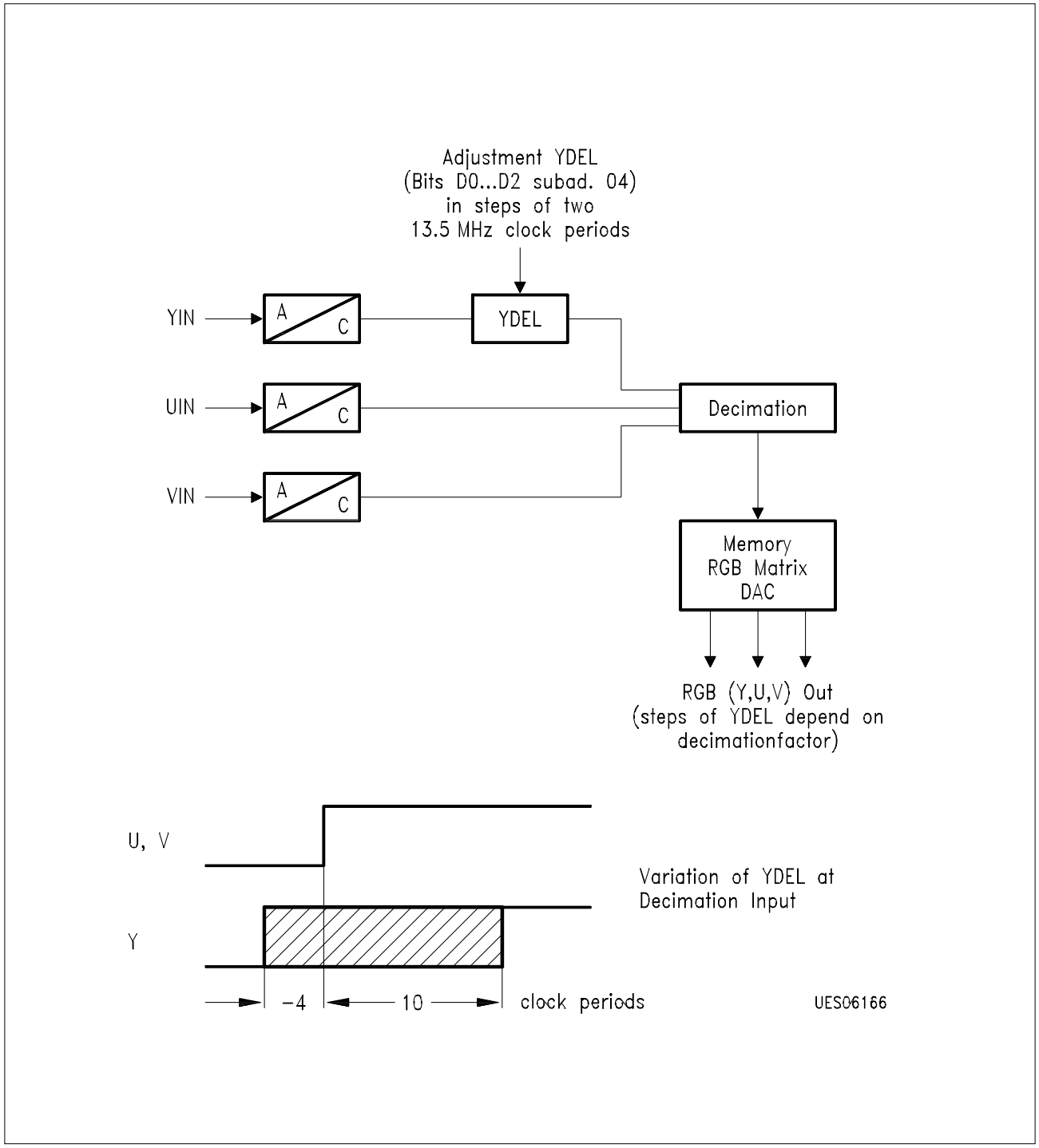


Figure 6

4.2.3 Three Level Interface (3-L)

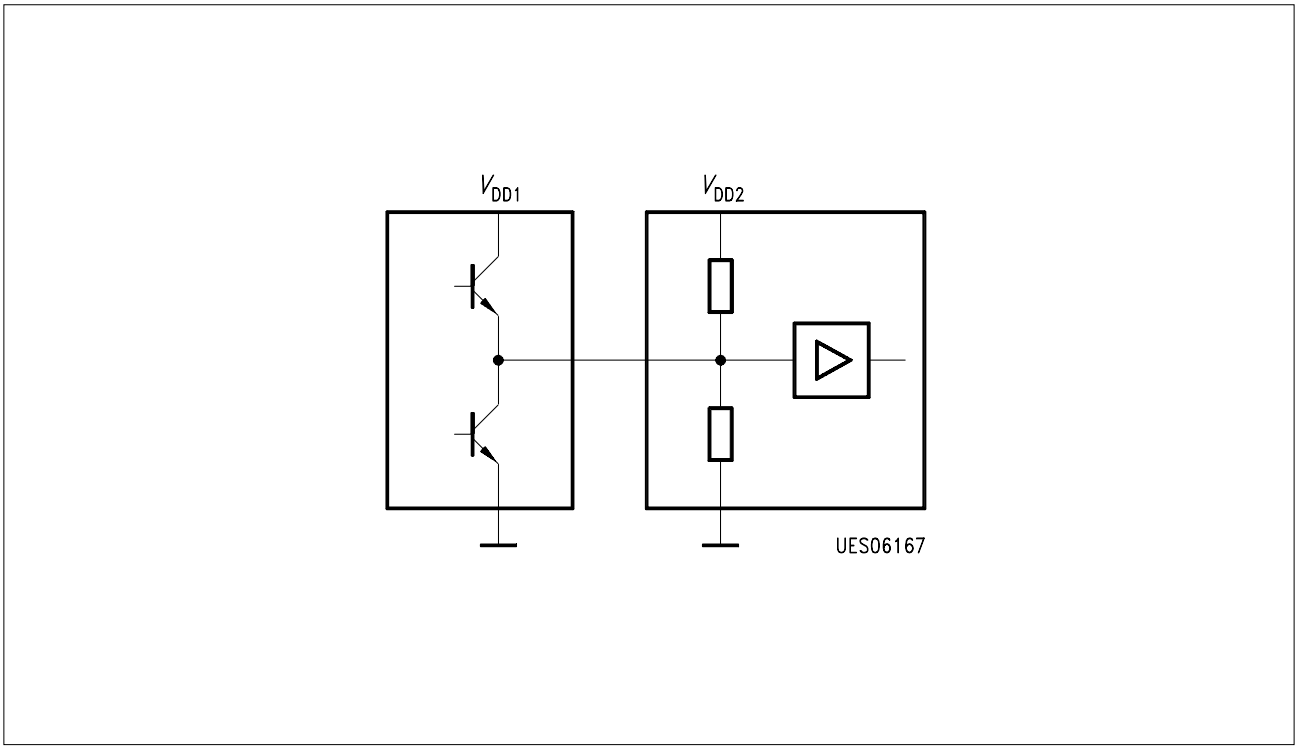


Figure 7

High level (H): upper transistor ON, lower transistor OFF

Medium level (M): both transistors OFF (interface voltage determined by input stage)

Low level (L): upper transistor OFF, lower transistor ON

4.2.4 Application Board Layout Proposal

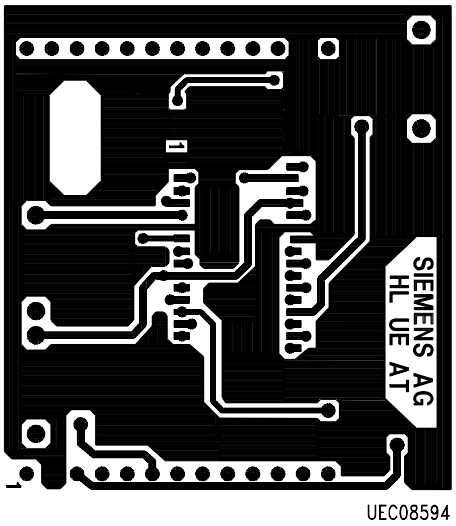


Figure 8
(top view)

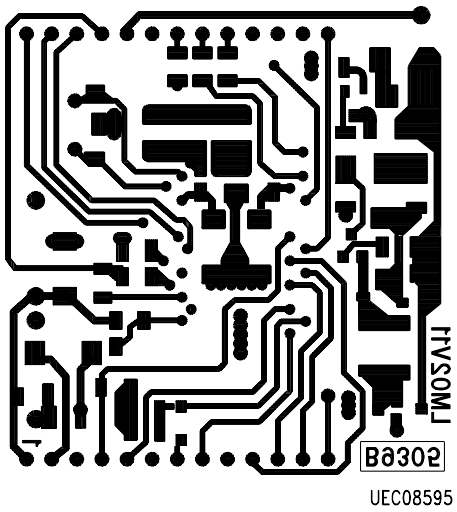


Figure 9
(bottom view)

4.2.5 Application Circuit (R, G, B-mode)

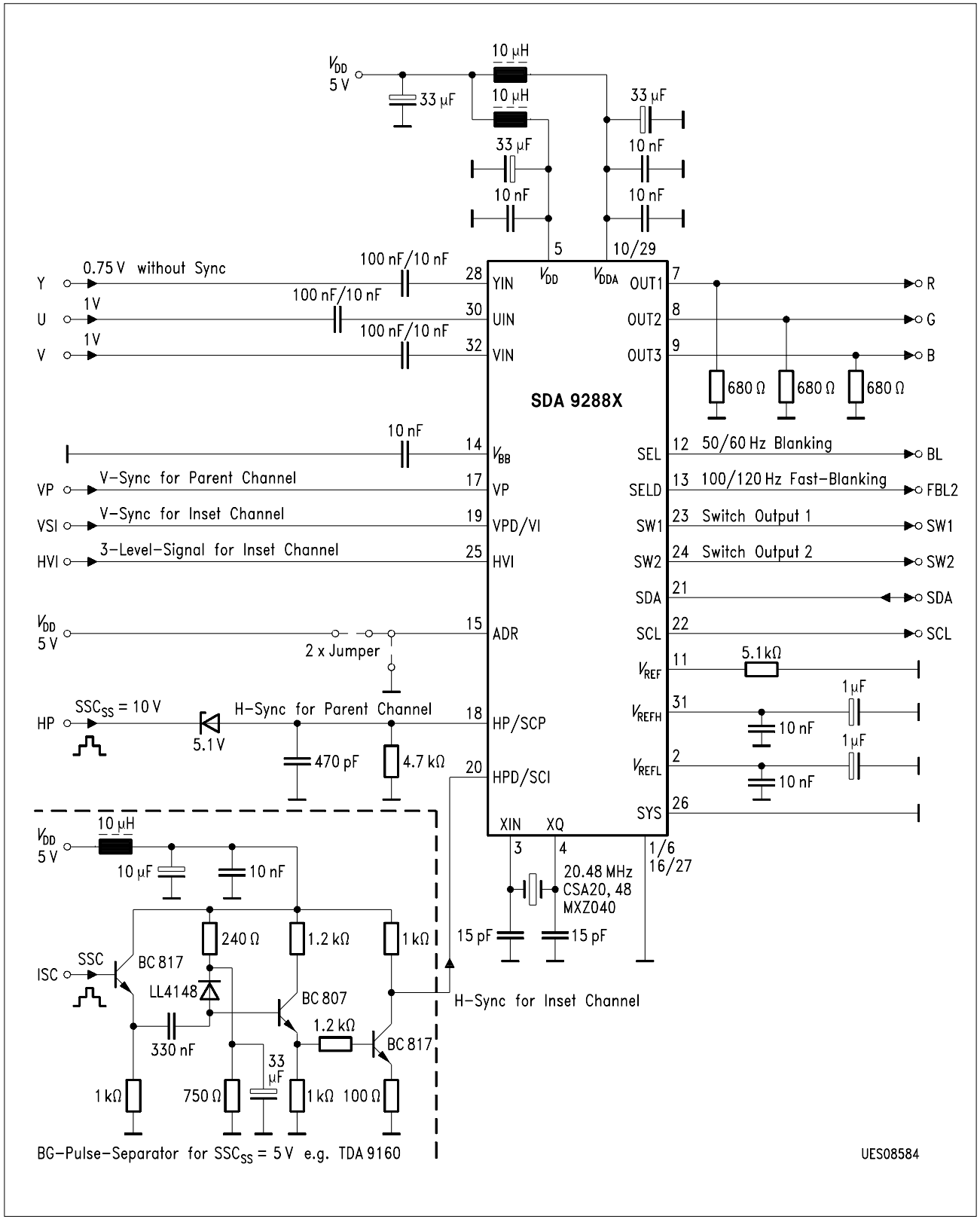


Figure 10

4.3 Waveforms

4.3.1 Timing of ADC Clamping

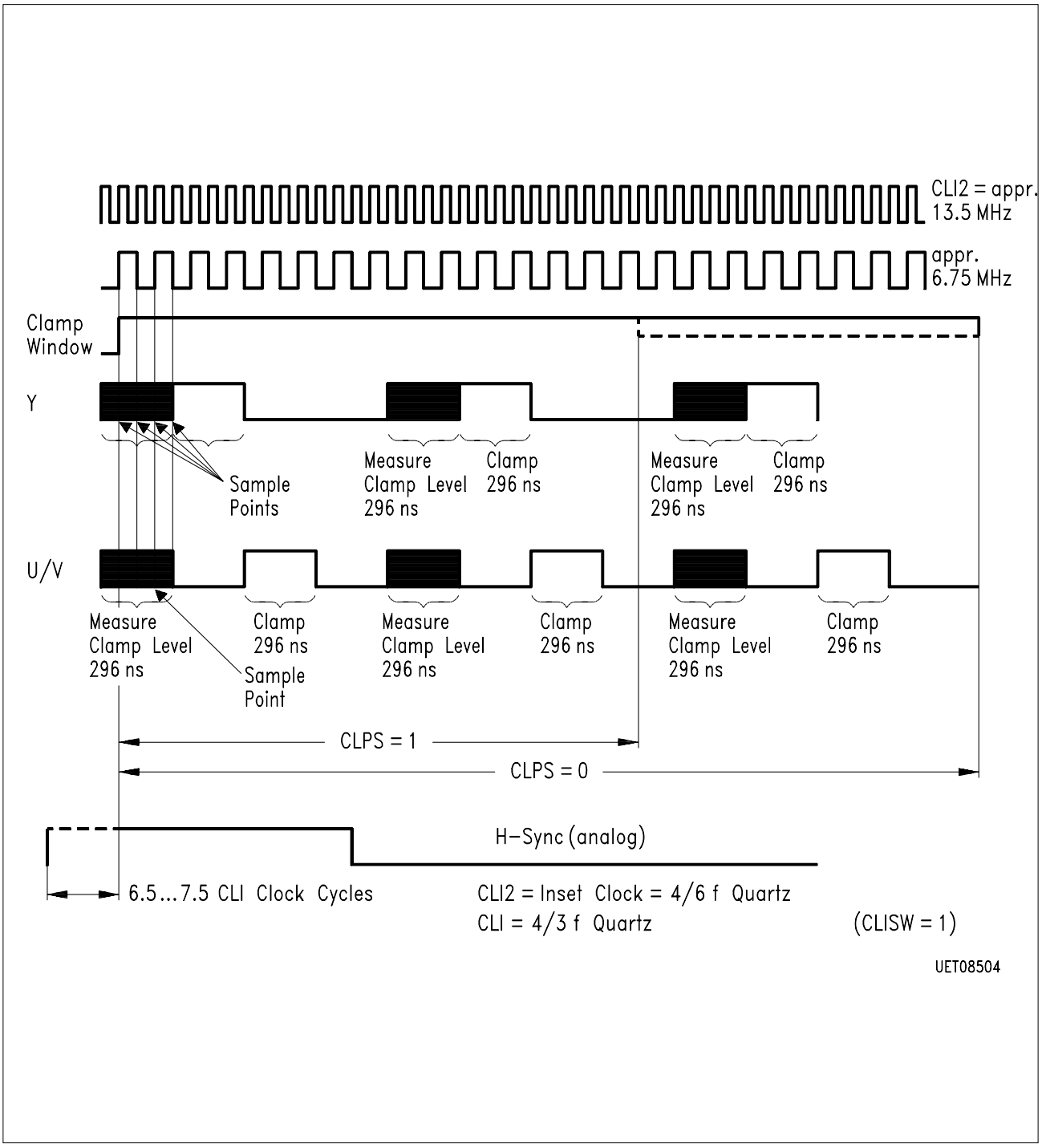


Figure 11

The values are valid if HSIDEL = '0'. To get the maximum values 444 ns for each step of HSIDEL adjustment must be added (CLPFIX = '0'). With CLPFIX = '1' there is no influence of the HSIDEL adjustment to the clamp timing.

4.3.2 Phase Relation of Sync Pulses at Frame Mode

If the phase relation is not correct at the H and V sync inputs, an adjustment via bits VSIDEL and VSPDEL is possible.

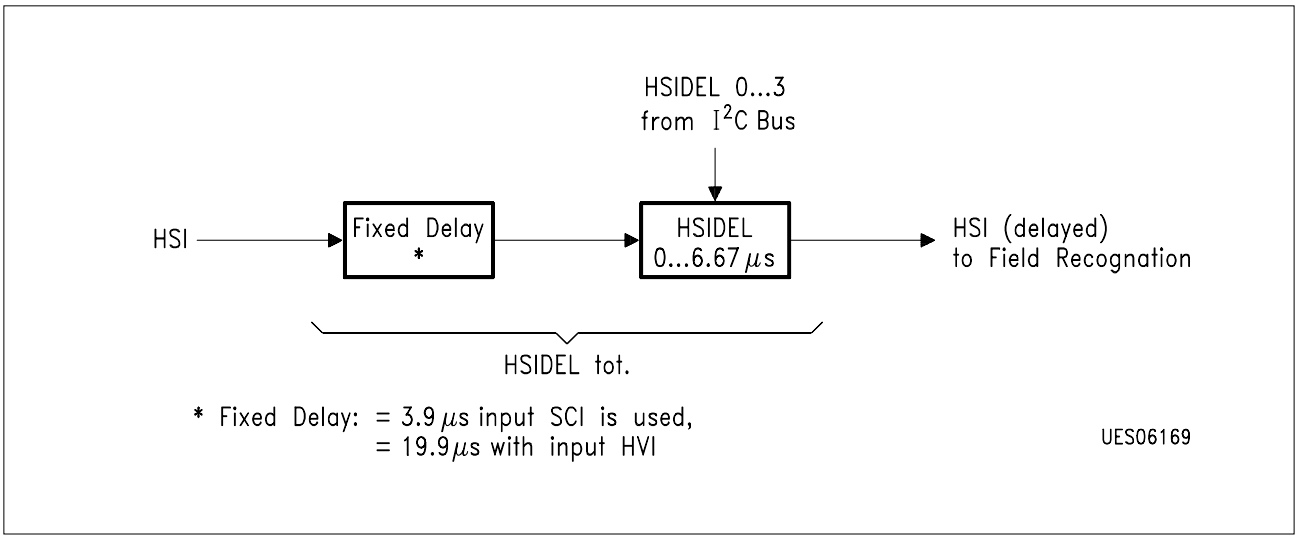


Figure 12
Signal Flow of the Horizontal Synchronization (insert part)

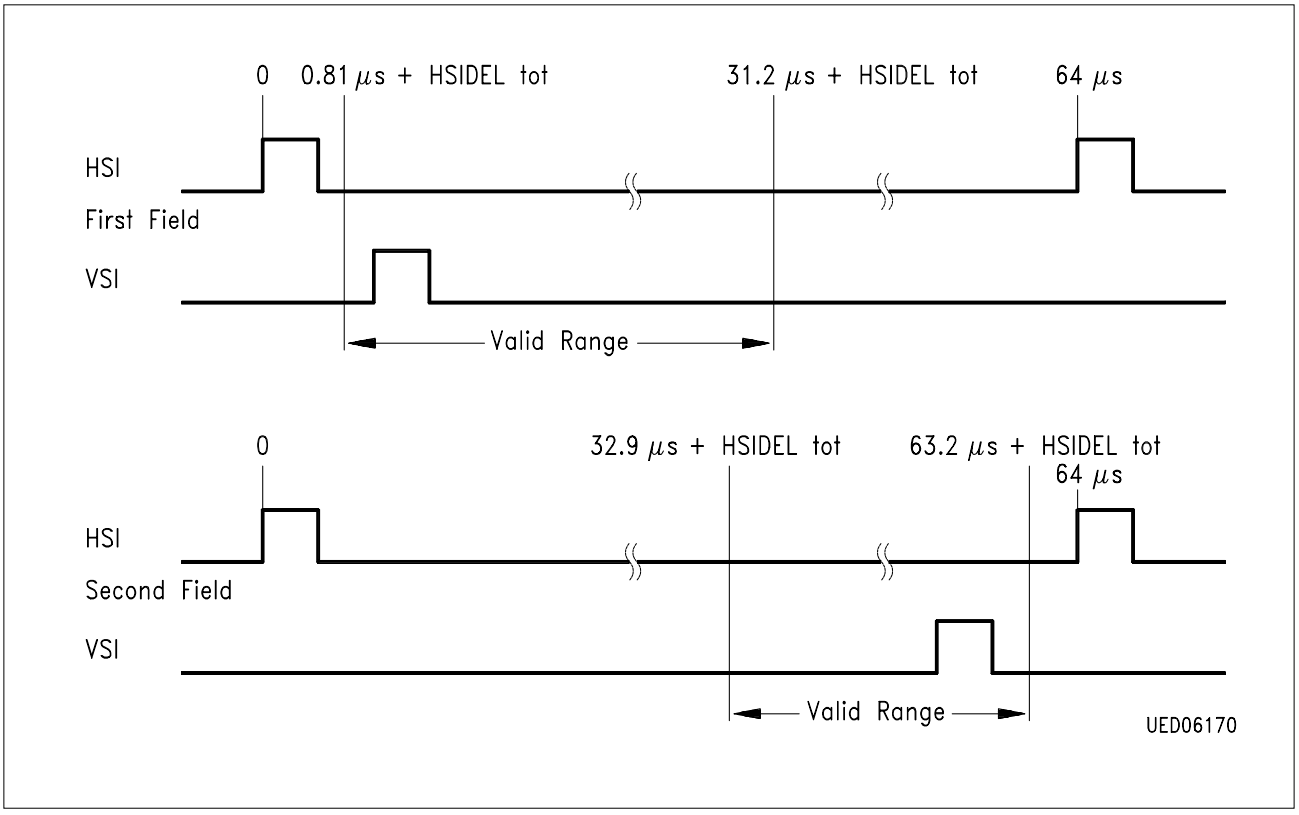


Figure 13
Allowed Phase Relation of the
Horizontal/Vertical Sync Pulses (insert channel) if VSIDEL(0:4) = '0000'

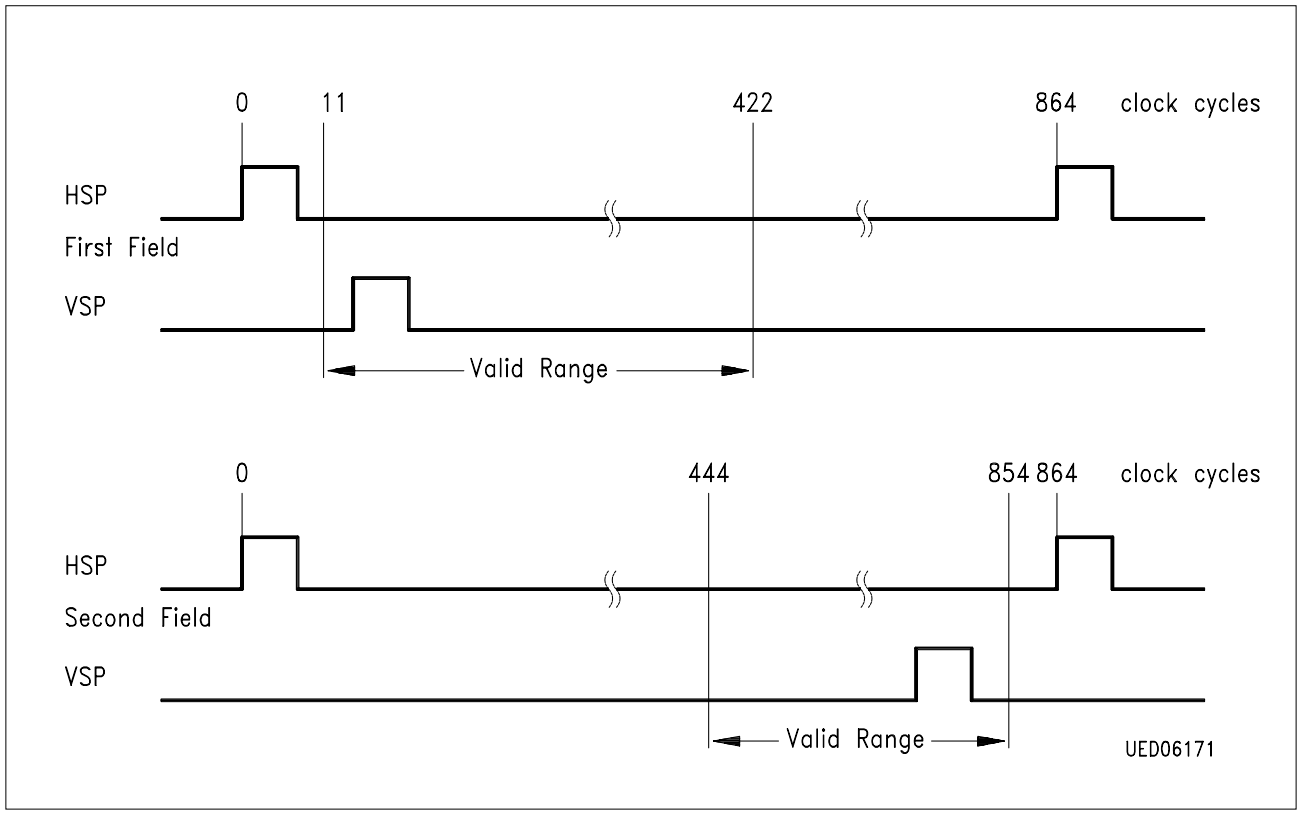
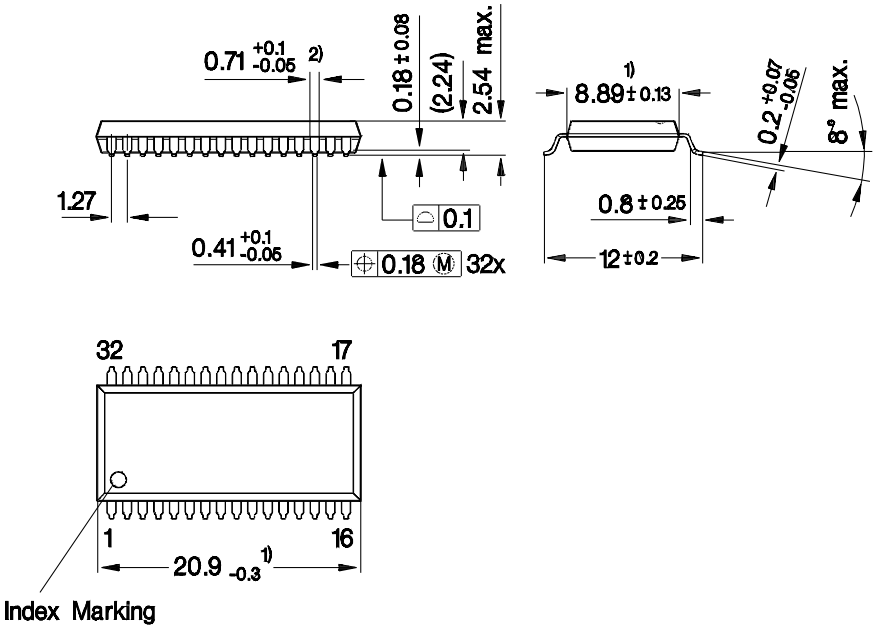


Figure 14
Allowed Phase Relation of the
Horizontal/Vertical Sync Pulses (parent channel)if VSIDEL(0:4) = ‘0000’

5 Package Outlines

P-DSO-32-2
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.1 max. per side

GPS05697

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm