

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

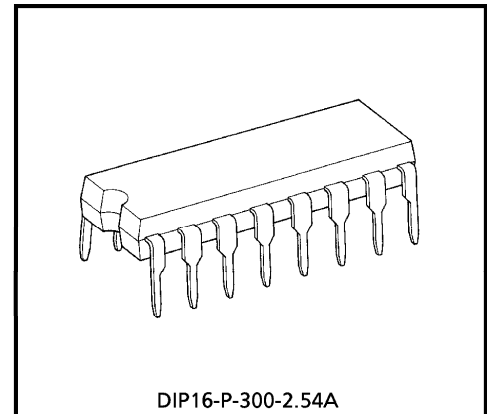
# TA8173AP

## SOUND FIELD REPRODUCTION IC

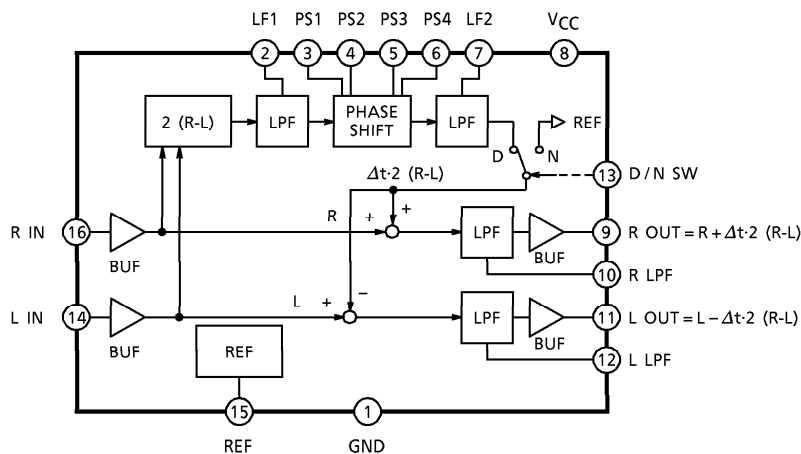
The TA8173AP is the sound field reproduction IC developed for use on such stereo equipment as radio cassette tape recorder, multivoice TV set. etc. This IC has made it possible to reproduce stereophonic sound with more presence by forcing difference signals of R-ch and L-ch to delay and applying these signals to R-ch and L-ch again.

### FEATURES

- Built-in 4 stages of the lagging phase filter
- Built-in NORMAL / DELAY switch
- Operating supply voltage range  
 $V_{CC} (opr) = 4 \sim 12V$  ( $T_a = 25^\circ C$ )



### BLOCK DIAGRAM



961001EBA2

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CAUTIONS FOR USE

1. D/N (delay / normal) switch

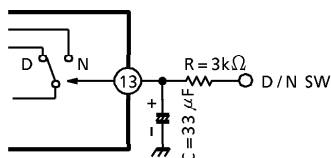
The Pin<sup>13</sup> is the delay / normal mode selector switch. The delay mode / normal mode control voltage ranges are as follows :

$V_{CC} = 5V, T_a = 25^{\circ}C$

Delay Mode	$V_{13} = 2.0V \sim V_{CC}$ or open
Normal Mode	$V_{13} = 0V \sim 0.7V$

If the output pop noise is generated when the delay / Normal mode is Switched by PIN<sup>13</sup>, the Noise level can be reduced by smoothing current with a capacitor and resistor connected to PIN<sup>13</sup> externally as shown in the test circuit diagram.

The recommended values are  $C = 33\mu F$  and  $R = 3k\Omega$ .

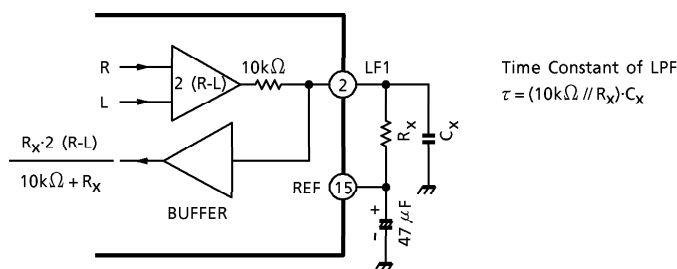


2. Delay system signal level

This IC delays phase of the difference signal (R-L) of the R (PIN<sup>16</sup> INPUT) signal and L (PIN<sup>14</sup> input) signal and adds it to the R and L signals again. This delay system signal level has been set at 2 (R-L) in the standard circuit. However, as it is possible to reduce this signal level by externally connected parts. Set an optimum value through a listening test, etc. as shown below.

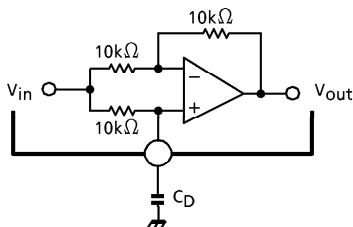
Connect a resistor from the LPF output PIN<sup>2</sup> or <sup>7</sup> to the REF PIN<sup>15</sup> as illustrated below. As a  $10k\Omega$  is seen in the LPF output PIN, it is possible to attenuate the delay system signal level by dividing resistance with the external resistor  $R_x$ .

In this case as the time constant of the LPF changes when the  $R_x$  is connected, decide the LPF's time constant by  $(10k\Omega // R_x) \cdot C_x$  again after deciding the  $R_x$ .



3. Delay system signal phase delay circuit

In the phase delay circuit of this IC, 4 stages of the block shown below are connected in series. Decide a time constant by the external  $C_D$  and total phase delay by the number of stages to be used.

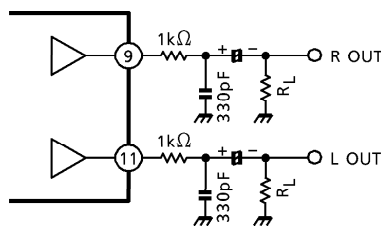


$$\frac{V_{out}}{V_{in}} = \frac{1 - j2\pi f \cdot 10k\Omega \cdot C_D}{1 + j2\pi f \cdot 10k\Omega \cdot C_D}$$

$$\phi = -2 \tan^{-1} (2\pi f \cdot 10k\Omega \cdot C)$$

4. Oscillation stability

In the test circuit diagram, the capacitor ( $C = 330pF$ ) and the resistor ( $R = 1k\Omega$ ) connected to the output PINS ⑨ and ⑪ consist of the LPF for preventing frequency parasitic oscillation. If this LPF is not inserted in the circuit, weak oscillation of several MHz may be generated and therefore, user is advised to surely connect this LPF.



MAXIMUM RATINGS ( $T_a = 25^\circ C$ )

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	$V_{CC}$	14	V
Power Dissipation	$P_D$ (Note)	750	mW
Operating Temperature	$T_{opr}$	- 25~75	$^\circ C$
Storage Temperature	$T_{stg}$	- 55~150	$^\circ C$

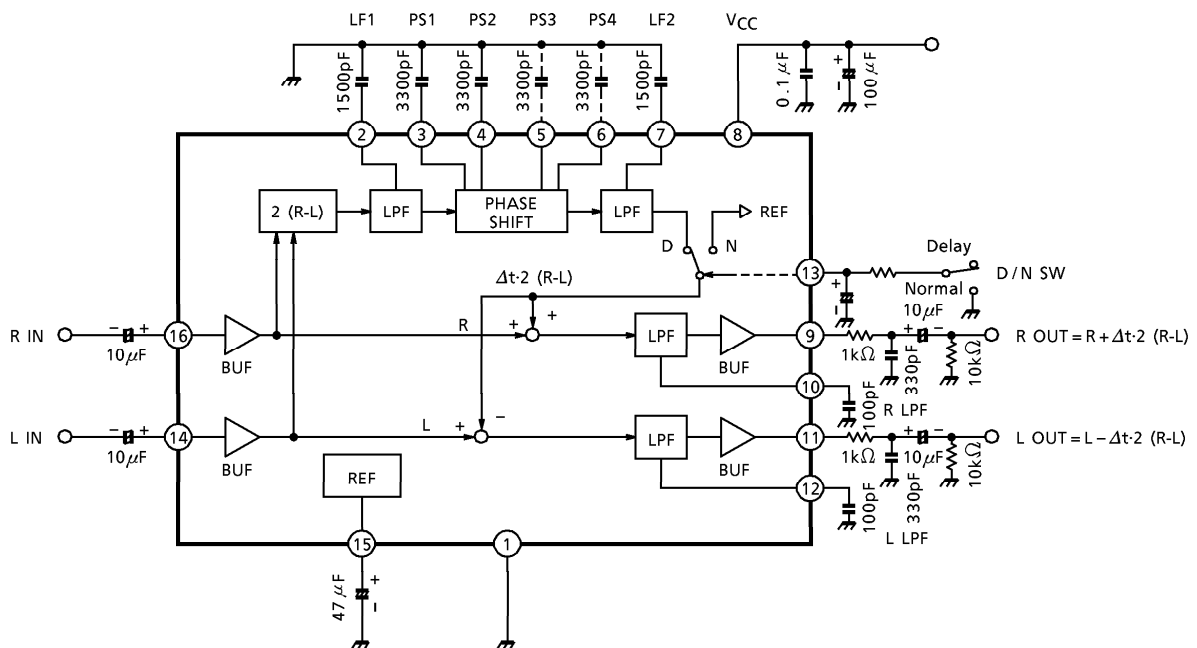
(Note) Derated above  $T_a = 25^\circ C$  in the proportion of  $6mW/^\circ C$ .

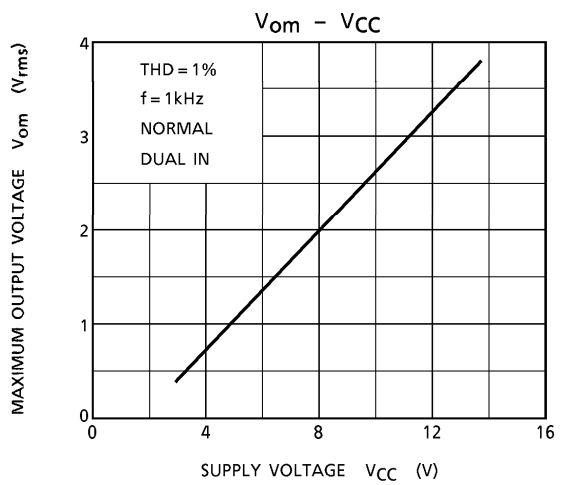
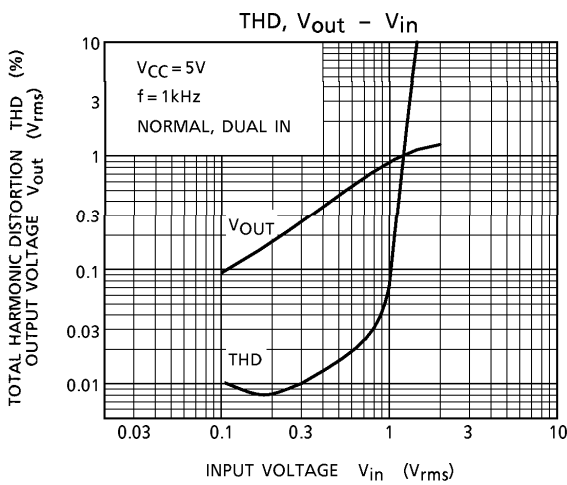
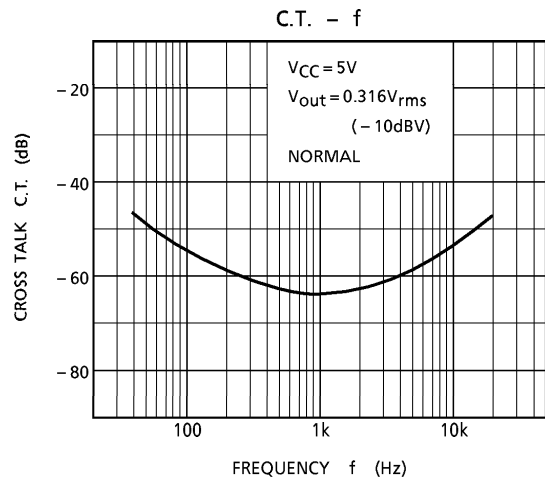
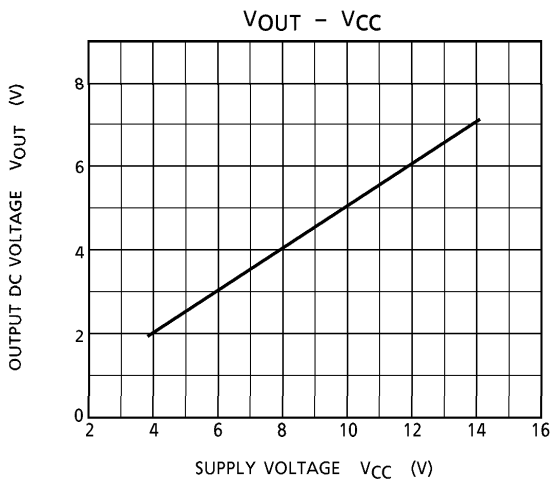
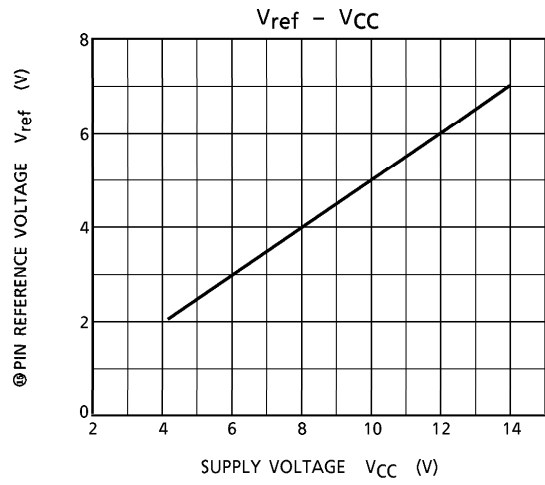
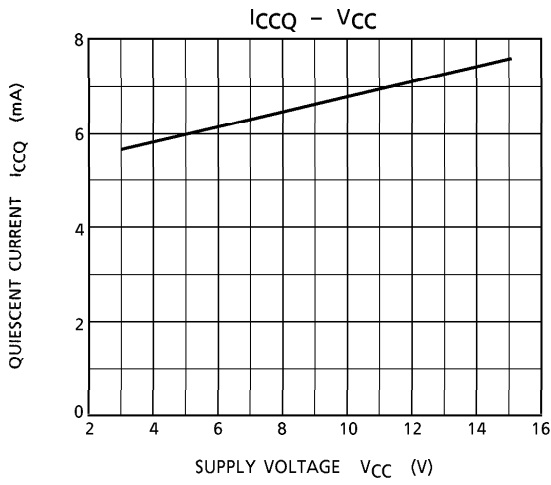
**ELECTRICAL CHARACTERISTICS**

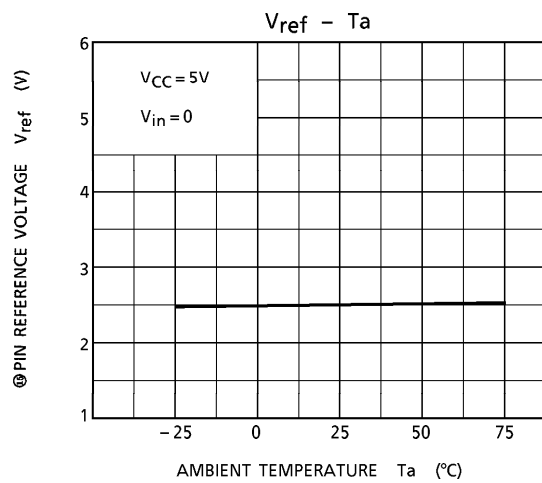
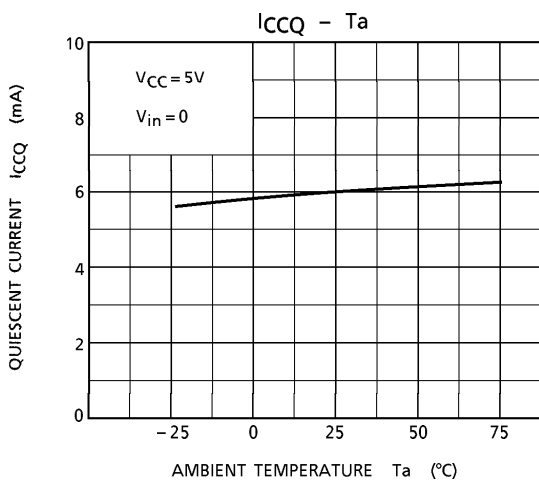
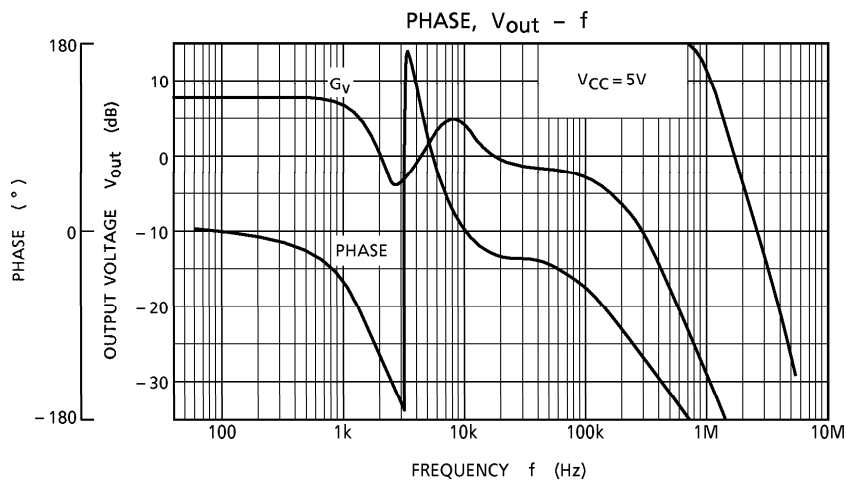
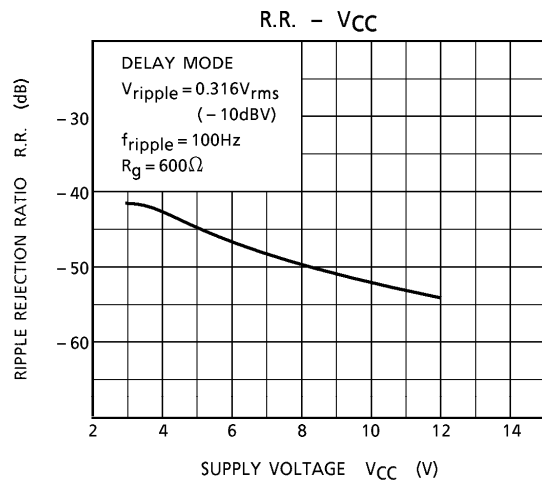
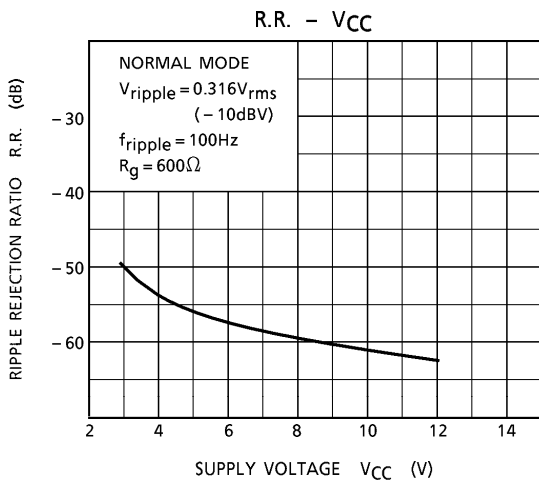
(Unless otherwise specified,  $V_{CC} = 5V$ ,  $f = 1kHz$ ,  $R_L = 10k\Omega$ ,  $T_a = 25^\circ C$ , NORMAL MODE)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current	$I_{CCQ}$	—	$V_{in} = 0$	—	6	10	mA
Voltage Gain 1	$G_{V1}$	—	—	-3	-1	1	dB
Voltage Gain Ratio	$\Delta G_V$	—	—	-1	0	1	dB
Voltage Gain 2	$G_{V2}$	—	DELAY MODE, $f = 100Hz$	6	8	10	dB
Maximum Output Voltage	$V_{om}$	—	THD = 1%	—	1.0	—	$V_{rms}$
Total Harmonic Distortion	THD	—	$V_{out} = 300mV_{rms}$	—	0.02	0.2	%
Output Noise Voltage 1	$V_{no1}$	—	NORMAL MODE, DIN AUDIO filter IN	—	10	40	$\mu V_{rms}$
Output Noise Voltage 2	$V_{no2}$	—	DELAY MODE, DIN AUDIO filter IN	—	17	—	$\mu V_{rms}$
Channel Separation Ratio	Sep.	—	$V_{out} = 1V_{rms}$	—	-55	—	dB
Ripple Rejection 1	R.R.1	—	NORMAL MODE, $f = 100Hz$ , $V_{ripple} = 0.316V_{rms} (-10dBV)$	—	-55	—	dB
Ripple Rejection 2	R.R.2	—	DELAY MODE, $f = 100Hz$ , $V_{ripple} = 0.316V_{rms} (-10dBV)$	—	-45	—	dB
Input Resistance	$R_{IN}$	—	—	—	33	—	$k\Omega$

**TEST CIRCUIT**

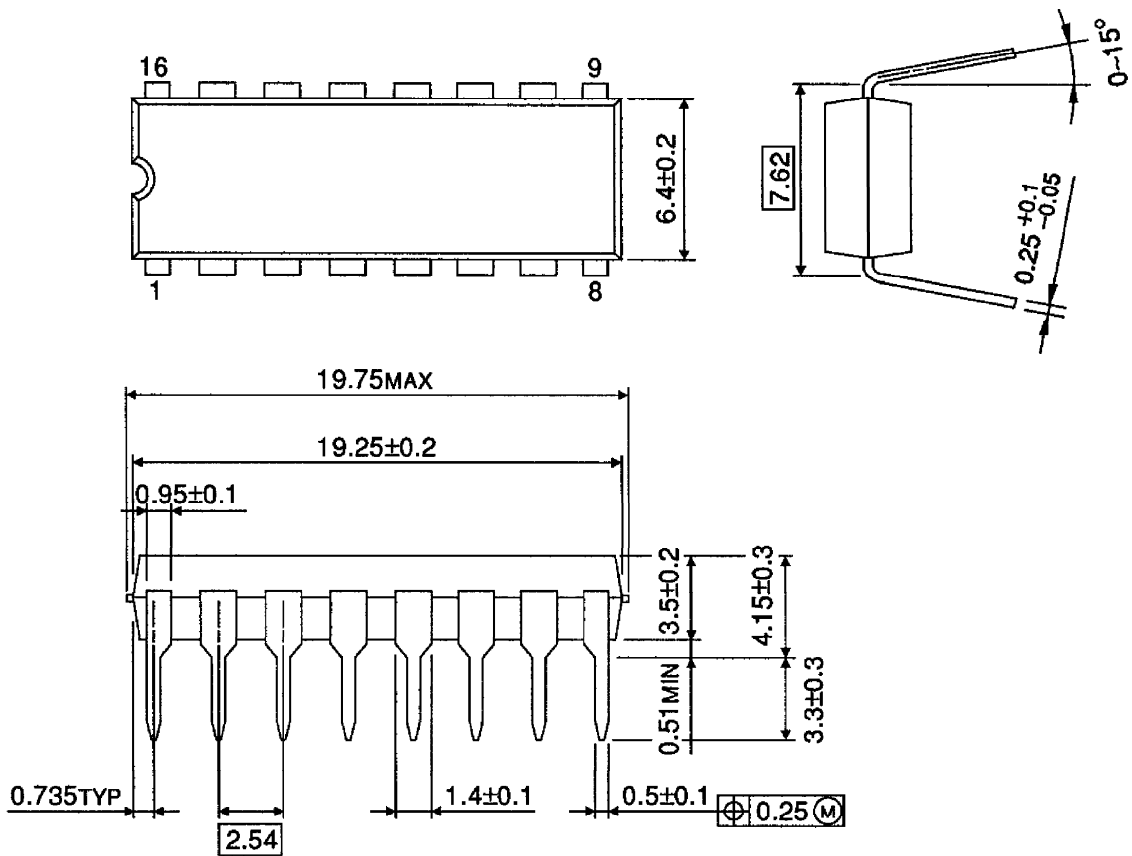






**OUTLINE DRAWING**  
DIP16-P-300-2.54A

Unit : mm



Weight : 1.00g (Typ.)