

## Linear Building Block – Single Comparator in SOT Package

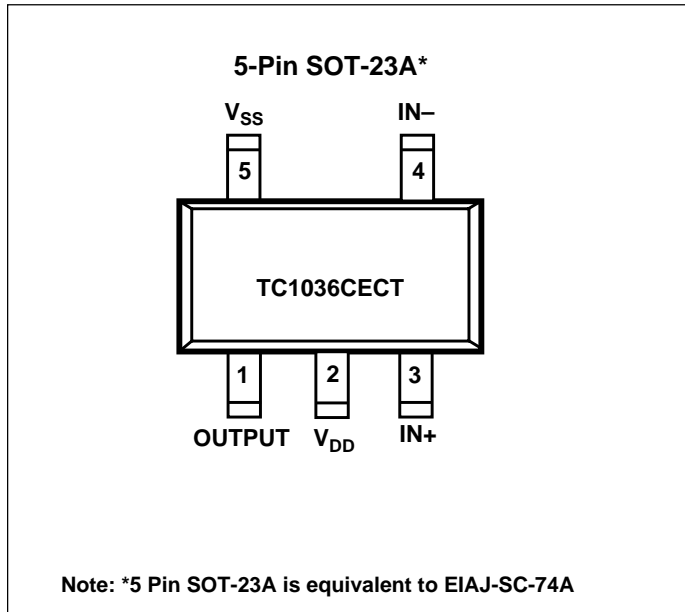
### FEATURES

- Space Saving SOT-23A Package
- Optimized for Single-Supply Operation
- Ultra Low Input Bias Current ..... Less than 100pA
- Low Quiescent Current ..... 4  $\mu$ A
- Rail-to-Rail Inputs and Outputs
- Operation Down to  $V_{DD} = 1.8V$
- LMC7211 Pin Replaceable

### APPLICATIONS

- Power Management Circuits
- Battery Operated Equipment
- Consumer Products

### PIN CONFIGURATION



### GENERAL DESCRIPTION

The TC1036 is a single low-power comparator designed for low-power applications.

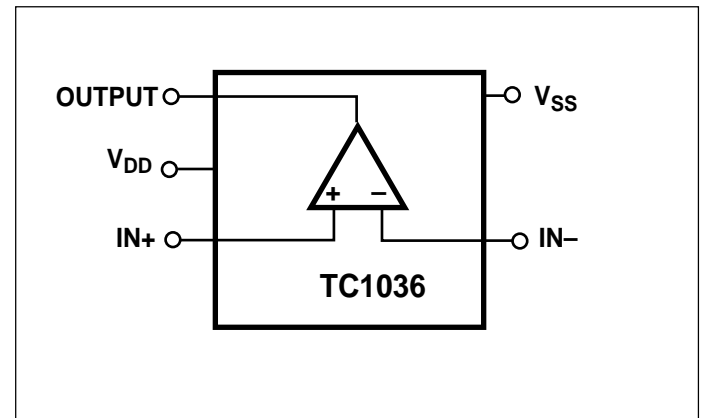
This comparator is specifically designed for operation from a single supply. However, operation from dual supplies also is possible, and power supply current is independent of the magnitude of the power supply voltage. The TC1036 can operate from two 1.5V alkaline cells down to  $V_{DD} = 1.8V$ . Active supply current is 4 $\mu$ A for the TC1036. Input and output swing of these devices is rail-to-rail.

Packaged in a 5-Pin SOT-23A, the TC1036 comparator is ideal for applications requiring high integration, small size, and low power.

### ORDERING INFORMATION

Part No.	Package	Temp. Range
TC1036CECT	5-Pin SOT-23A	- 40°C to +85°C

### FUNCTIONAL BLOCK DIAGRAM



# Linear Building Block – Single Comparator in SOT Package

## TC1036

### ABSOLUTE MAXIMUM RATINGS\*

Supply Voltage .....	6.0V
Voltage on Any Pin: (With Respect to Supplies) ..... (V <sub>SS</sub> – 0.3V) to (V <sub>DD</sub> +0.3V)	
Operating Temperature Range: .....	– 40°C to + 85°C
Storage Temperature Range .....	– 55°C to +150°C
Lead Temperature (Soldering, 10 sec) .....	+260°C

\* Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

**ELECTRICAL CHARACTERISTICS:** Typical values apply at 25°C and V<sub>DD</sub> = 3.0V. Minimum and maximum values apply for V<sub>DD</sub> = 1.8V to 5.5V, and T<sub>A</sub> = -40°C to +85°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>DD</sub>	Supply Voltage		1.8	—	5.5	V
I <sub>Q</sub>	Supply Current, Operating	All Outputs Unloaded	—	4	8	μA
V <sub>ICMR</sub>	Common Mode Input Voltage Range		V <sub>SS</sub> – 0.2	—	V <sub>DD</sub> +0.2	V
V <sub>OS</sub>	Input Offset Voltage	V <sub>DD</sub> = 3V, V <sub>CM</sub> = 1.5V, T <sub>A</sub> = 25°C T <sub>A</sub> = –40°C to 85°C	–5 –5	—	+5 +5	mV mV
I <sub>B</sub>	Input Bias Current	T <sub>A</sub> = 25°C, IN+, IN– = V <sub>DD</sub> to V <sub>SS</sub>	—	—	±100	pA
V <sub>OH</sub>	Output High Voltage	R <sub>L</sub> = 10KΩ to V <sub>SS</sub>	V <sub>DD</sub> – 0.3	—	—	V
V <sub>OL</sub>	Output Low Voltage	R <sub>L</sub> = 10KΩ to V <sub>DD</sub>	—	—	0.3	V
CMRR	Common Mode Rejection Ratio	T <sub>A</sub> = 25°C, V <sub>DD</sub> = 5V V <sub>CM</sub> = V <sub>DD</sub> to V <sub>SS</sub>	66	—	—	dB
PSRR	Power Supply Rejection Ratio	T <sub>A</sub> = 25°C, V <sub>CM</sub> = 1.2V V <sub>DD</sub> = 1.8V to 5V	60	—	—	dB
I <sub>SRC</sub>	Output Source Current	IN+ = V <sub>DD</sub> , IN– = V <sub>SS</sub> Output Shorted to V <sub>SS</sub> V <sub>DD</sub> = 1.8V	1	—	—	mA
I <sub>SINK</sub>	Output Sink Current	IN+ = V <sub>SS</sub> , IN– = V <sub>DD</sub> , Output Shorted to V <sub>DD</sub> V <sub>DD</sub> = 1.8V	2	—	—	mA
t <sub>PD1</sub>	Response Time	100mV Overdrive, C <sub>L</sub> = 100pF	—	4	—	μsec
t <sub>PD2</sub>	Response Time	10mV Overdrive, C <sub>L</sub> = 100pF	—	6	—	μsec

### PIN DESCRIPTION

Pin No.	Name	Description
1	OUTPUT	Comparator Output Terminal.
2	V <sub>DD</sub>	Positive Supply Voltage.
3	IN+	Comparator Non-Inverting Input Terminal.
4	IN–	Comparator Inverting Input Terminal.
5	V <sub>SS</sub>	Ground Terminal.

### DETAILED DESCRIPTION

The TC1036 is a very low-power, linear building block comparator targeted at low-voltage, single-supply applications. The TC1036 minimum operating voltage is 1.8V, and typical supply current is only 4  $\mu$ A.

The comparator's input range extends beyond both supply voltages by 200mV and the outputs will swing to within several millivolts of the supplies depending on the load current being driven.

The comparator exhibits a propagation delay and supply current which is largely independent of supply voltage. The low input bias current and offset voltage makes it suitable for high impedance precision applications.

### TYPICAL APPLICATIONS

The TC1036 lends itself to a wide variety of applications, particularly in battery-powered systems. It typically finds application in power management, processor supervisory, and interface circuitry.

### External Hysteresis

Hysteresis can be set externally with two resistors using positive feedback techniques (see Figure 1). The design procedure for setting external comparator hysteresis is as follows:

1. Choose the feedback resistor  $R_C$ . Since the input bias current of the comparator is at most 100 pA, the current through  $R_C$  can be set to 100 nA (i.e. 1000 times the input bias current) and retain excellent accuracy. The current through  $R_C$  at the comparator's trip point is  $V_R / R_C$  where  $V_R$  is a stable reference voltage.

2. Determine the hysteresis voltage ( $V_{HY}$ ) between the upper and lower thresholds.

3. Calculate  $R_A$  as follows.

$$R_A = R_C \left( \frac{V_{HY}}{V_{DD}} \right)$$

4. Choose the rising threshold voltage for  $V_{SRC}$  ( $V_{THR}$ ).

5. Calculate  $R_B$  as follows:

$$R_B = \frac{1}{\left[ \left( \frac{V_{THR}}{V_R * R_A} \right) - \frac{1}{R_A} - \frac{1}{R_C} \right]}$$

6. Verify the threshold voltages with these formulas:

$V_{SRC}$  rising:

$$V_{THR} = (V_R) (R_A) \left[ \left( \frac{1}{R_A} \right) + \left( \frac{1}{R_B} \right) + \left( \frac{1}{R_C} \right) \right]$$

$V_{SRC}$  falling:

$$V_{THF} = V_{THR} - \left[ \frac{(R_A * V_{DD})}{R_C} \right]$$

### Precision Battery Monitor

Figure 2 is a precision battery low/battery dead monitoring circuit. Typically, the battery low output warns the user that a battery dead condition is imminent. Battery dead typically initiates a forced shutdown to prevent operation at low internal supply voltages (which can cause unstable system operation).

The circuit of Figure 2 uses a TC1034, a TC1037 and a TC1039, and only six external resistors. AMP 1 is a simple buffer while CMPTR1 and CMPTR2 provide precision voltage detection using  $V_R$  as a reference. Resistors R2 and R4 set the detection threshold for  $\overline{BATT\ LOW}$  while resistors R1 and R3 set the detection threshold for  $\overline{BATT\ FAIL}$ . The component values shown assert  $\overline{BATT\ LOW}$  at 2.2V (typical) and  $\overline{BATT\ FAIL}$  at 2.0V (typical). Total current consumed by this circuit is typically 16 $\mu$ A at 3V. Resistors R5 and R6 provide hysteresis for comparators CMPTR1 and CMPTR2, respectively.

### 32.768 KHz 'Time Of Day Clock' Crystal Controlled Oscillator

A very stable oscillator driver can be designed by using a crystal resonator as the feedback element. Figure 3 shows a typical application circuit using this technique to develop a clock driver for a Time Of Day (TOD) clock chip. The value of  $R_A$  and  $R_B$  determine the DC voltage level at which the comparator trips — in this case one-half of  $V_{DD}$ . The RC time constant of  $R_C$  and  $C_A$  should be set several times greater than the crystal oscillator's period, which will ensure a 50% duty cycle by maintaining a DC voltage at the inverting comparator input equal to the absolute average of the output signal.

## TC1036

### Non-Retriggerable One Shot Multivibrator

Using two comparators, a non-retriggerable one shot multivibrator can be designed using the circuit configuration of Figure 4. A key feature of this design is that the pulse width is independent of the magnitude of the supply voltage because the charging voltage and the intercept voltage are a fixed percentage of  $V_{DD}$ . In addition, this one shot is capable of pulse width with as much as a 99% duty cycle and exhibits input lockout to ensure that the circuit will not re-trigger before the output pulse has completely timed out. The trigger level is the voltage required at the input to raise the voltage at node A higher than the voltage at node B, and is set by the resistive divider R4 and R10 and the impedance network composed of R1, R2, and R3. When the one shot has been triggered, the output of CMPTR2 is high, causing the reference voltage at the non-inverting input of CMPTR1 to go to  $V_{DD}$ . This prevents any additional input pulses from disturbing the circuit until the output pulse has timed out.

The value of the timing capacitor C1 must be small enough to allow CMPTR1 to discharge C1 to a diode voltage before the feedback signal from CMPTR2 (through R10) switches CMPTR1 to its high state and allows C1 to start an exponential charge through R5. Proper circuit action depends upon rapidly discharging C1 through the voltage set by R6, R9, and D2 to a final voltage of a small diode drop. Two propagation delays after the voltage on C1 drops below the level on the non-inverting input of CMPTR2, the output of CMPTR1 switches to the positive rail and begins to charge C1 through R5. The time delay which sets the output pulse width results from C1 charging to the reference voltage set by R6, R9, and D2, plus four comparator propagation delays. When the voltage across C1 charges beyond the reference, the output pulse returns to ground and the input is again ready to accept a trigger signal.

### Oscillators and Pulse Width Modulators

TelCom's linear building block comparators adapt well to oscillator applications for low frequencies (less than 100 KHz). Figure 5 shows a symmetrical square wave generator using a minimum number of components. The output is set by the RC time constant of R4 and C1, and the total hysteresis of the loop is set by R1, R2, and R3. The maximum frequency of the oscillator is limited only by the large signal propagation delay of the comparator in addition to any capacitive loading at the output which degrades the slew rate.

To analyze this circuit, assume that the output is initially high. For this to occur, the voltage at the inverting input must be less than the voltage at the non-inverting input. Therefore, capacitor C1 is discharged. The voltage at the non-inverting input ( $V_H$ ) is:

$$V_H = \frac{R2(V_{DD})}{[R2 + (R1 || R3)]}$$

where, if  $R1 = R2 = R3$ , then:

$$V_H = \frac{2(V_{DD})}{3}$$

Capacitor C1 will charge up through R4. When the voltage of the comparator's inverting input is equal to  $V_H$ , the comparator output will switch. With the output at ground potential, the value at the non-inverting input terminal ( $V_L$ ) is reduced by the hysteresis network to a value given by:

$$V_L = \frac{V_{DD}}{3}$$

Using the same resistors as before, capacitor C1 must now discharge through R4 toward ground. The output will return to a high state when the voltage across the capacitor has discharged to a value equal to  $V_L$ . The period of oscillation will be twice the time it takes for the RC circuit to charge up to one half its final value. The period can be calculated from:

$$\frac{1}{\text{FREQ}} = 2 (0.694) (R4) (C1)$$

Equation 8.

The frequency stability of this circuit should only be a function of the external component tolerances.

Figure 6 shows the circuit for a pulse width modulator circuit. It is essentially the same as in Figure 5 with the addition of an input control voltage. When the input control voltage is equal to one-half  $V_{DD}$ , operation is basically the same as described for the free-running oscillator. If the input control voltage is moved above or below one-half  $V_{DD}$ , the duty cycle of the output square wave will be altered. This is because the addition of the control voltage at the input has now altered the trip points. The equations for these trip points are shown in Figure 6 (see  $V_H$  and  $V_L$ ).

Pulse width sensitivity to the input voltage variations can be increased by reducing the value of R6 from 10 K $\Omega$  and conversely, sensitivity will be reduced by increasing the value of R6. The values of R1 and C1 can be varied to produce the desired center frequency.

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TC1036

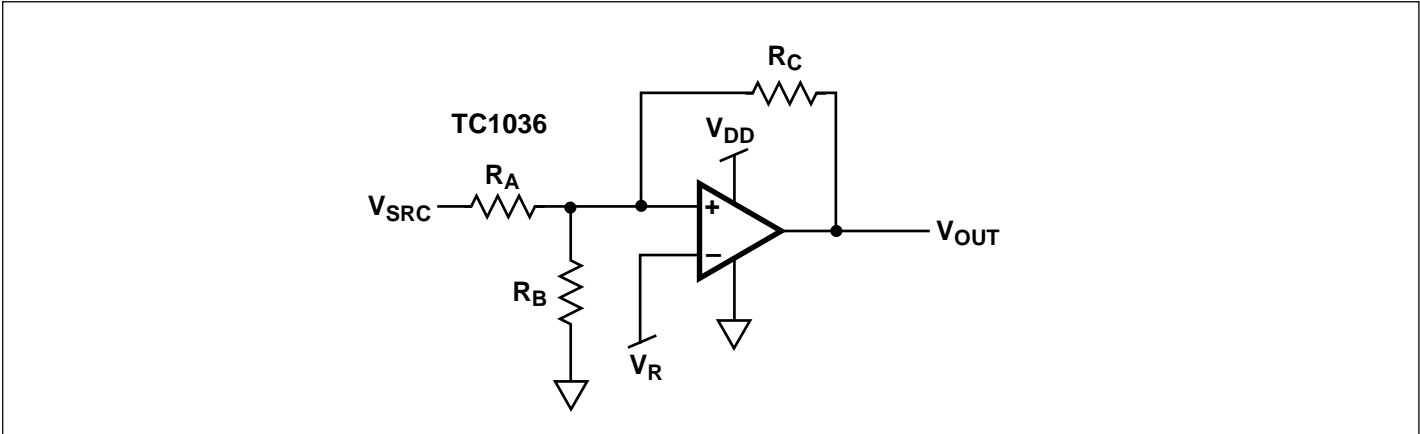


Figure 1. Comparator External Hysteresis Configuration

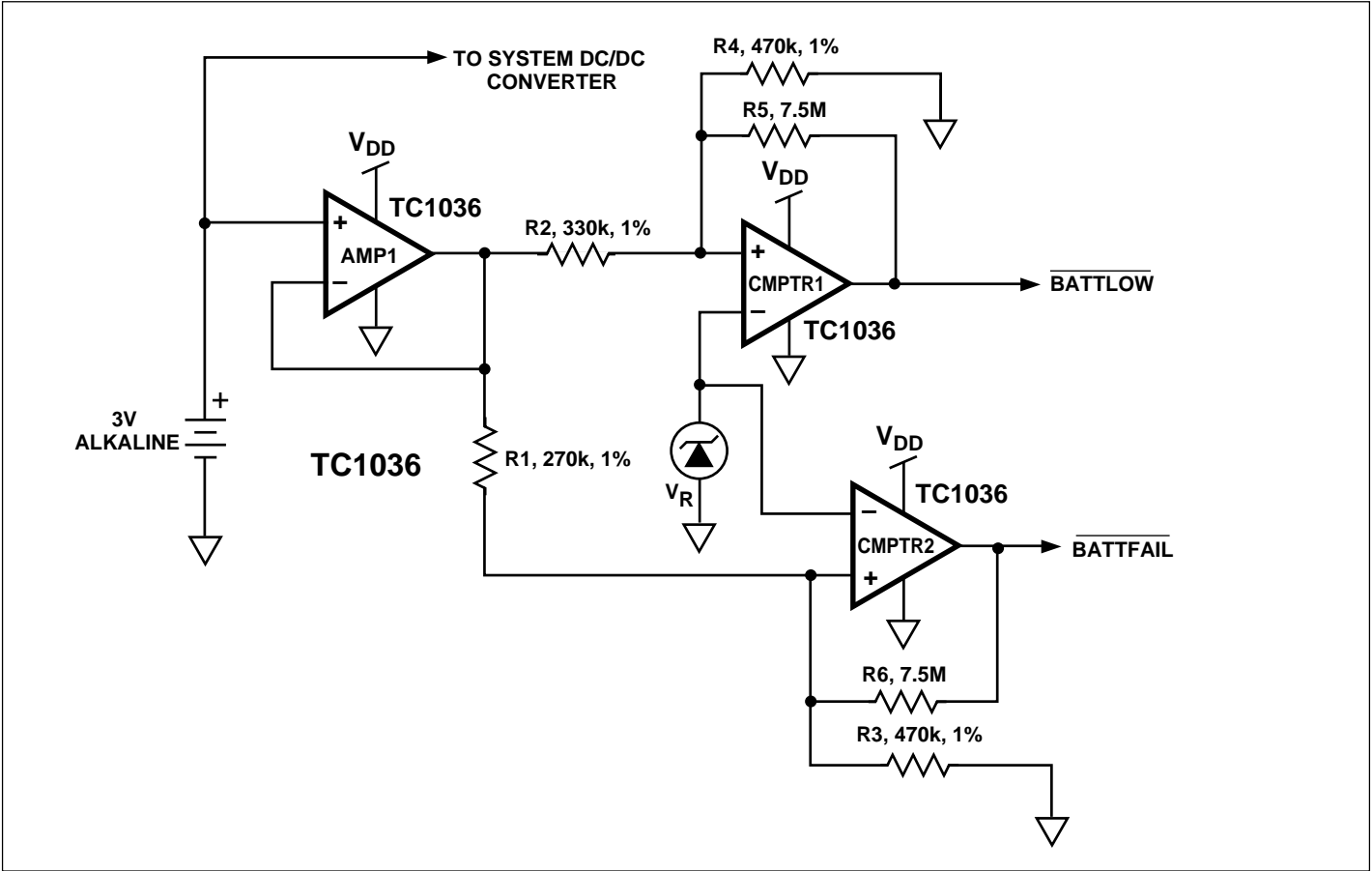


Figure 2. Precision Battery Monitor

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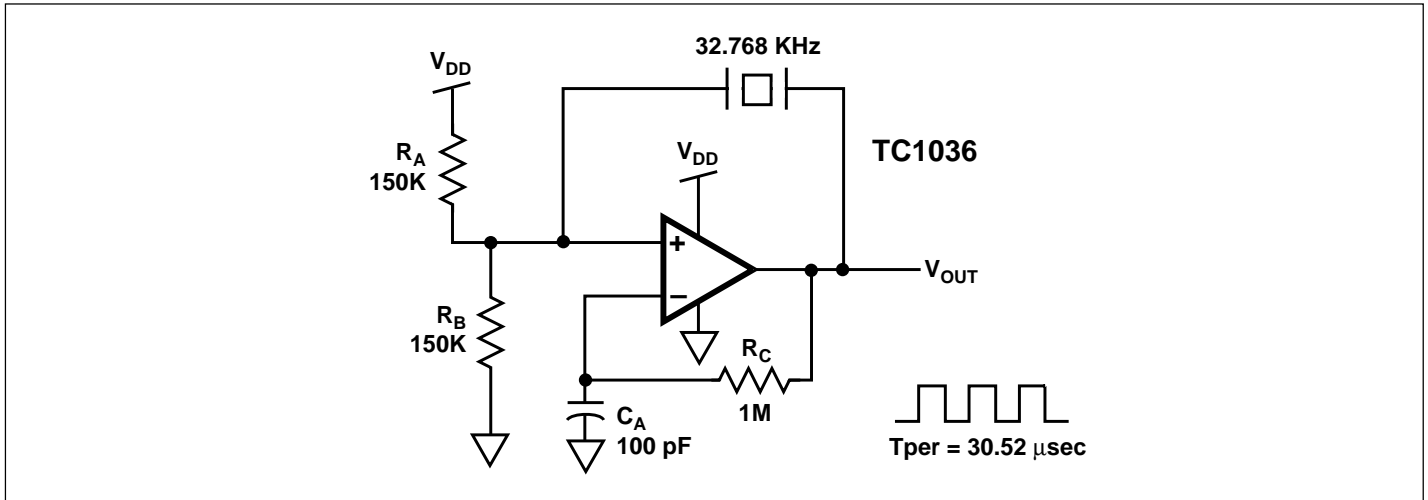


Figure 3. 32.768 KHz "Time of Day" Clock Oscillator

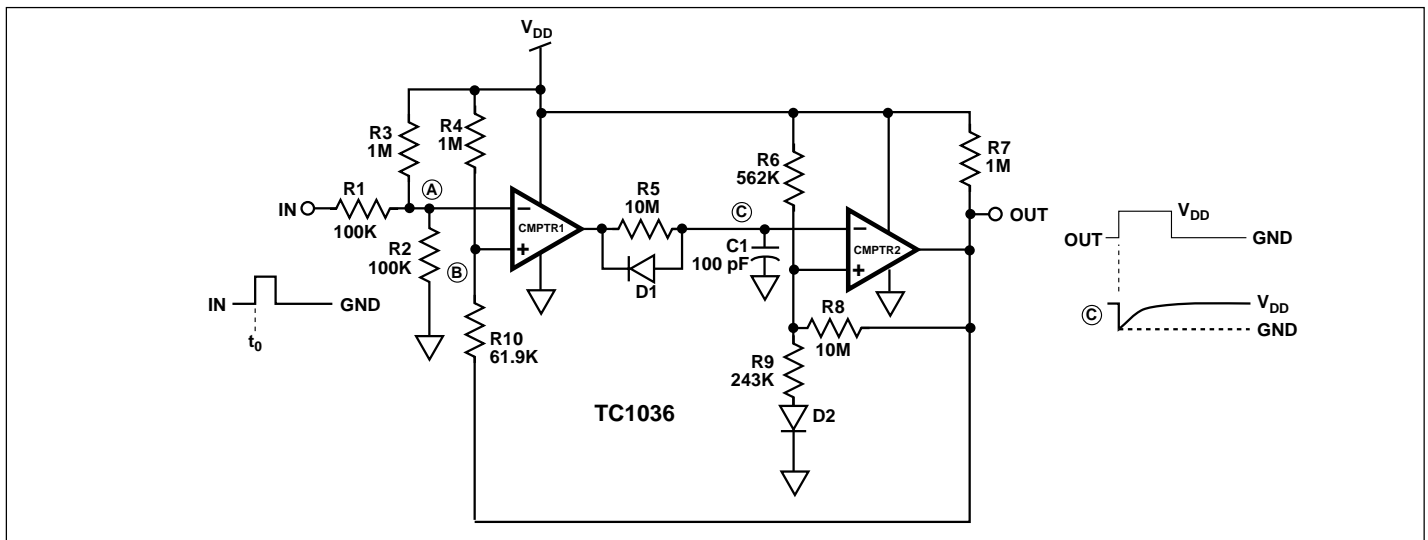


Figure 4. Non-Retriggerable Multivibrator

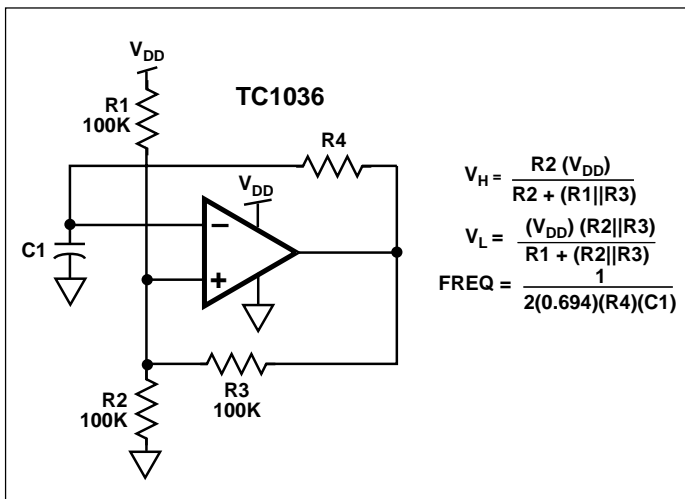


Figure 5. Square Wave Generator

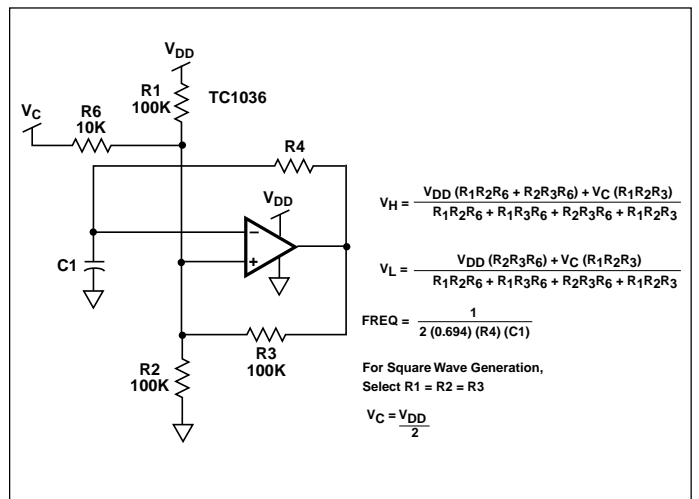
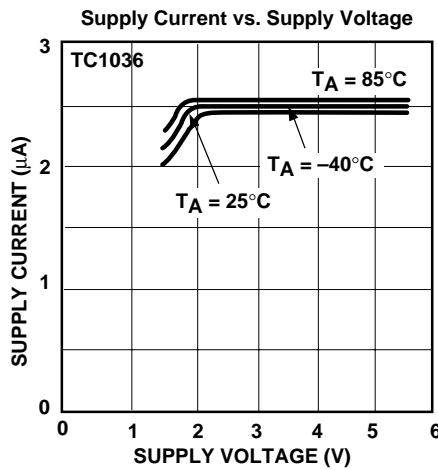
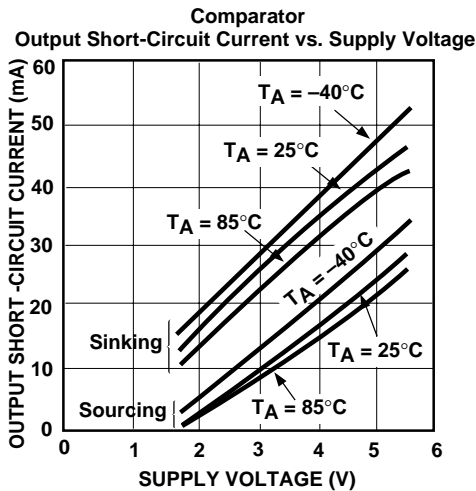
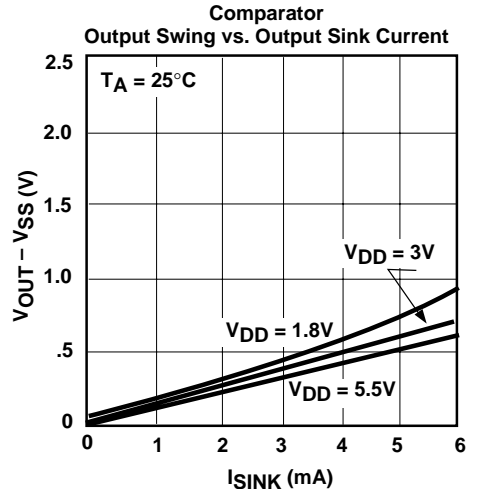
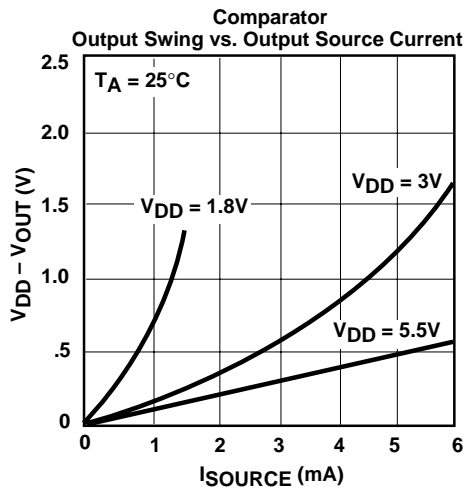
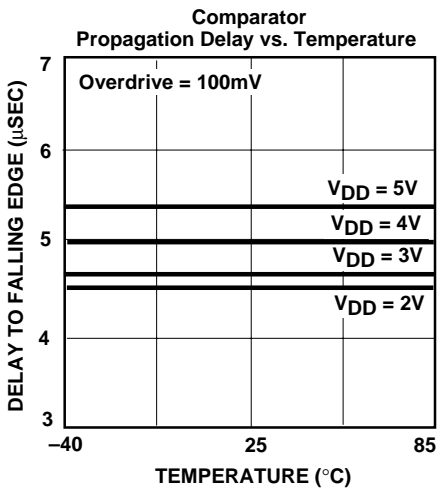
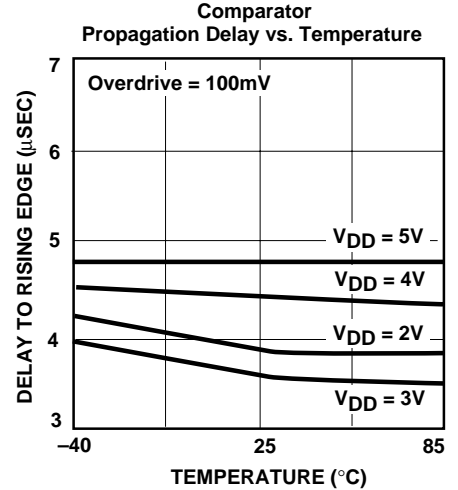
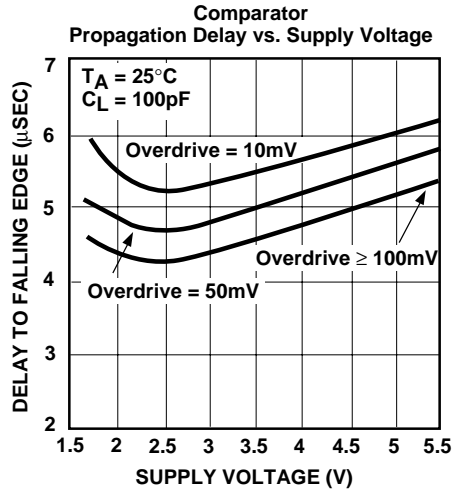
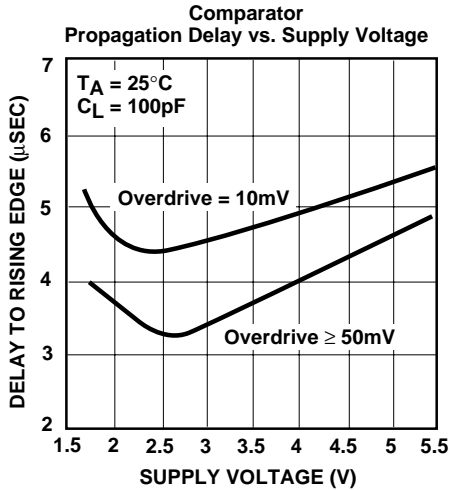


Figure 6. Pulse Width Modulator

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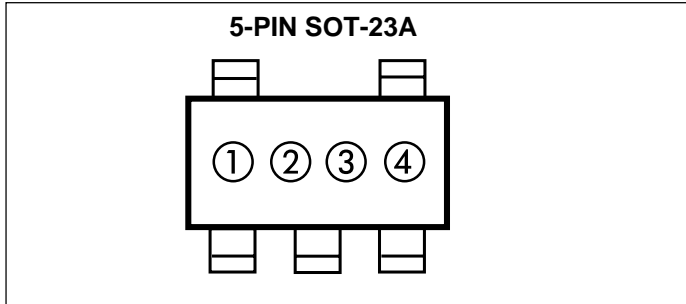
## TYPICAL CHARACTERISTICS



# Linear Building Block – Single Comparator in SOT Package

## TC1036

### MARKINGS



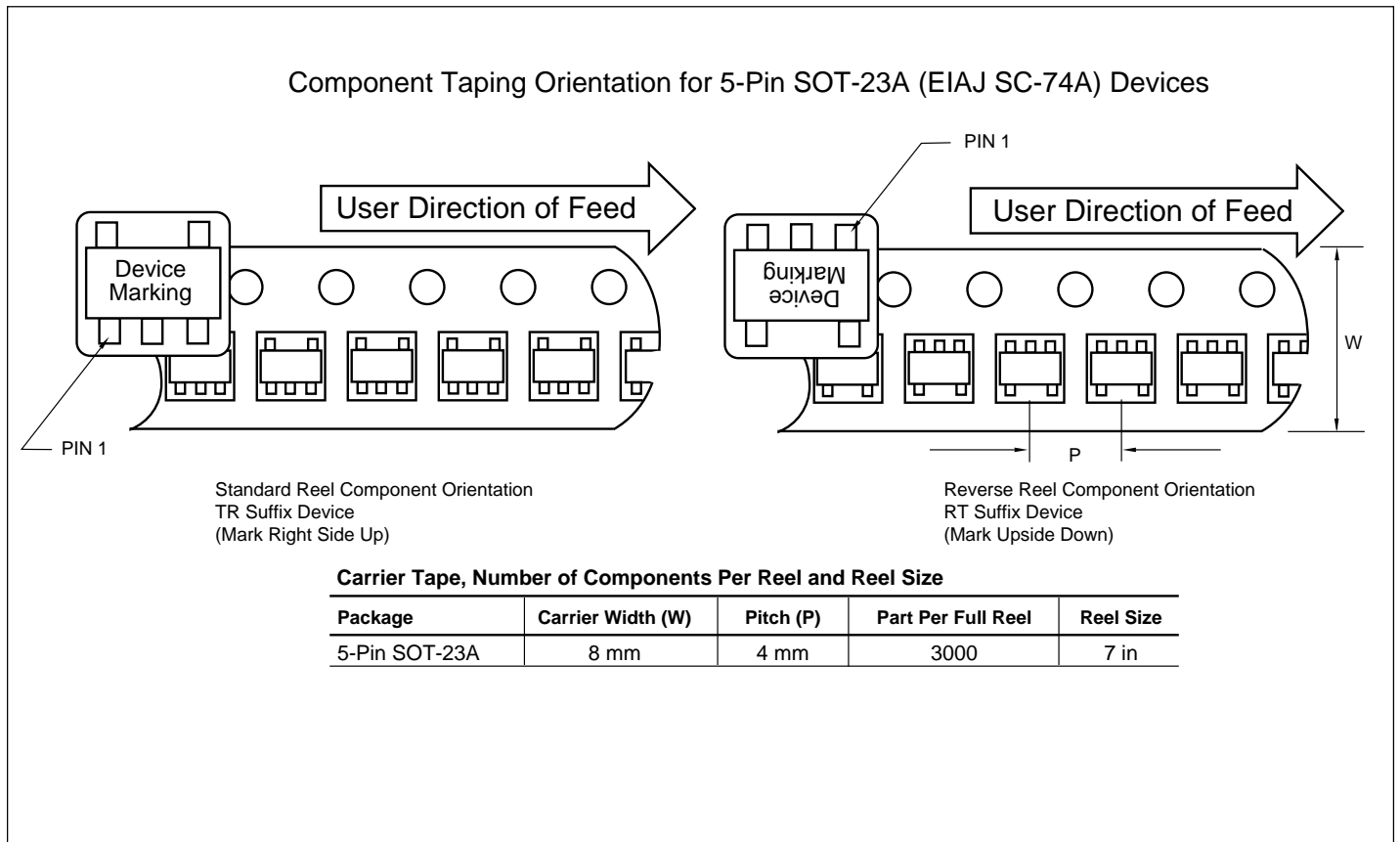
① & ② = part number code + temperature range and voltage

Part Number	Code
TC1036CECT	BP

ex: 1036CECT = (B)(P)○○

③ represents year and 2-month period code

④ represents lot ID number



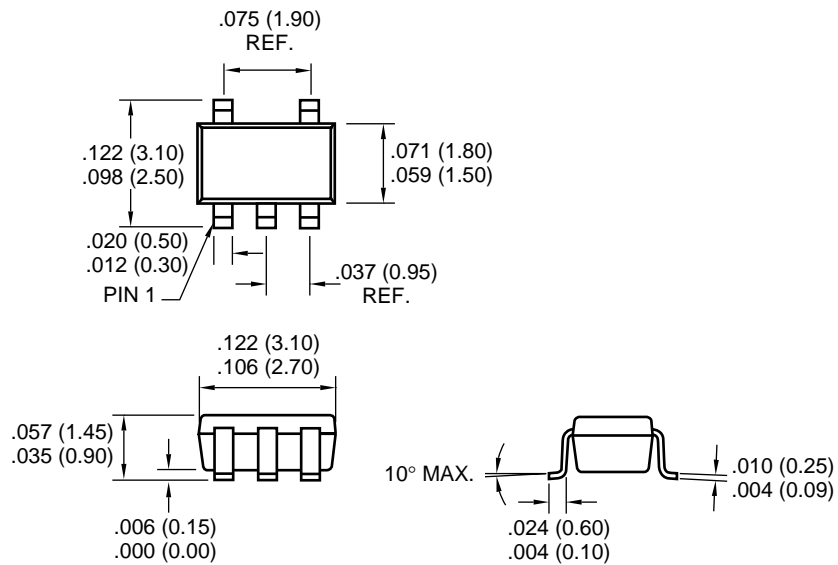


# Linear Building Block – Single Comparator in SOT Package

TC1036

## PACKAGE DIMENSIONS

5-Pin SOT-23A (EIAJ SC-74A)



Dimensions: inches (mm)



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