2.5 V to 5.5 V, 400 μA, Quad Voltage Output 8-/10-/12-Bit DACs in 16-Lead TSSOP

AD5307/AD5317/AD5327*

FEATURES

AD5307: Four Buffered 8-Bit DACs in 16-Lead TSSOP
AD5317: Four Buffered 10-Bit DACs in 16-Lead TSSOP
AD5327: Four Buffered 12-Bit DACs in 16-Lead TSSOP
Low Power Operation: 400 μA @ 3 V, 500 μA @ 5 V
2.5 V to 5.5 V Power Supply
Guaranteed Monotonic By Design over All Codes
Power-Down to 90 nA @ 3 V, 300 nA @ 5 V ($\overline{PD}$ Pin)
Double-Buffered Input Logic
Buffered/Unbuffered Reference Input Options
Output Range: 0–V_{REF} or 0–2 V_{REF}
Power-On-Reset to Zero Volts
Simultaneous Update of Outputs ($\overline{LDAC}$ Pin)
Asynchronous Clear Facility ($\overline{CLR}$ Pin)
Low Power, SPI™, QSPI™, MICROWIRE™ and DSP-Compatible 3-Wire Serial Interface
SDO Daisy-Chaining Option
On-Chip Rail-to-Rail Output Buffer Amplifiers
Temperature Range –40°C to +105°C

APPLICATIONS

Portable Battery-Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Programmable Attenuators
Industrial Process Control

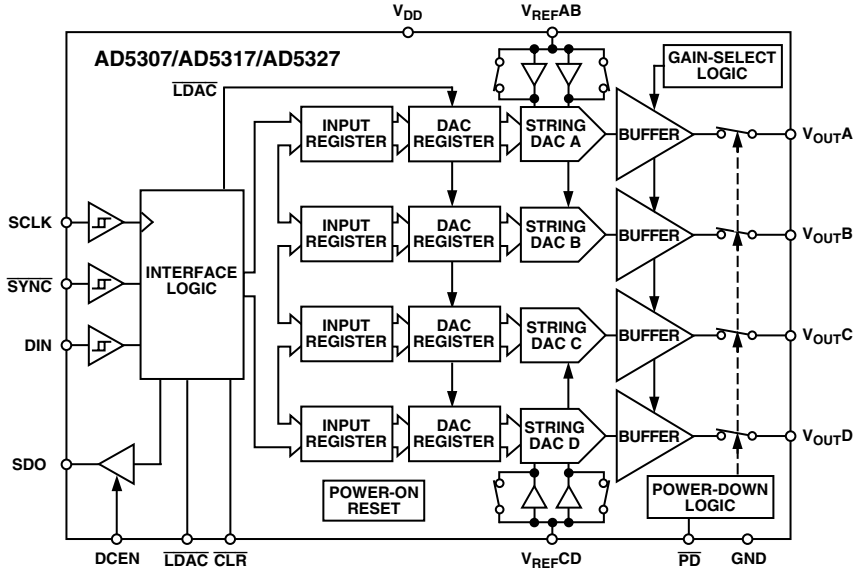
GENERAL DESCRIPTION

The AD5307/AD5317/AD5327 are quad 8-, 10-, and 12-bit buffered voltage-output DACs, in a 16-lead TSSOP package, which operate from a single 2.5 V to 5.5 V supply consuming 400 μA at 3 V. Their on-chip output amplifiers allow the outputs to swing rail-to-rail with a slew rate of 0.7 V/μs. The AD5307/AD5317/AD5327 utilize a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with standard SPI, QSPI, MICROWIRE, and DSP interface standards.

The references for the four DACs are derived from two reference pins (one per DAC pair). These reference inputs can be configured as buffered or unbuffered inputs. The parts incorporate a power-on-reset circuit that ensures that the DAC outputs power-up to 0 V and remain there until a valid write to the device takes place. There is also an asynchronous active-low $\overline{CLR}$ pin that clears all DACs to 0 V. The outputs of all DACs may be updated simultaneously using the asynchronous $\overline{LDAC}$ input. The parts contain a power-down feature that reduces the current consumption of the devices to 300 nA @ 5 V (90 nA @ 3 V). The parts may also be used in daisy-chaining applications using the SDO pin.

All three parts are offered in the same pinout, which allows users to select the amount of resolution appropriate for their application without redesigning their circuit board.

FUNCTIONAL BLOCK DIAGRAM



*Protected by U.S. Patent No. 5,969,657; other patents pending.
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MICROWIRE is a trademark of National Semiconductor Corporation.

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AD5307/AD5317/AD5327–SPECIFICATIONS (V_{DD} = 2.5 V to 5.5 V; V_{REF} = 2 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1]	B Version[2] Min	Typ	Max	Unit	Conditions/Comments
DC PERFORMANCE[3, 4]					
AD5307					
Resolution		8		Bits	
Relative Accuracy		±0.15	±1	LSB	
Differential Nonlinearity		±0.02	±0.25	LSB	Guaranteed Monotonic by Design Over All Codes
AD5317					
Resolution		10		Bits	
Relative Accuracy		±0.5	±4	LSB	
Differential Nonlinearity		±0.05	±0.5	LSB	Guaranteed Monotonic by Design Over All Codes
AD5327					
Resolution		12		Bits	
Relative Accuracy		±2	±16	LSB	
Differential Nonlinearity		±0.2	±1	LSB	Guaranteed Monotonic by Design Over All Codes
Offset Error		±5	±60	mV	V_{DD} = 4.5 V, Gain = 2; See Figures 4 and 5
Gain Error		±0.3	±1.25	% of FSR	V_{DD} = 4.5 V, Gain = 2; See Figures 4 and 5
Lower Deadband[5]		10	60	mV	See Figure 4. Lower Deadband Exists Only If Offset Error Is Negative
Upper Deadband[5]		10	60	mV	See Figure 5. Upper Deadband Exists Only If V_{REF} = V_{DD} and Offset Plus Gain Error is Positive
Offset Error Drift[6]		–12		ppm of FSR/°C	
Gain Error Drift[6]		–5		ppm of FSR/°C	
DC Power Supply Rejection Ratio[6]		–60		dB	ΔV_{DD} = ±10%
DC Crosstalk[6]		200		µV	R_L = 2 kΩ to GND or V_{DD}
DAC REFERENCE INPUTS[6]					
V_{REF} Input Range	1		V_{DD}	V	Buffered Reference Mode
	0.25		V_{DD}	V	Unbuffered Reference Mode
V_{REF} Input Impedance (R_{DAC})		>10		MΩ	Buffered Reference Mode and Power-Down Mode
	74	90		kΩ	Unbuffered Reference Mode. 0–V_{REF} Output Range
	37	45		kΩ	Unbuffered Reference Mode. 0–2 V_{REF} Output Range
Reference Feedthrough		–90		dB	Frequency = 10 kHz
Channel-to-Channel Isolation		–75		dB	Frequency = 10 kHz
OUTPUT CHARACTERISTICS[6]					
Minimum Output Voltage[7]		0.001		V	This is a measure of the minimum and maximum drive
Maximum Output Voltage[7]		V_{DD} – 0.001		V	capability of the output amplifier.
DC Output Impedance		0.5		Ω	
Short Circuit Current		25		mA	V_{DD} = 5 V
		16		mA	V_{DD} = 3 V
Power-Up Time		2.5		µs	Coming Out of Power-Down Mode. V_{DD} = 5 V
		5		µs	Coming Out of Power-Down Mode. V_{DD} = 3 V
LOGIC INPUTS[6]					
Input Current			±1	µA	
V_{IL}, Input Low Voltage			0.8	V	V_{DD} = 5 V ± 10%
			0.6	V	V_{DD} = 3 V ± 10%
			0.5	V	V_{DD} = 2.5 V
V_{IH}, Input High Voltage (excl. DCEN)	1.7			V	V_{DD} = 2.5 V to 5.5 V; TTL and 1.8 V CMOS-Compatible
V_{IH}, Input High Voltage (DCEN)	2.4			V	V_{DD} = 5 V ± 10%
	2.1			V	V_{DD} = 3 V ± 10%
	2.0			V	V_{DD} = 2.5 V
Pin Capacitance		3		pF	
LOGIC OUTPUT (SDO)[6]					
V_{DD} = 4.5 V to 5.5 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 2 mA
Output High Voltage, V_{OH}	V_{DD} –1			V	I_{SOURCE} = 2 mA
V_{DD} = 2.5 V to 3.6 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 2 mA
Output High Voltage, V_{OH}	V_{DD} –0.5			V	I_{SOURCE} = 2 mA
Floating-State Leakage Current			±1	µA	DCEN = GND
Floating State O/P Capacitance		3		pF	DCEN = GND
POWER REQUIREMENTS					
V_{DD}	2.5		5.5	V	
I_{DD} (Normal Mode)[8]					V_{IH} = V_{DD} and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		500	900	µA	All DACs in Unbuffered Mode. In Buffered Mode, extra
V_{DD} = 2.5 V to 3.6 V		400	750	µA	current is typically x µA per DAC where x = 5 µA + V_{REF}/R_{DAC}.
I_{DD} (Power-Down Mode)					V_{IH} = V_{DD} and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		0.3	1	µA	
V_{DD} = 2.5 V to 3.6 V		0.09	1	µA	

NOTES
[1]See Terminology.
[2]Temperature range: B Version: –40°C to +105°C; typical at 25°C.
[3]DC specifications tested with the outputs unloaded unless stated otherwise.
[4]Linearity is tested using a reduced code range: AD5307 (Code 8 to 255); AD5317 (Code 28 to 1023); AD5327 (Code 115 to 4095).
[5]This corresponds to x codes. x = Deadband Voltage/LSB size.
[6]Guaranteed by design and characterization; not production tested.
[7]For the amplifier output to reach its minimum voltage, Offset Error must be negative; for the amplifier output to reach its maximum voltage, $V_{REF} = V_{DD}$ and Offset plus Gain Error must be positive.
[8]Interface Inactive. All DACs active. DAC outputs unloaded.

Specifications subject to change without notice.

AC CHARACTERISTICS[1] (V_{DD} = 2.5 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[2]	B Version[3] Min	Typ	Max	Unit	Conditions/Comments
Output Voltage Settling Time					$V_{REF} = V_{DD}$ = 5 V
AD5307		6	8	µs	1/4 Scale to 3/4 Scale Change (40 Hex to C0 Hex)
AD5317		7	9	µs	1/4 Scale to 3/4 Scale Change (100 Hex to 300 Hex)
AD5327		8	10	µs	1/4 Scale to 3/4 Scale Change (400 Hex to C00 Hex)
Slew Rate		0.7		V/µs	
Major-Code Change Glitch Energy		12		nV sec	1 LSB Change Around Major Carry
Digital Feedthrough		0.5		nV sec	
SDO Feedthrough		4		nV sec	Daisy-Chain Mode; SDO Load is 10 pF
Digital Crosstalk		0.5		nV sec	
Analog Crosstalk		1		nV sec	
DAC-to-DAC Crosstalk		3		nV sec	
Multiplying Bandwidth		200		kHz	V_{REF} = 2 V ± 0.1 V p-p. Unbuffered Mode
Total Harmonic Distortion		–70		dB	V_{REF} = 2.5 V ± 0.1 V p-p. Frequency = 10 kHz

NOTES
[1]Guaranteed by design and characterization; not production tested.
[2]See Terminology.
[3]Temperature range: B Version: –40°C to +105°C; typical at 25°C.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2, 3] (V_{DD} = 2.5 V to 5.5 V; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
t_1	33	ns min	SCLK Cycle Time
t_2	13	ns min	SCLK High Time
t_3	13	ns min	SCLK Low Time
t_4	13	ns min	$\overline{SYNC}$ to SCLK Falling Edge Setup Time
t_5	5	ns min	Data Setup Time
t_6	4.5	ns min	Data Hold Time
t_7	0	ns min	SCLK Falling Edge to $\overline{SYNC}$ Rising Edge
t_8	50	ns min	Minimum $\overline{SYNC}$ High Time
t_9	20	ns min	$\overline{LDAC}$ Pulsewidth
t_{10}	20	ns min	SCLK Falling Edge to $\overline{LDAC}$ Rising Edge
t_{11}	20	ns min	$\overline{CLR}$ Pulsewidth
t_{12}	0	ns min	SCLK Falling Edge to $\overline{LDAC}$ Falling Edge
t_{13}[4, 5]	20	ns max	SCLK Rising Edge to SDO Valid (V_{DD} = 3.6 V to 5.5 V)
	25	ns max	SCLK Rising Edge to SDO Valid (V_{DD} = 2.5 V to 3.5 V)
t_{14}[5]	5	ns min	SCLK Falling Edge to $\overline{SYNC}$ Rising Edge
t_{15}[5]	8	ns min	$\overline{SYNC}$ Rising Edge to SCLK Rising Edge
t_{16}[5]	0	ns min	$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$ Falling Edge

NOTES
[1]Guaranteed by design and characterization; not production tested.
[2]All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[3]See Figures 2 and 3.
[4]This is measured with the load circuit of Figure 1. t_{13} determines maximum SCLK frequency in Daisy-Chain Mode.
[5]Daisy-Chain Mode only.

Specifications subject to change without notice.

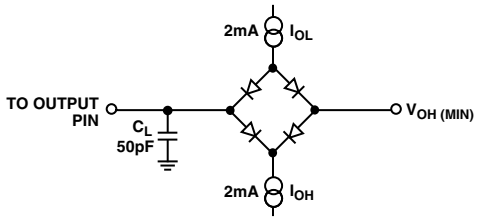


Figure 1. Load Circuit for Digital Output (SDO) Timing Specifications

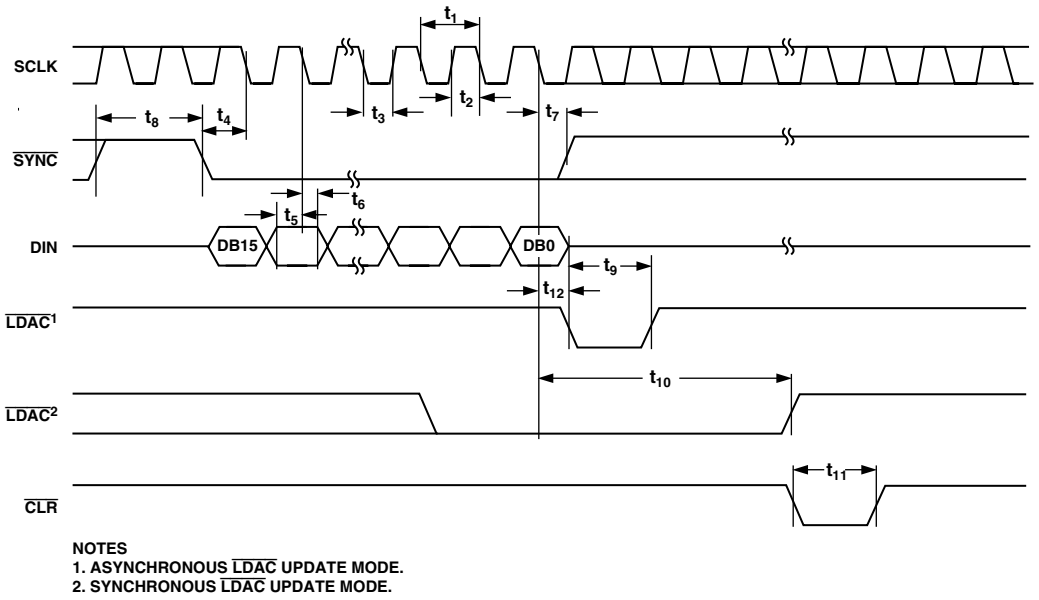


Figure 2. Serial Interface Timing Diagram

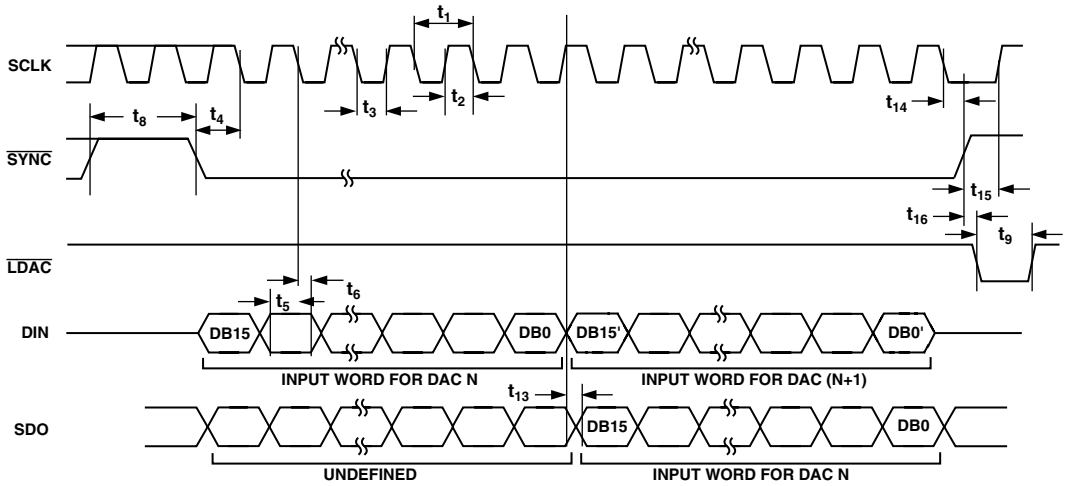


Figure 3. Daisy-Chaining Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = 25°C unless otherwise noted)

V_{DD} to GND . . . . . –0.3 V to +7 V
Digital Input Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND . . . . –0.3 V to V_{DD} + 0.3 V
$V_{OUT}A$–$V_{OUT}D$ to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Industrial (B Version) . . . . . –40°C to +105°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature (T_J max) . . . . . 150°C

16-Lead TSSOP Package
  Power Dissipation . . . . . (T_J max – T_A)/θ_{JA}
  θ_{JA} Thermal Impedance . . . . . 150.4°C/W
  Reflow Soldering
    Peak Temperature . . . . . 220 +5/–0°C
    Time at Peak Temperature . . . . . 10 sec to 40 sec

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch-up.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD5307BRU	–40°C to +105°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5317BRU	–40°C to +105°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5327BRU	–40°C to +105°C	Thin Shrink Small Outline Package (TSSOP)	RU-16

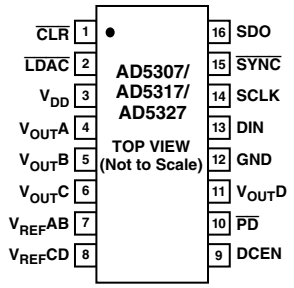
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5307/AD5317/AD5327 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	$\overline{\text{CLR}}$	Active low control input that loads all zeros to all input and DAC registers. Hence, the outputs also go to 0 V.
2	$\overline{\text{LDAC}}$	Active low control input that transfers the contents of the input registers to their respective DAC registers. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows simultaneous update of all DAC outputs. Alternatively this pin can be tied permanently low.
3	V_{DD}	Power Supply Input. These parts can be operated from 2.5 V to 5.5 V, and the supply should be decoupled with a 10 μF capacitor in parallel with a 0.1 μF capacitor to GND.
4	$V_{OUT}A$	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
5	$V_{OUT}B$	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
6	$V_{OUT}C$	Buffered Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
7	$V_{REF}AB$	Reference Input Pin for DACs A and B. It may be configured as a buffered or an unbuffered input to each or both of the DACs, depending on the state of the BUF bits in the serial input words to DACs A and B. It has an input range from 0.25 V to V_{DD} in unbuffered mode and from 1 V to V_{DD} in buffered mode.
8	$V_{REF}CD$	Reference Input Pin for DACs C and D. It may be configured as a buffered or an unbuffered input to each or both of the DACs, depending on the state of the BUF bits in the serial input words to DACs C and D. It has an input range from 0.25 V to V_{DD} in unbuffered mode and from 1 V to V_{DD} in buffered mode.
9	DCEN	This pin is used to enable the daisy-chaining option. This should be tied high if the part is being used in a daisy-chain. The pin should be tied low if it is being used in standalone mode.
10	$\overline{\text{PD}}$	Active low control input that acts as a hardware power-down option. All DACs go into power-down mode when this pin is tied low. The DAC outputs go into a high-impedance state and the current consumption of the part drops to 300 nA @ 5 V (90 nA @ 3 V)
11	$V_{OUT}D$	Buffered Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
12	GND	Ground reference point for all circuitry on the part.
13	DIN	Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input. The DIN input buffer is powered down after each write cycle.
14	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz. The SCLK input buffer is powered down after each write cycle.
15	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the following 16 clocks. If $\overline{\text{SYNC}}$ is taken high before the 16th falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.
16	SDO	Serial Data Output that can be used for daisy-chaining a number of these devices together or for reading back the data in the shift register for diagnostic purposes. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock.

PIN CONFIGURATION



TERMINOLOGY

RELATIVE ACCURACY

For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. Typical INL versus Code plots can be seen in TPCs 1, 2, and 3.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Typical DNL versus Code plots can be seen in TPCs 4, 5, and 6.

OFFSET ERROR

This is a measure of the offset error of the DAC and the output amplifier. (See Figures 4 and 5.) It can be negative or positive. It is expressed in mV.

GAIN ERROR

This is a measure of the span error of the DAC. It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

OFFSET ERROR DRIFT

This is a measure of the change in offset error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

GAIN ERROR DRIFT

This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

DC POWER-SUPPLY REJECTION RATIO (PSRR)

This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dBs. V_{REF} is held at 2 V and V_{DD} is varied ±10%.

DC CROSSTALK

This is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC. It is expressed in μV.

REFERENCE FEEDTHROUGH

This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (i.e., $\overline{\text{LDAC}}$ is high). It is expressed in dBs.

CHANNEL-TO-CHANNEL ISOLATION

This is the ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of another DAC. It is measured in dBs.

MAJOR-CODE TRANSITION GLITCH ENERGY

Major-code transition glitch energy is the energy of the impulse injected into the analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV secs and is measured when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00 or 100 . . . 00 to 011 . . . 11).

DIGITAL FEEDTHROUGH

Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device but is measured when the DAC is not being written to the ($\overline{\text{SYNC}}$ held high). It is specified in nV secs and is measured with a full-scale change on the digital input pins, i.e., from all 0s to all 1s or vice versa.

DIGITAL CROSSTALK

This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV secs.

ANALOG CROSSTALK

This is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{\text{LDAC}}$ high. Then pulse $\overline{\text{LDAC}}$ low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV secs.

DAC-TO-DAC CROSSTALK

This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV secs.

MULTIPLYING BANDWIDTH

The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

TOTAL HARMONIC DISTORTION

This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. It is measured in dBs.

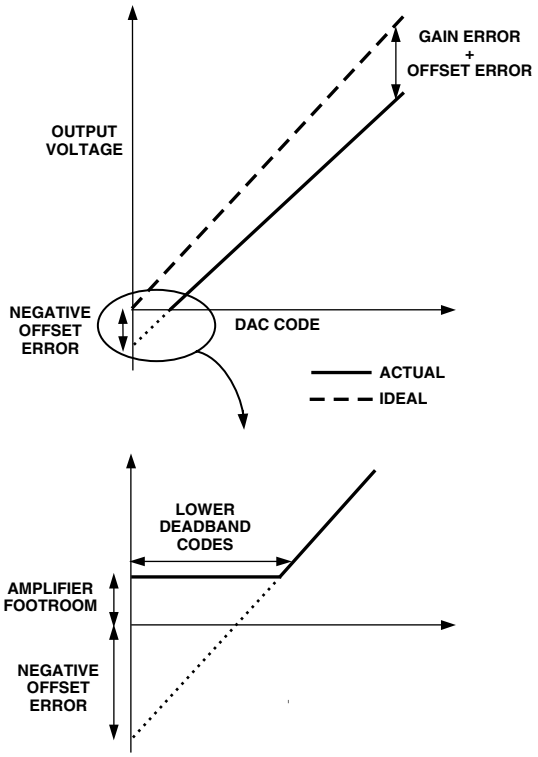


Figure 4. Transfer Function with Negative Offset

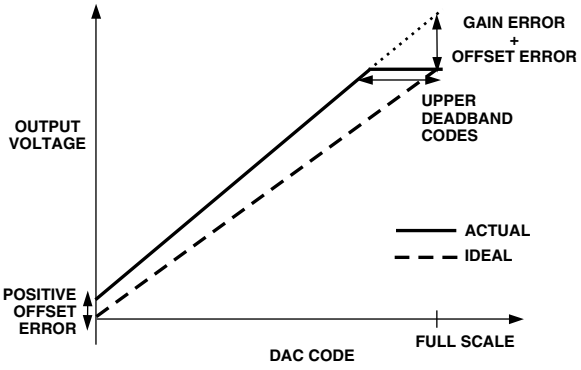
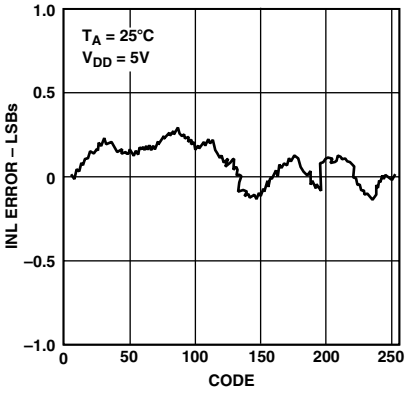
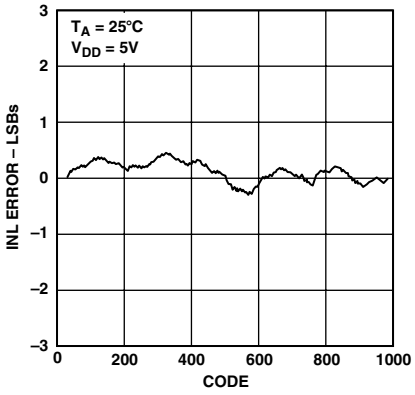


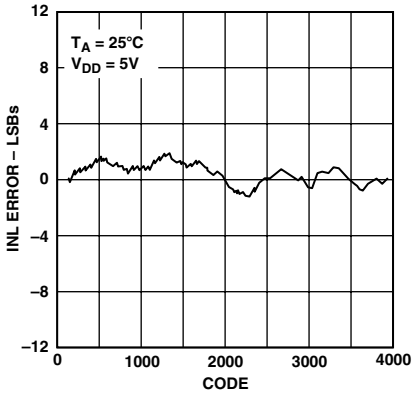
Figure 5. Transfer Function with Positive Offset ($V_{REF} = V_{DD}$)



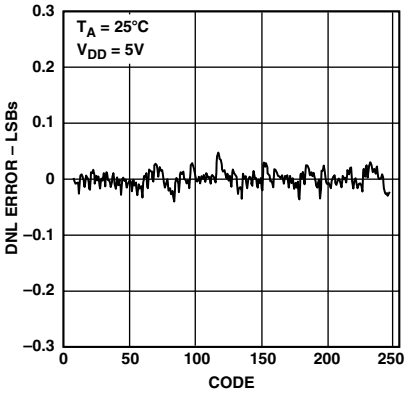
TPC 1. AD5307 Typical INL Plot



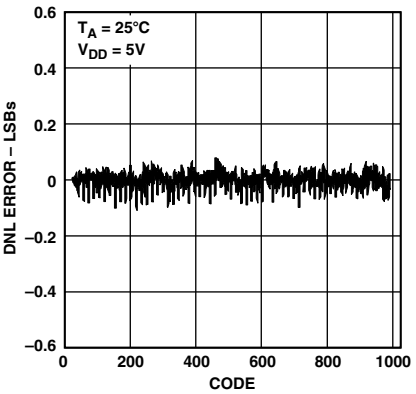
TPC 2. AD5317 Typical INL Plot



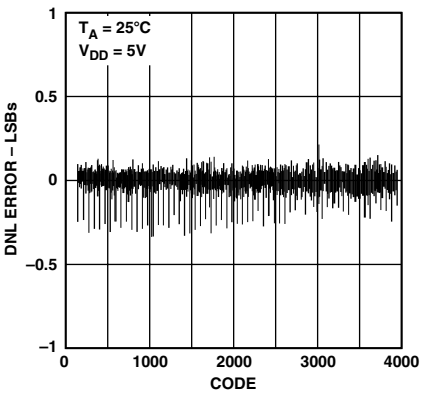
TPC 3. AD5327 Typical INL Plot



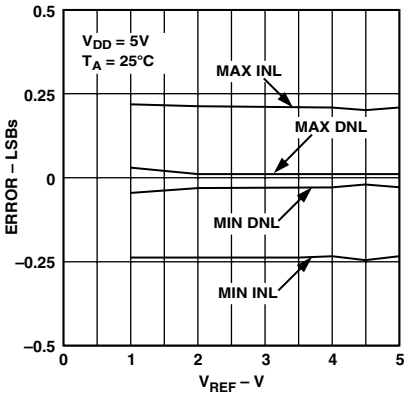
TPC 4. AD5307 Typical DNL Plot



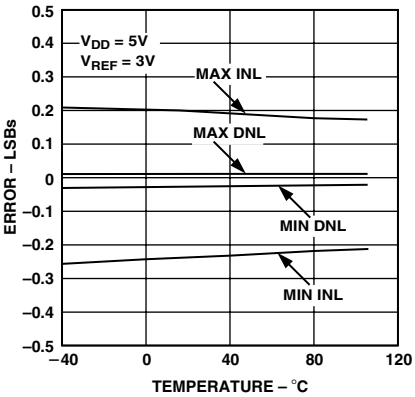
TPC 5. AD5317 Typical DNL Plot



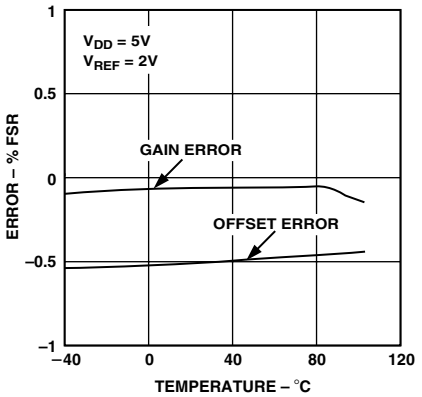
TPC 6. AD5327 Typical DNL Plot



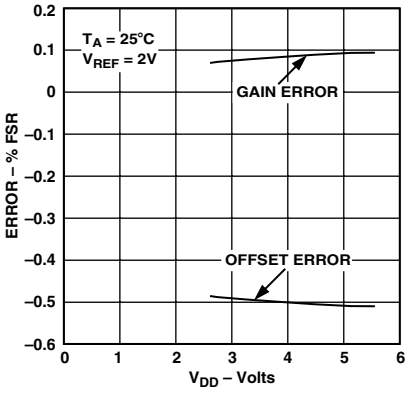
TPC 7. AD5307 INL and DNL Error vs. V_{REF}



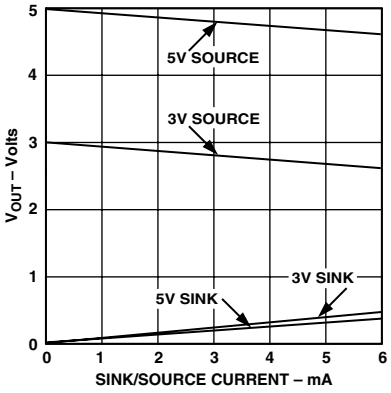
TPC 8. AD5307 INL Error and DNL Error vs. Temperature



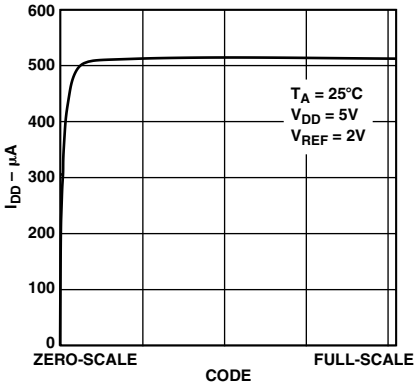
TPC 9. AD5307 Offset Error and Gain Error vs. Temperature



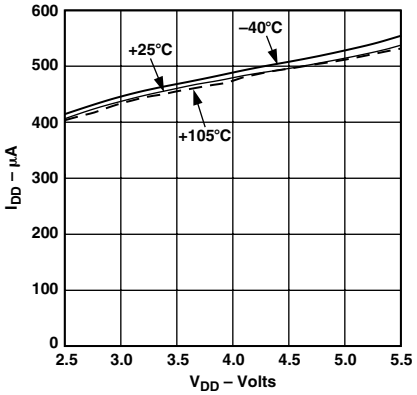
TPC 10. Offset Error and Gain Error vs. V_{DD}



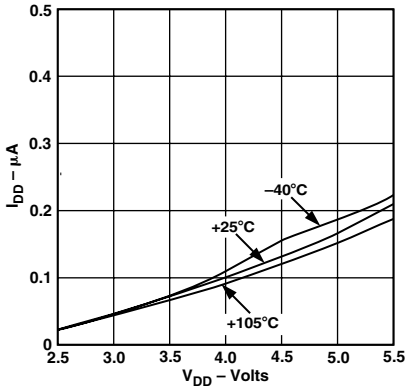
TPC 11. V_{OUT} Source and Sink Current Capability



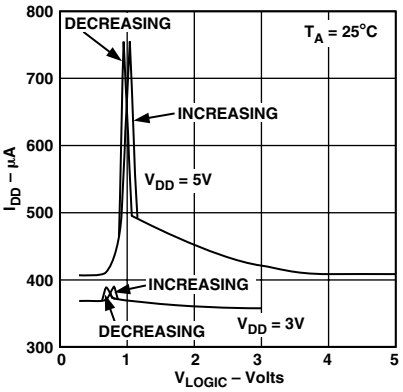
TPC 12. Supply Current vs. DAC Code



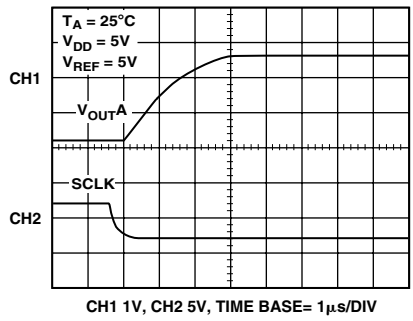
TPC 13. Supply Current vs. Supply Voltage



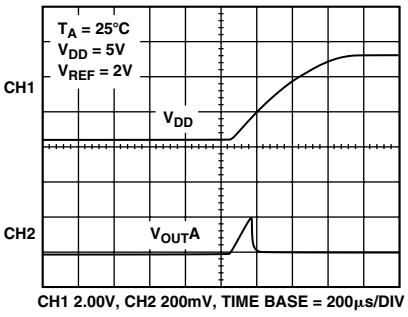
TPC 14. Power-Down Current vs. Supply Voltage



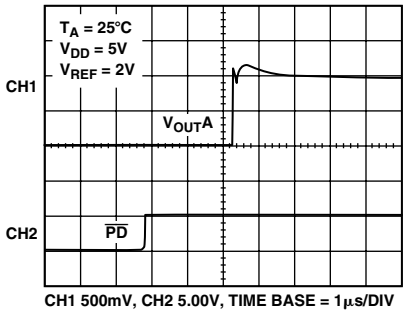
TPC 15. Supply Current vs. Logic Input Voltage for SCLK and DIN Increasing and Decreasing



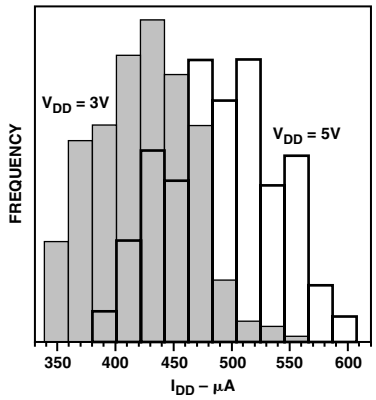
TPC 16. Half-Scale Settling (1/4 to 3/4 Scale Code Change)



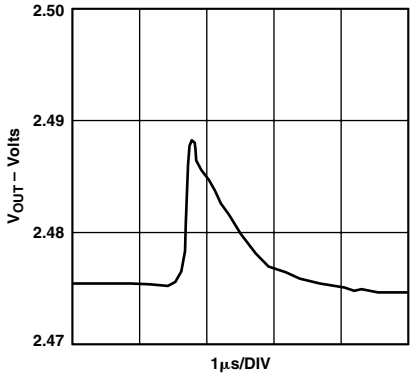
TPC 17. Power-On Reset to 0 V



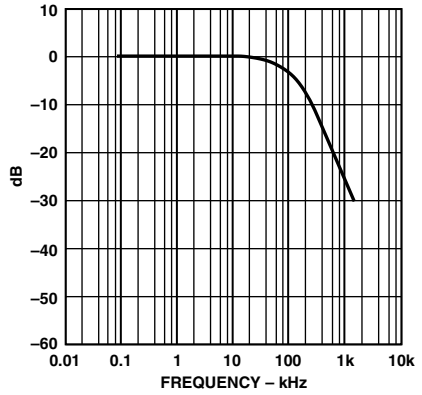
TPC 18. Exiting Power-Down to Midscale



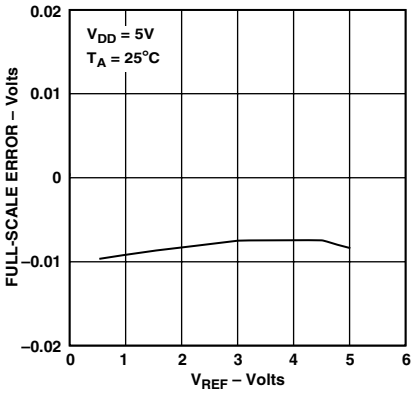
TPC 19. I_{DD} Histogram with V_{DD} = 3 V and V_{DD} = 5 V



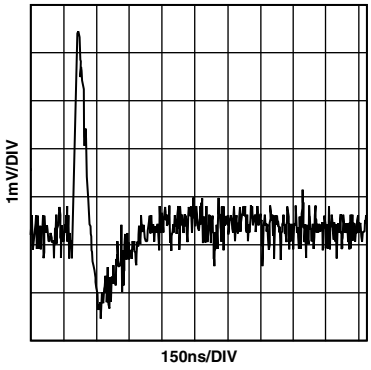
TPC 20. AD5327 Major-Code Transition Glitch Energy



TPC 21. Multiplying Bandwidth (Small-Signal Frequency Response)



TPC 22. Full-Scale Error vs. V_{REF}



TPC 23. DAC-to-DAC Crosstalk

FUNCTIONAL DESCRIPTION

The AD5307/AD5317/AD5327 are quad resistor-string DACs fabricated on a CMOS process with resolutions of 8, 10, and 12 bits respectively. Each contains four output buffer amplifiers and is written to via a 3-wire serial interface. They operate from single supplies of 2.5 V to 5.5 V and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7 V/μs. DACs A and B share a common reference input, namely $V_{REF}AB$. DACs C and D share a common reference input, namely $V_{REF}CD$. Each reference input may be buffered to draw virtually no current from the reference source, or unbuffered to give a reference input range from 0.25 V to V_{DD}. The devices have a power-down mode in which all DACs may be turned off completely with a high-impedance output.

Digital-to-Analog Section

The architecture of one DAC channel consists of a resistor-string DAC followed by an output buffer amplifier. The voltage at the V_{REF} pin provides the reference voltage for the corresponding DAC. Figure 6 shows a block diagram of the DAC architecture. Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where

D = decimal equivalent of the binary code that is loaded to the DAC register;

0–255 for AD5307 (8 Bits)
0–1023 for AD5317 (10 Bits)
0–4095 for AD5327 (12 Bits)

N = DAC resolution

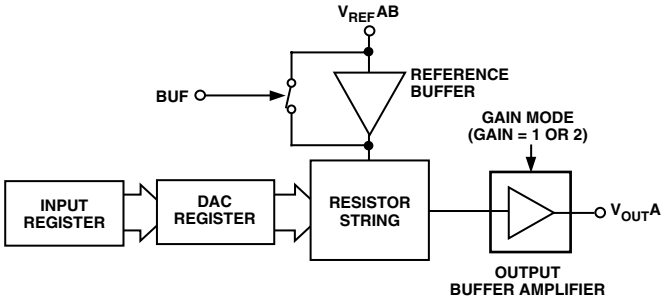


Figure 6. Single DAC Channel Architecture

Resistor String

The resistor string section is shown in Figure 7. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

DAC Reference Inputs

There is a reference pin for each pair of DACs. The reference inputs are buffered but can also be individually configured as unbuffered. The advantage with the buffered input is the high impedance it presents to the voltage source driving it. However, if the unbuffered mode is used, the user can have a reference voltage as low as 0.25 V and as high as V_{DD} since there is no restriction due to headroom and footroom of the reference amplifier.

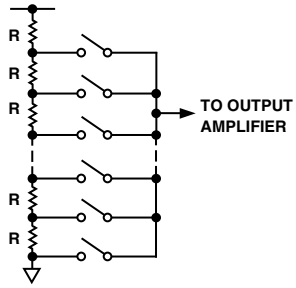


Figure 7. Resistor String

If there is a buffered reference in the circuit (e.g., REF192), there is no need to use the on-chip buffers of the AD5307/AD5317/AD5327. In unbuffered mode the input impedance is still large at typically 90 kΩ per reference input for 0–V_{REF} mode and 45 kΩ for 0–2 V_{REF} mode.

The buffered/unbuffered option is controlled by the BUF bit in the Data Word. The BUF bit setting applies to whichever DAC is selected.

Output Amplifier

The output buffer amplifier is capable of generating output voltages to within 1 mV of either rail. Its actual range depends on the value of V_{REF}, GAIN, offset error, and gain error.

If a gain of 1 is selected (GAIN = 0), the output range is 0.001 V to V_{REF}.

If a gain of 2 is selected (GAIN = 1), the output range is 0.001 V to 2 V_{REF}. Because of clamping, however, the maximum output is limited to V_{DD} – 0.001 V.

The output amplifier is capable of driving a load of 2 kΩ to GND or V_{DD}, in parallel with 500 pF to GND or V_{DD}. The source and sink capabilities of the output amplifier can be seen in the plot in TPC 11.

The slew rate is 0.7 V/μs with a half-scale settling time to ±0.5 LSB (at 8 bits) of 6 μs.

POWER-ON RESET

The AD5307/AD5317/AD5327 are provided with a power-on reset function, so that they power up in a defined state. The power-on state is:

- Normal Operation
- Reference Inputs Unbuffered
- 0–V_{REF} Output Range
- Output Voltage Set to 0 V

Both input and DAC registers are filled with zeros and remain so until a valid write sequence is made to the device. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering up.

SERIAL INTERFACE

The AD5307/AD5317/AD5327 are controlled over a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with SPI, QSPI, MICROWIRE and DSP interface standards.

Input Shift Register

The input shift register is 16 bits wide. Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK. The timing diagram for this operation is shown in Figure 2. The 16-bit word consists of four control bits followed by 8, 10, or 12 bits of DAC data, depending on the device type. Data is loaded MSB first (Bit 15) and the first two bits determine whether the data is for DAC A, DAC B, DAC C, or DAC D. Bits 13 and 12 control the operating mode of the DAC. Bit 13 is GAIN, which determines the output range of the part. Bit 12 is BUF, which controls whether the reference inputs are buffered or unbuffered.

Table I. Address Bits for the AD53x7

A1 (Bit 15)	A0 (Bit 14)	DAC Addressed
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

Control Bits

GAIN: Controls the output range of the addressed DAC
0: Output Range of 0–V_{REF}
1: Output Range of 0–2 V_{REF}

BUF: Controls whether reference of the addressed DAC is buffered or unbuffered
0: Unbuffered Reference
1: Buffered Reference

The AD5327 uses all 12 bits of DAC data, the AD5317 uses ten bits and ignores the two LSBs. The AD5307 uses eight bits and ignores the last four bits. The data format is straight binary, with all zeros corresponding to 0 V output and all ones corresponding to full-scale output (V_{REF} – 1 LSB).

The $\overline{SYNC}$ input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can only be transferred into the device while $\overline{SYNC}$ is low. To start the serial data transfer, $\overline{SYNC}$ should be taken low, observing the minimum $\overline{SYNC}$ to SCLK falling edge setup time, t_4. After $\overline{SYNC}$ goes low, serial data will be shifted into the device's input shift register on the falling edges of SCLK for 16 clock pulses. In Standalone Mode (DCEN = 0), any data and clock pulses after the sixteenth falling edge of SCLK will be ignored and no further serial data transfer will occur until $\overline{SYNC}$ is taken high and low again.

$\overline{SYNC}$ may be taken high after the falling edge of the sixteenth SCLK pulse, observing the minimum SCLK falling edge to $\overline{SYNC}$ rising edge time, t_7.

After the end of serial data transfer, data will automatically be transferred from the input shift register to the input register of the selected DAC. If $\overline{SYNC}$ is taken high before the 16th falling edge of SCLK, the data transfer will be aborted and the DAC input registers will not be updated.

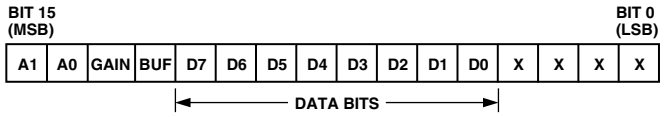


Figure 8. AD5307 Input Shift Register Contents

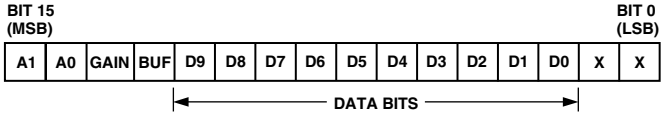


Figure 9. AD5317 Input Shift Register Contents

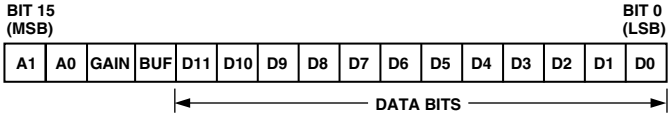


Figure 10. AD5327 Input Shift Register Contents

When data has been transferred into the input register of a DAC, the corresponding DAC register and DAC output can be updated by taking $\overline{\text{LDAC}}$ low. $\overline{\text{CLR}}$ is an active-low, asynchronous clear that clears the input registers and DAC registers to all zeros.

Low Power Serial Interface
To minimize the power consumption of the device, the interface only powers up fully when the device is being written to, i.e., on the falling edge of $\overline{\text{SYNC}}$. The SCLK and DIN input buffers are powered down on the rising edge of $\overline{\text{SYNC}}$.

Daisy-Chaining
For systems that contain several DACs, or where the user wishes to read back the DAC contents for diagnostic purposes, the SDO pin may be used to daisy-chain several devices together and provide serial readback.

By connecting the DCEN (Daisy-Chain Enable) pin high, the Daisy-Chain Mode is enabled. It is tied low in the case of Stand-alone Mode. In Daisy-Chain Mode the internal gating on SCLK is disabled. The SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 16 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting this line to the DIN input on the next DAC in the chain, a multi-DAC interface is constructed. Sixteen clock pulses are required for each DAC in the system. Therefore, the total number of clock cycles must equal 16N where N is the total number of devices in the chain. When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ should be taken high. This prevents any further data being clocked into the input shift register.

A continuous SCLK source may be used if it can be arranged that $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. Alternatively, a burst clock containing the exact number of clock cycles may be used and $\overline{\text{SYNC}}$ taken high some time later.

When the transfer to all input registers is complete, a common $\overline{\text{LDAC}}$ signal updates all DAC registers and all analog outputs are updated simultaneously.

Double-Buffered Interface
The AD5307/AD5317/AD5327 DACs all have double-buffered interfaces consisting of two banks of registers: input registers and DAC registers. The input registers are connected directly to the input shift register and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC registers contain the digital code used by the resistor strings.

Access to the DAC registers is controlled by the $\overline{\text{LDAC}}$ pin. When the $\overline{\text{LDAC}}$ pin is high, the DAC registers are latched and the input registers may change state without affecting the contents of the DAC registers. When $\overline{\text{LDAC}}$ is brought low, however, the DAC registers become transparent and the contents of the input registers are transferred to them.

The double-buffered interface is useful if the user requires simultaneous updating of all DAC outputs. The user may write to three of the input registers individually and then, by bringing $\overline{\text{LDAC}}$ low when writing to the remaining DAC input register, all outputs will update simultaneously.

These parts contain an extra feature whereby a DAC register is not updated unless its input register has been updated since the last time $\overline{\text{LDAC}}$ was brought low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers are filled with the contents of the input registers. In the case of the AD5307/AD5317/AD5327, the part will only update the DAC register if the input register has been changed since the last time the DAC register was updated thereby removing unnecessary digital crosstalk.

Load DAC Input ($\overline{\text{LDAC}}$)
$\overline{\text{LDAC}}$ transfers data from the input registers to the DAC registers (and hence updates the outputs). Use of the $\overline{\text{LDAC}}$ function enables double-buffering of the DAC data, GAIN, and BUF. There are two $\overline{\text{LDAC}}$ modes:

Synchronous Mode: In this mode the DAC registers are updated after new data is read in on the falling edge of the 16th SCLK pulse. $\overline{\text{LDAC}}$ can be tied permanently low or pulsed as in Figure 2.

Asynchronous Mode: In this mode the outputs are not updated at the same time that the input registers are written to. When $\overline{\text{LDAC}}$ goes low, the DAC registers are updated with the contents of the input register.

POWER-DOWN MODE
The AD5307/AD5317/AD5327 have low power consumption, typically dissipating 1.2 mW with a 3 V supply and 2.5 mW with a 5 V supply. Power consumption can be further reduced when the DACs are not in use by putting them into power-down mode, which is selected by taking pin $\overline{\text{PD}}$ low.

When the $\overline{\text{PD}}$ pin is high, all DACs work normally with a typical power consumption of 500 μA at 5 V (400 μA at 3 V). However, in power-down mode, the supply current falls to 300 nA at 5 V (90 nA at 3 V) when all DACs are powered down. Not only does the supply current drop, but the output stage is also internally switched from the output of the amplifier making it open-circuit. This has the advantage that the output is three-state while the part is in power-down mode and provides a defined input condition for whatever is connected to the output of the DAC amplifier. The output stage is illustrated in Figure 11.

The bias generator, the output amplifiers, the resistor string, and all other associated linear circuitry are shut down when the power-down mode is activated. However, the contents of the registers are unaffected when in power-down. In fact it is possible to load new data to the input registers and DAC registers during power-down. The DAC outputs will update as soon as $\overline{\text{PD}}$ goes high. The time to exit power-down is typically 2.5 μs for V_{DD} = 5 V and 5 μs when V_{DD} = 3 V. This is the time from the rising edge of $\overline{\text{PD}}$ to when the output voltage deviates from its power-down voltage. See TPC 18 for a plot.

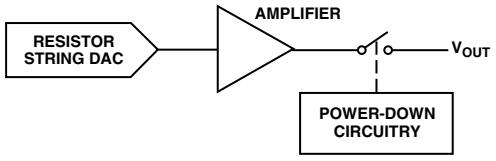


Figure 11. Output Stage During Power-Down

MICROPROCESSOR INTERFACING

ADSP-2101/ADSP-2103 to AD5307/AD5317/AD5327 Interface

Figure 12 shows a serial interface between the AD5307/AD5317/AD5327 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set up to operate in the SPORT Transmit Alternate Framing Mode. The ADSP-2101/ADSP-2103 SPORT is programmed through the SPORT control register and should be configured as follows: Internal Clock Operation, Active-Low Framing, 16-Bit Word Length. Transmission is initiated by writing a word to the TX register after the SPORT has been enabled. The data is clocked out on each rising edge of the DSP's serial clock and clocked into the AD5307/AD5317/AD5327 on the falling edge of the DAC's SCLK.

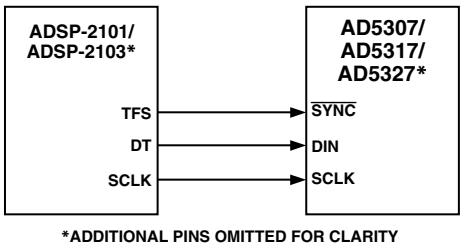


Figure 12. ADSP-2101/ADSP-2103 to AD5307/AD5317/AD5327 Interface

68HC11/68L11 to AD5307/AD5317/AD5327 Interface

Figure 13 shows a serial interface between the AD5307/AD5317/AD5327 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5307/AD5317/AD5327, while the MOSI output drives the serial data line (DIN) of the DAC. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows: the 68HC11/68L11 should be configured so that its CPOL bit is a 0 and its CPHA bit is a 1. When data is being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is taken low (PC7). When the 68HC11/68L11 is configured as above, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data to the AD5307/AD5317/AD5327, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC and PC7 is taken high at the end of this procedure.

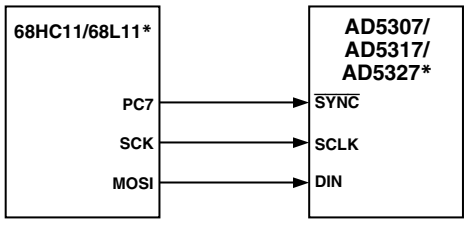


Figure 13. 68HC11/68L11 to AD5307/AD5317/AD5327 Interface

80C51/80L51 to AD5307/AD5317/AD5327 Interface

Figure 14 shows a serial interface between the AD5307/AD5317/AD5327 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TXD of the 80C51/80L51 drives SCLK of the AD5307/AD5317/AD5327, while RXD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is again derived from a bit programmable pin on the port. In this case port line P3.3 is used. When data is to be transmitted to the AD5307/AD5317/AD5327, P3.3 is taken low. The 80C51/80L51 transmits data only in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 outputs the serial data in a format which has the LSB first. The AD5307/AD5317/AD5327 requires its data with the MSB as the first bit received. The 80C51/80L51 transmit routine should take this into account.

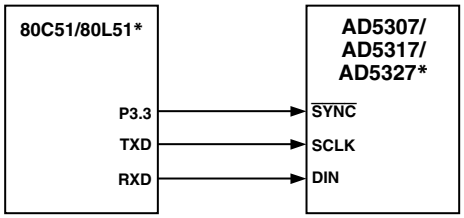


Figure 14. 80C51/80L51 to AD5307/AD5317/AD5327 Interface

MICROWIRE to AD5307/AD5317/AD5327 Interface

Figure 15 shows an interface between the AD5307/AD5317/AD5327 and any MICROWIRE compatible device. Serial data is shifted out on the falling edge of the serial clock, SK and is clocked into the AD5307/AD5317/AD5327 on the rising edge of SK, which corresponds to the falling edge of the DAC's SCLK.

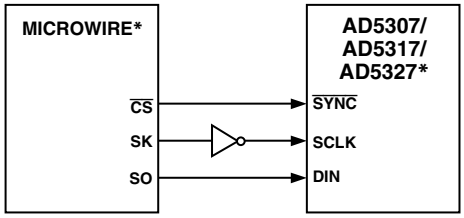


Figure 15. MICROWIRE to AD5307/AD5317/AD5327 Interface

APPLICATIONS

Typical Application Circuit

The AD5307/AD5317/AD5327 can be used with a wide range of reference voltages where the devices offer full, one-quadrant multiplying capability over a reference range of 0.25 V to V_{DD}. More typically, these devices are used with a fixed, precision reference voltage. Suitable references for 5 V operation are the AD780 and REF192 (2.5 V references). For 2.5 V operation, a suitable external reference would be the AD589, a 1.23 V bandgap reference. Figure 16 shows a typical setup for the AD5307/AD5317/AD5327 when using an external reference.

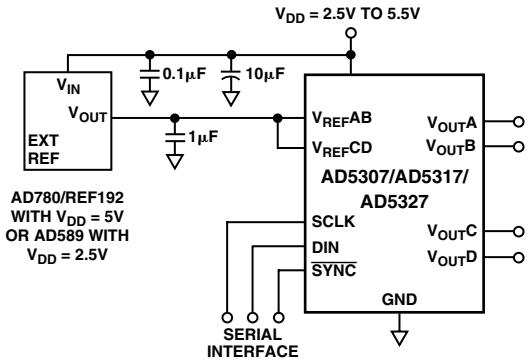


Figure 16. AD5307/AD5317/AD5327 Using a 2.5 V External Reference

Driving V_{DD} from the Reference Voltage

If an output range of 0 V to V_{DD} is required when the reference inputs are configured as unbuffered, the simplest solution is to connect the reference input to V_{DD}. As this supply may be noisy and not very accurate, the AD5307/AD5317/AD5327 may be powered from the reference voltage; for example, using a 5 V reference such as the REF195. The REF195 will output a steady supply voltage for the AD5307/AD5317/AD5327. The typical current required from the REF195 is 500 µA supply current and ≈ 112 µA into the reference inputs (if unbuffered). This is with no load on the DAC outputs. When the DAC outputs are loaded, the REF195 also needs to supply the current to the loads. The total current required (with a 10 kΩ load on each output) is:

$$612\ \mu A + 4(5\ V/10\ k\Omega) = 2.6\ mA$$

The load regulation of the REF195 is typically 2 ppm/mA, which results in an error of 5.2 ppm (26 µV) for the 2.6 mA current drawn from it. This corresponds to a 0.0013 LSB error at 8 bits and 0.021 LSB error at 12 bits.

Bipolar Operation Using the AD5307/AD5317/AD5327

The AD5307/AD5317/AD5327 have been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 17. This circuit will give an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_{OUT} = [(REFIN \times D/2^N) \times (R1 + R2)/R1 - REFIN \times (R2/R1)]$$

where:

D is the decimal equivalent of the code loaded to the DAC.

N is the DAC resolution.

REFIN is the reference voltage input.

With *REFIN* = 5 V, R1 = R2 = 10 kΩ:

$$V_{OUT} = (10 \times D/2^N) - 5\ V$$

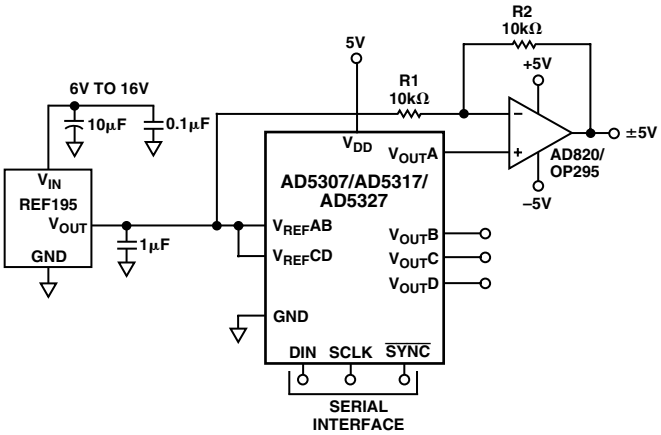


Figure 17. Bipolar Operation with the AD5307/AD5317/AD5327

Opto-Isolated Interface for Process Control Applications

The AD5307/AD5317/AD5327 have a versatile 3-wire serial interface making them ideal for generating accurate voltages in process control and industrial applications. Due to noise, safety requirements, or distance, it may be necessary to isolate the AD5307/AD5317/AD5327 from the controller. This can easily be achieved by using opto-isolators that will provide isolation in excess of 3 kV. The actual data rate achieved may be limited by the type of optocouplers chosen. The serial loading structure of the AD5307/AD5317/AD5327 makes them ideally suited for use in opto-isolated applications. Figure 18 shows an opto-isolated interface to the AD5307/AD5317/AD5327 where DIN, SCLK, and $\overline{\text{SYNC}}$ are driven from optocouplers. The power supply to the part also needs to be isolated. This is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5307/AD5317/AD5327.

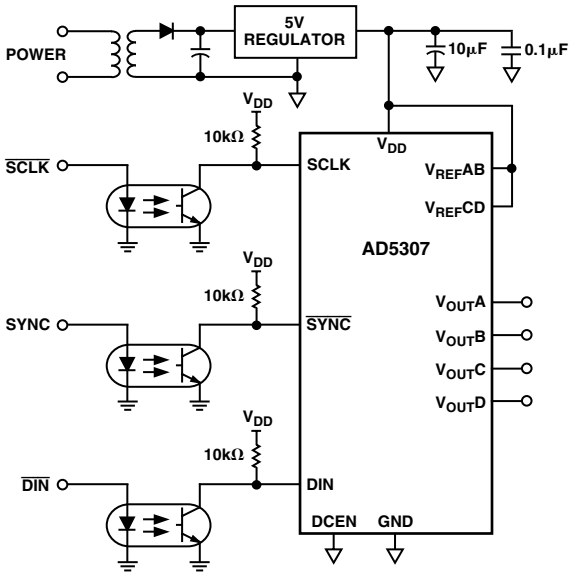


Figure 18. AD5307 in an Opto-Isolated Interface

Decoding Multiple AD5307/AD5317/AD5327s

The $\overline{\text{SYNC}}$ pin on the AD5307/AD5317/AD5327 can be used in applications to decode a number of DACs. In this application, all the DACs in the system receive the same serial clock and serial data, but only the $\overline{\text{SYNC}}$ to one of the devices will be active at any one time allowing access to four channels in this sixteen-channel system. The 74HC139 is used as a 2-to-4 line decoder to address any of the DACs in the system. To prevent timing errors from occurring, the enable input should be brought to its inactive state while the coded address inputs are changing state. Figure 19 shows a diagram of a typical setup for decoding multiple AD5307 devices in a system.

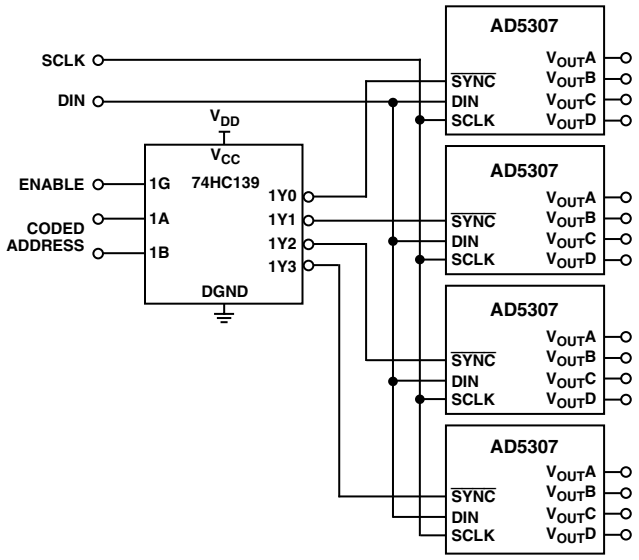


Figure 19. Decoding Multiple AD5307 Devices in a System

AD5307/AD5317/AD5327 as a Digitally Programmable Window Detector

A digitally programmable upper/lower limit detector using two of the DACs in the AD5307/AD5317/AD5327 is shown in Figure 20. The upper and lower limits for the test are loaded to DACs A and B which, in turn, set the limits on the CMP04. If the signal at the V_{IN} input is not within the programmed window, an LED will indicate the fail condition. Similarly DACs C and D can be used for window detection on a second V_{IN} signal.

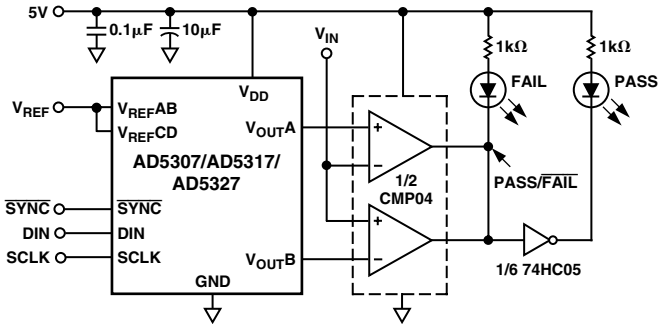


Figure 20. Window Detection

Daisy-Chaining

For systems that contain several DACs, or where the user wishes to read back the DAC contents for diagnostic purposes, the SDO pin may be used to daisy-chain several devices together and provide serial readback. Figure 3 shows the timing diagram for Daisy-Chain applications. The Daisy-Chain Mode is enabled by connecting DCEN high. See Figure 21 below.

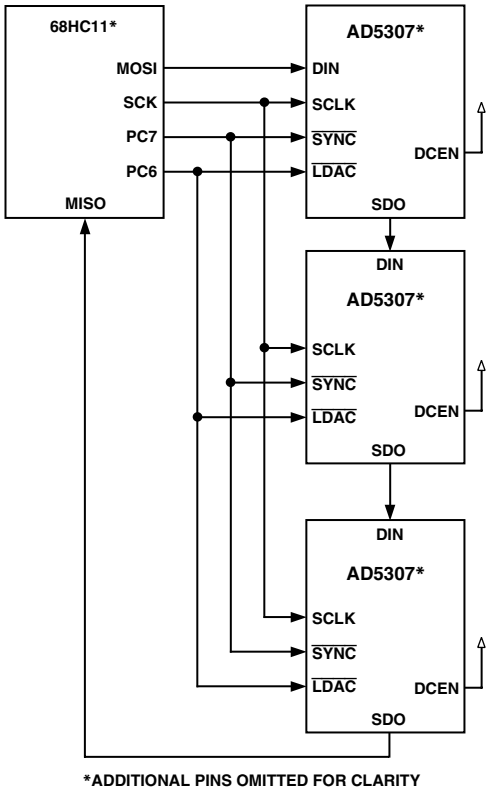


Figure 21. AD5307 in Daisy-Chain Mode

Power Supply Bypassing and Grounding

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5307/AD5317/AD5327 is mounted should be designed so that the analog and digital sections are separated, and confined to certain areas of the board. If the AD5307/AD5317/AD5327 is in a system where multiple devices require an AGND to DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. The AD5307/AD5317/AD5327 should have ample supply bypassing of 10 μF in parallel with 0.1 μF on the supply located as close to the package as possible, ideally right up against the device. The 10 μF capacitors are the tantalum bead type. The 0.1 μF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5307/AD5317/AD5327 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

Table II. Overview of AD53xx Serial Devices

Part No.	Resolution	No. of DACs	DNL	Interface	Settling Time	Package	Pins
SINGLES							
AD5300	8	1	±0.25	SPI	4 µs	SOT-23, microSOIC	6, 8
AD5310	10	1	±0.5	SPI	6 µs	SOT-23, microSOIC	6, 8
AD5320	12	1	±1.0	SPI	8 µs	SOT-23, microSOIC	6, 8
AD5301	8	1	±0.25	2-Wire	6 µs	SOT-23, microSOIC	6, 8
AD5311	10	1	±0.5	2-Wire	7 µs	SOT-23, microSOIC	6, 8
AD5321	12	1	±1.0	2-Wire	8 µs	SOT-23, microSOIC	6, 8
DUALS							
AD5302	8	2	±0.25	SPI	6 µs	microSOIC	8
AD5312	10	2	±0.5	SPI	7 µs	microSOIC	8
AD5322	12	2	±1.0	SPI	8 µs	microSOIC	8
AD5303	8	2	±0.25	SPI	6 µs	TSSOP	16
AD5313	10	2	±0.5	SPI	7 µs	TSSOP	16
AD5323	12	2	±1.0	SPI	8 µs	TSSOP	16
QUADS							
AD5304	8	4	±0.25	SPI	6 µs	microSOIC	10
AD5314	10	4	±0.5	SPI	7 µs	microSOIC	10
AD5324	12	4	±1.0	SPI	8 µs	microSOIC	10
AD5305	8	4	±0.25	2-Wire	6 µs	microSOIC	10
AD5315	10	4	±0.5	2-Wire	7 µs	microSOIC	10
AD5325	12	4	±1.0	2-Wire	8 µs	microSOIC	10
AD5306	8	4	±0.25	2-Wire	6 µs	TSSOP	16
AD5316	10	4	±0.5	2-Wire	7 µs	TSSOP	16
AD5326	12	4	±1.0	2-Wire	8 µs	TSSOP	16
AD5307	8	4	±0.25	SPI	6 µs	TSSOP	16
AD5317	10	4	±0.5	SPI	7 µs	TSSOP	16
AD5327	12	4	±1.0	SPI	8 µs	TSSOP	16

Visit our web-page at http://www.analog.com/support/standard_linear/selection_guides/AD53xx.html

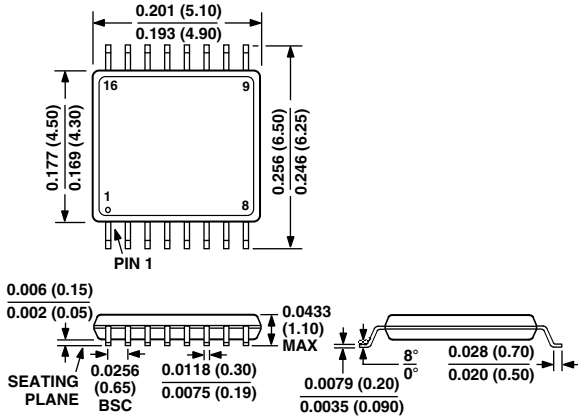
Table III. Overview of AD53xx Parallel Devices

Part No.	Resolution	DNL	V_{REF} Pins	Settling Time	Additional Pin Functions				Package	Pins
SINGLES					**BUF**	**GAIN**	**HBEN**	**$\overline{CLR}$**		
AD5330	8	±0.25	1	6 µs	✓	✓		✓	TSSOP	20
AD5331	10	±0.5	1	7 µs		✓		✓	TSSOP	20
AD5340	12	±1.0	1	8 µs	✓	✓		✓	TSSOP	24
AD5341	12	±1.0	1	8 µs	✓	✓	✓	✓	TSSOP	20
DUALS										
AD5332	8	±0.25	2	6 µs				✓	TSSOP	20
AD5333	10	±0.5	2	7 µs	✓	✓		✓	TSSOP	24
AD5342	12	±1.0	2	8 µs	✓	✓		✓	TSSOP	28
AD5343	12	±1.0	1	8 µs			✓	✓	TSSOP	20
QUADS										
AD5334	8	±0.25	2	6 µs		✓		✓	TSSOP	24
AD5335	10	±0.5	2	7 µs			✓	✓	TSSOP	24
AD5336	10	±0.5	4	7 µs		✓		✓	TSSOP	28
AD5344	12	±1.0	4	8 µs					TSSOP	28

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Small Outline Package (TSSOP)
(RU-16)



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