ANALOG DEVICES

16-Channel 14-Bit Voltage-Output DAC

Preliminary Technical Data AD5517-1/AD5517-2/AD5517-3*

FEATURES

High Integration: 16-channel DAC in 12x12 mm^2 LFBGA
Guaranteed Monotonic
Low Power, SPI™, MICROWIRE™ and DSP-Compatible 3-Wire Serial Interface
Output Impedance 0.5Ω
Output Voltage Range
- **± 2.5 V (AD5517-1)**
- **± 5 V (AD5517-2)**
- **± 10V (AD5517-3)**

Asynchronous $\overline{\text{RESET}}$ facility
Daisy-Chaining Option
Temperature Range -40°C to +85°C

APPLICATIONS

Level Setting
Instrumentation
Automatic Test Equipment
Optical Networks
Industrial Control Systems
Data Acquisition
Low Cost I/O

GENERAL DESCRIPTION

The AD5517 is a 16-channel voltage-output 14-bit DAC. The selected DAC register is written to via the 3-wire serial interface. DAC selection is accomplished via address bits A3-A0. 14-bit resolution is achieved by fine adjusment in Mode 2. The serial interface operates at clock rates up to 20 MHz and is compatible with standard SPI, MICROWIRE and DSP interface standards. The output voltage range is fixed at ±2.5 V (AD5517-1), ±5 V (AD5517-2) and ±10 V (AD5517-3). Access to the feedback resistor in each channel is provided via $R_{FB}0$ to $R_{BF}15$ pins.

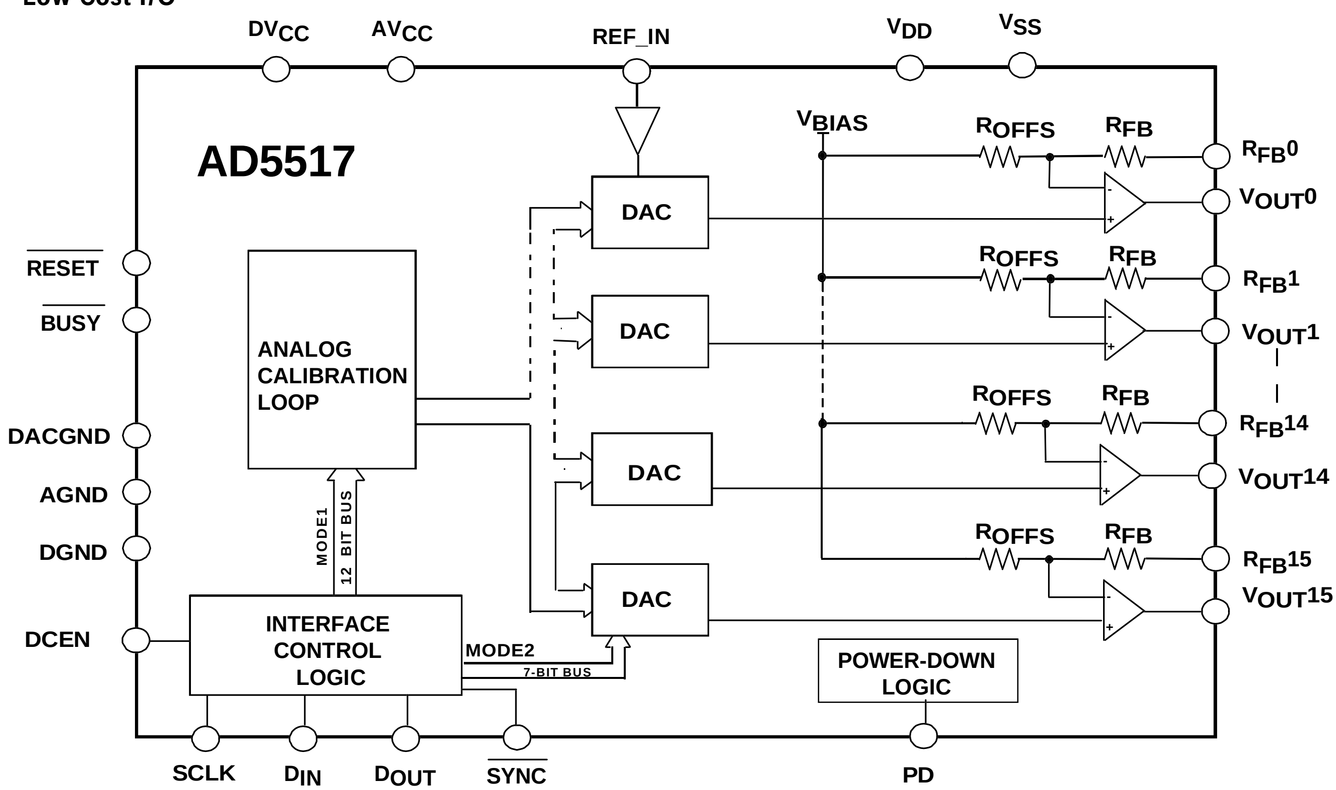
The device is operated with AVcc = 5 V ± 5%, DVcc = 2.7 V to 5.25 V, V_{SS} = -4.75 V to -12 V and V_{DD} = 4.75 V to 12 V and requires a stable 2.5 V reference on REF_IN.

PRODUCT HIGHLIGHTS

1. 16 14-bit DACs in one package, guaranteed monotonic.

2. The AD5517 is available in a 74-lead LFBGA package with a body size of 12mm by 12mm.

FUNCTIONAL BLOCK DIAGRAM



*Protected by U.S. Patent Nos. 5,684,481 and 5,969,657; other patents pending.
SPI and **QSPI** are Trademarks of Motorola, Inc.
MICROWIRE is a Trademark of National Semiconductor Corporation.

REV. PrA 2/01

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD5517-1/AD5517-2/AD5517-3 SPECIFICATIONS

(V_{DD} = 4.75 V to 12 V, V_{SS} = -4.75 V to -12 V; AV_{CC} = 4.75 V to 5.25 V; DV_{CC} = 2.7 V to 5.25 V; AGND = DGND = DACGND = 0 V; REF_IN = 2.5 V; All outputs unloaded. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1]	A Version[2]	Units	Conditions/Comments
DAC DC PERFORMANCE			
Resolution	14	Bits	
Integral Nonlinearity (INL)	±8	LSB max	Mode1 Operation
Differential Nonlinearity (DNL)	±1	LSB max	±0.5 LSB typ, Monotonic; Mode2
Bipolar Zero Error	TBD	LSB max	
Positive Fullscale Error	TBD	LSB max	
Negative Fullscale Error	TBD	LSB max	
VOLTAGE REFERENCE			
REF_IN			
Nominal Input Voltage	2.5	V	
Input Voltage Range[3]	2.375/2.625	V min/max	
Input Current	±1	μA max	< 1 nA typ
ANALOG OUTPUTS (V_{OUT} 0-15)			
Output Temperature Coefficient[3,4]	10	ppm/°C typ	
DC Output Impedance[3]	0.5	Ω typ	
Output Range[5]			
AD5516-1	±2.5	V typ	100 μA output load
AD5516-2	±5	V typ	100 μA output load
AD5516-3	±10	V typ	100 μA output load
Resistive Load[3,6]	5	kΩ min	
Capacitive Load[3,6]	100	pF max	
Short-Circuit Current[3]	10	mA typ	
DC Power-Supply Rejection Ratio[3]	-70	dB typ	V_{DD} = 10 V ± 5%
	-70	dB typ	V_{SS} = -10 V ± 5%
DC Crosstalk[3]	120	μV max	
DIGITAL INPUTS[3]			
Input Current	±10	μA max	±5 μA typ
Input Low Voltage	0.8	V max	DV_{CC} = 5 V ± 5%
	0.4	V max	DV_{CC} = 3 V ± 10%
Input High Voltage	2.4	V min	DV_{CC} = 5 V ± 5%
	2.0	V min	DV_{CC} = 3 V ± 10%
Input Hysteresis (SCLK and $\overline{SYNC}$)	200	mV typ	
Input Capacitance	10	pF max	
DIGITAL OUTPUTS ($\overline{BUSY}$, D_{OUT})[3]			
Output Low Voltage, DV_{CC} = 5V	0.4	V max	Sinking 200 μA
Output High Voltage, DV_{CC} = 5V	4.0	V min	Sourcing 200 μA
Output Low Voltage, DV_{CC} = 3V	0.4	V max	Sinking 200 μA
Output High Voltage, DV_{CC} = 3V	2.4	V min	Sourcing 200 μA
High Impedance Leakage Current (D_{OUT} only)	±1	μA max	DCEN = 0
High Impedance Output Capacitance (D_{OUT} only)	15	pF typ	DCEN = 0
Power-Supply Voltages			
V_{DD}	+4.75/+12	V min/max	
V_{SS}	-4.75/-12	V min/max	
AV_{CC}	+4.75/+5.25	V min/max	
DV_{CC}	+2.7/+5.25	V min/max	
Power-Supply Currents[7]			
I_{DD}	7.5	mA max	5 mA typ. All channels Fullscale
I_{SS}	7.5	mA max	5 mA typ. All channels Fullscale
AI_{CC}	16.5	mA max	13 mA typ
DI_{CC}	1.5	mA max	1 mA typ
Power Dissipation[7]	115	mW typ	V_{DD} = 5 V, V_{SS} = -5 V

NOTES:
[1]See Terminology
[2]A Version: Industrial temperature range -40°C to +85°C; typical at +25°C.
[3]Guaranteed by design and characterization, not production tested.
[4]AD780 as reference for the AD5517.
[5]Output range is restricted from V_{SS} + 2 V to V_{DD} - 2 V
[6]Ensure that you do not exceed Tj(max). See Maximum ratings.
[7]Outputs Unloaded.
Specifications subject to change without notice

AC Characteristics

(V_{DD} = 4.75V to 12V, V_{SS} = -4.75V to -12V; AV_{CC} = 4.75V to 5.25V; DV_{CC} = 2.7V to 5.25V; AGND = DGND = DACGND = 0V; REF_IN = 2.5 V; All outputs unloaded. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1,2]	A Version[3]	Units	Conditions/ Comments
Output Voltage Settling Time[4]	20	µs max	100 pF, 5 kΩ Load Full Scale change
Slew Rate	0.85	V/µs typ	
Digital-to-Analog Glitch Impulse	1	nV-s typ	1 LSB change around major carry
Digital Crosstalk	5	nV-s typ	
Analog Crosstalk	1	nV-s typ	
Digital Feedthrough	0.2	nV-s typ	
Output Noise Spectral Density @ 1kHz	400	$nV/(Hz)^{1/2}$ typ	

NOTES:
[1]See Terminology
[2]Guaranteed by design and characterization, not production tested
[3]A version: Industrial temperature range -40°C to +85°C
[4]Timed from the end of a write sequence
Specifications subject to change without notice

Timing Characteristics

(V_{DD} = 4.75 V to 12 V, V_{SS} = -4.75 V to -12 V; AV_{CC} = 4.75 V to 5.25 V; DV_{CC} = 2.7 V to 5.25 V; AGND = DGND = DACGND = 0 V; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1,2,3]	Limit at T_{MIN}, T_{MAX} (A Version)	Units	Conditions/Comments
$f_{UPDATE1}$	50	kHz max	DAC Update Rate (Mode 1)
$f_{UPDATE2}$	900	kHz max	DAC Update Rate (Mode 2)
f_{CLKIN}	20	MHz max	SCLK Frequency
t_1	20	ns min	SCLK High Pulse Width
t_2	20	ns min	SCLK Low Pulse Width
t_3	10	ns min	$\overline{\text{SYNC}}$ Falling Edge to SCLK Falling Edge Setup Time
t_4	5	ns min	D_{IN} Setup Time
t_5	5	ns min	D_{IN} Hold Time
t_6	0	ns min	SCLK Falling Edge to $\overline{\text{SYNC}}$ Rising Edge
t_7	10	ns min	Minimum $\overline{\text{SYNC}}$ High Time (Stand-Alone Mode)
t_{7MODE2}	400	ns min	Minimum $\overline{\text{SYNC}}$ High Time (Daisy-Chain Mode)
t_{8MODE1}	10	ns min	$\overline{\text{BUSY}}$ Rising Edge to $\overline{\text{SYNC}}$ Falling Edge
t_{9MODE2}	200	ns min	18th SCLK Falling Edge to $\overline{\text{SYNC}}$ Falling Edge (Stand-Alone Mode)
t_{10}	10	ns min	$\overline{\text{SYNC}}$ Rising Edge to SCLK Rising Edge (Daisy-Chain Mode)
t_{11}[4]	20	ns max	SCLK Rising Edge to D_{OUT} Valid (Daisy-Chain Mode)
t_{12}	20	ns min	$\overline{\text{RESET}}$ Pulse Width

NOTES
[1]See Timing Diagrams in Figures 1 and 2.
[2]Guaranteed by design and characterization, not production tested.
[3]All input signals are specified with tr = tf = 5ns (10% to 90% of DV_{CC}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$
[4]This is measured with the load circuit of Figure 3.

SERIAL INTERFACE TIMING DIAGRAMS

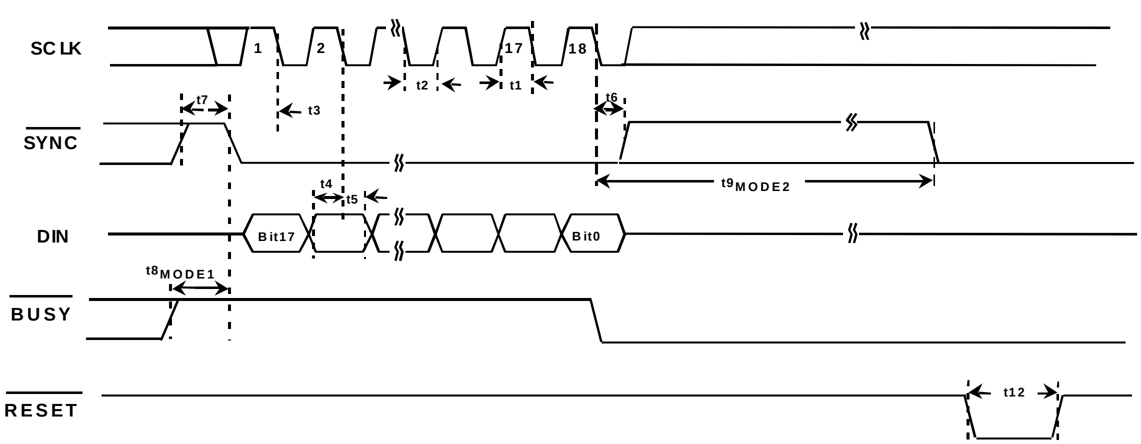


Figure 1. Serial Interface Timing Diagram

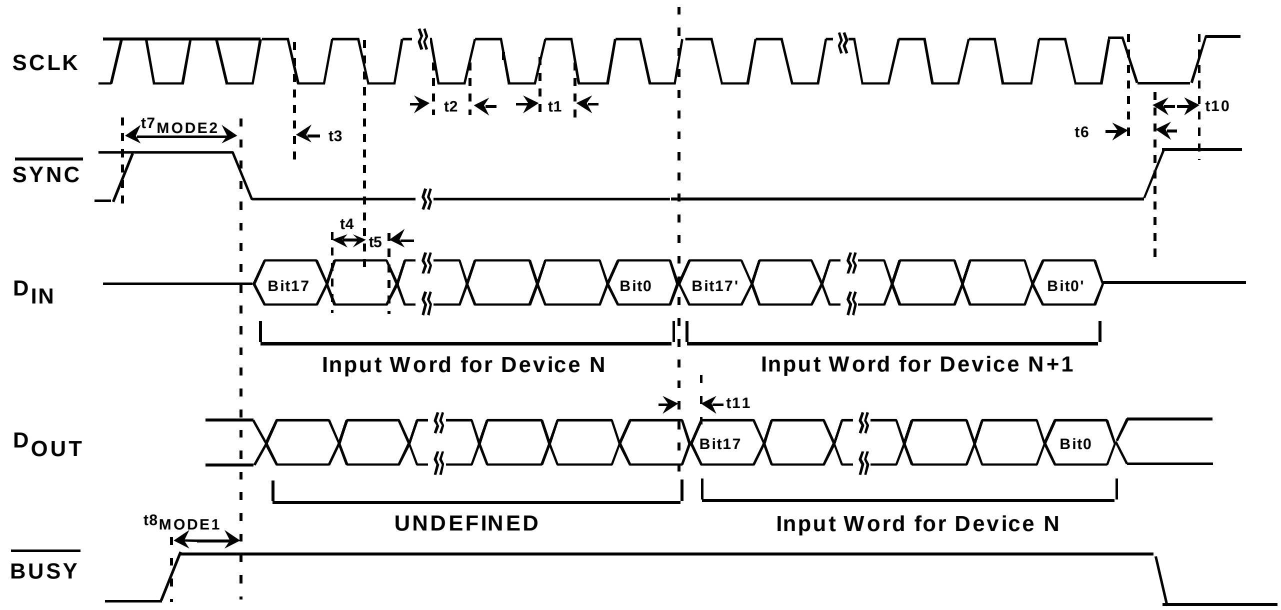


Figure 2. Daisy-Chaining Timing Diagram

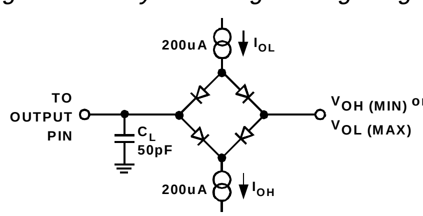


Figure 3. Load Circuit for D_{OUT} Timing Specifications

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND...-0.3 V to +17 V
V_{SS} to AGND...+0.3 V to -17 V
AV_{CC} to AGND, DACGND.............................-0.3 V to +7 V
DV_{CC} to DGND...-0.3 V to +7 V
Digital Inputs to DGND......................-0.3 V to DV_{CC} + 0.3 V
Digital Outputs to DGND...................-0.3 V to DV_{CC} + 0.3 V
REF_IN to AGND, DACGND.........................-0.3 V to +7 V
V_{OUT}0-15 to AGND........................V_{SS} - 0.3 V to V_{DD} + 0.3 V
AGND to DGND..-0.3 V to + 0.3 V

Operating Temperature Range
Industrial ....-40°C to +85°C
Storage Temperature Range......................-65°C to +150°C
Junction Temperature (T_J max).............................+150°C
74-lead LFBGA Package, θ_{JA} Thermal Impedance....41°C/W
Reflow Soldering
Peak Temperature..220°C
Time at Peak Temperature.......................10 sec to 40 sec

NOTES:
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100mA will not cause SCR latch-up

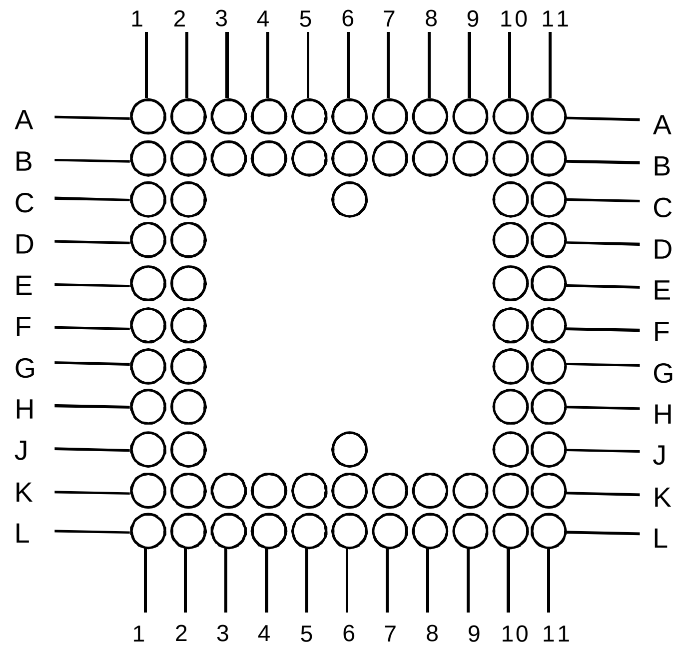
ORDERING GUIDE

Model	Function	Output Voltage Span	Package Option
AD5517ABC-1	16 DACs	±2.5 V	74-lead LFBGA
AD5517ABC-2	16 DACs	±5 V	74-lead LFBGA
AD5517ABC-3	16 DACs	±10 V	74-lead LFBGA

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5517 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



AD5517 74-lead LFBGA Ball Configuration

LFBGA Number	Ball Name	LFBGA Number	Ball Name	LFBGA Number	Ball Name
A1	N/C	C10	AVCC1	J10	RFB12
A2	N/C	C11	N/C	J11	RFB11
A3	$\overline{\text{RESET}}$	D1	RFB0	K1	RFB4
A4	$\overline{\text{BUSY}}$	D2	DACGND	K2	VOUT5
A5	DGND	D10	AVCC2	K3	RFB5
A6	DVCC	D11	N/C	K4	N/C
A7	DOUT	E1	VOUT1	K5	VSS2
A8	DIN	E2	N/C	K6	VSS1
A9	$\overline{\text{SYNC}}$	E10	AGND1	K7	VOUT10
A10	N/C	E11	PD	K8	VOUT9
A11	N/C	F1	VOUT2	K9	RFB10
B1	N/C	F2	RFB1	K10	RFB9
B2	N/C	F10	AGND2	K11	VOUT11
B3	N/C	F11	RFB14	L1	N/C
B4	DCEN	G1	RFB2	L2	VOUT6
B5	DGND	G2	RFB15	L3	RFB6
B6	DGND	G10	VOUT14	L4	VOUT7
B7	N/C	G11	RFB13	L5	N/C
B8	N/C	H1	VOUT3	L6	VDD2
B9	SCLK	H2	VOUT15	L7	VDD1
B10	N/C	H10	VOUT13	L8	RFB7
B11	REF_IN	H11	VOUT12	L9	VOUT8
C1	VOUT0	J1	RFB3	L10	RFB8
C2	DACGND	J2	VOUT4	L11	N/C
C6	N/C	J6	N/C		

PIN FUNCTION DESCRIPTION

Pin	Function
AGND(1-2)	Analog GND pins.
AV_{CC} (1-2)	Analog supply pins. Voltage range from 4.75 V to 5.25 V.
V_{DD} (1-2)	V_{DD} supply pins. Voltage range from 4.75 V to 12 V.
V_{SS} (1-2)	V_{SS} supply pins. Voltage range from -4.75 V to -12 V.
DGND	Digital GND pins.
DV_{CC}	Digital supply pins. Voltage range from 2.7 V to 5.25 V.
DACGND	Reference GND supply for all 16 DACs.
REF_IN	Reference input voltage for all 16 DACs.
V_{OUT} (0-15)	Analog output voltages from the 16 DAC channels.
R_{FB} (0-15)	Feedback Resistors. Access to the inverting inputs of the 16 output amplifiers allows remote sensing in force/sense applications. For nominal output voltage range connect each R_{FB} to it's corresponding V_{OUT}.
$\overline{SYNC}$	Active Low Input. This is the Frame Synchronisation signal for the serial interface. While $\overline{SYNC}$ is low, data is transferred in on the falling edge of SCLK.
SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds up to 20 MHz.
D_{IN}	Serial Data Input. Data must be valid on the falling edge of SCLK.
D_{OUT}	Serial Data Output. D_{OUT} can be used for daisy-chaining a number of devices together or for reading back the data in the shift register for diagnostic purposes. Data is clocked out on D_{OUT} on the rising edge of SCLK and is valid on the falling edge of SCLK.
DCEN[1]	Active High Control Input. This pin is tied high to enable Daisy-Chain Mode.
$\overline{RESET}$[2]	Active Low Control Input. This resets all DAC registers to their mid-scale value.
PD	Active High Control Input. All DACs go into power-down mode when this pin is high. The DAC outputs go into a high-impedance state and the power dissipation drops to TBD.
$\overline{BUSY}$	Active Low Output. This signal tells the user that the analog calibration loop is active. It goes low during conversion. The duration of the pulse on $\overline{BUSY}$ determines the maximum DAC update rate, f_{UPDATE}.

NOTES:
[1]Internal Pull-down device on this logic input. Therfore it can be left floating and will default to a logic low condition.
[2]Internal Pull-up device on this logic input. Therfore it can be left floating and will default to a logic high condition.

TERMINOLOGY

Integral Nonlinearity (INL)
This is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is expressed in LSBs.

Differential Nonlinearity (DNL)
Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified DNL of ±1 LSB maximum ensures monotonicity.

Bipolar Zero Error
Bipolar zero error is the deviation of the DAC output from the ideal midscale of 0 V. It is measured with 10...00 loaded to the DAC. It is expressed in LSBs.

Positive Full-Scale Error
This is the error in the DAC output voltage with all 1s loaded to the DAC. Ideally the DAC output voltage, with all 1s loaded to the DAC registers, should be REF_IN (AD5517-1), 2 REF_IN (AD5517-2) and 4 REF_IN (AD5517-3). It is expressed in LSBs.

Negative Full-Scale Error
This is the error in the DAC output voltage with all 0s loaded to the DAC. Ideally the DAC output voltage, with all 0s loaded to the DAC registers, should be -REF_IN (AD5517-1), -2 REF_IN (AD5517-2) and -4 REF_IN (AD5517-3). It is expressed in LSBs.

Output Temperature Coefficient
This is a measure of the change in analog output with changes in temperature. It is expressed in ppm/°C.

DC Power-Supply Rejection Ratio
DC Power-Supply Rejection Ratio (PSRR) is a measure of the change in analog output for a change in supply voltage (V_{DD} and V_{SS}). It is expressed in dBs. V_{DD} and V_{SS} are varied ± 5%.

DC Crosstalk
This the DC change in the output level of one DAC at mid-scale in response to a full-scale code change (all 0s to all 1s and vice versa) and output change of another DAC. It is expressed in µV.

Output Settling Time
This is the time taken from when the last data bit is clocked into the DAC until the output has settled to within ± 0.5 LSB of it's final value.

Digital-to-Analog Glitch Impulse
This is the area of the glitch injected into the analog output when the code in the DAC register changes state. It is specified as the area of the glitch in nV-secs when the digital code is changed by 1 LSB at the major carry transition (011...11 to 100...00 or 100...00 to 011...11).

Digital Crosstalk
This is the glitch impulse transferred to the output of one DAC at mid-scale while a full-scale code change (all 1s to all 0s and vice versa) is being written to another DAC. It is expressed in nV-secs.

Analog Crosstalk
This the area of the glitch transferred to the output (V_{OUT}) of one DAC due to a full-scale change in the output (V_{OUT}) of another DAC. The area of the glitch is expressed in nV-secs.

Digital Feeedthrough
This is a measure of the impulse injected into the analog outputs from the digital control inputs when the part is not being written to, i.e. $\overline{SYNC}$ is high. It is specified in nV-secs and is measured with a worst-case change on the digital input pins, e.g. from all 0s to all 1s and vice versa.

Output Noise Spectral Density
This is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per root Hertz). It is measured in $nV/(Hz)^{1/2}$.

Typical Performance Characteristics – AD5517-1/AD5517-2/AD5517-3)

TPC 1. Typical DNL plot

TPC 2. Typical INL plot

TPC 3. INL Error and DNL Error vs. Temperature

TPC 4. Bipolar Zero Error and Fullscale Error vs. Temperature

TPC 5. V_{OUT} vs. Temperature

TPC 6. V_{OUT} Source and Sink Capability

TPC 7. Full-Scale Settling Time

TPC 8. Exiting Powerdown to Fullscale

TPC 9. Major Code Transition Glitch Impulse

FUNCTIONAL DESCRIPTION

The AD5517 consists of 16 14-bit DACs in a single package. A single reference input pin (REF_IN) is used to provide a 2.5 V reference for all 16 DACs. To update a DAC's output voltage an 18-bit word is written to the part via the 3-wire serial interface. This 18-bit word consists of 2 mode bits, 4 address bits and 12 data bits as shown in Figure 4. Once the serial write is complete the selected DAC converts the code. The output amplifiers translate the 0 - 2.5 V DAC output range to give a ±5 V range at the output pins $V_{OUT}0$ to $V_{OUT}15$.

SERIAL INTERFACE

DCEN (Daisy-Chain Enable) determines whether the serial interface is in Daisy-Chain Mode or Stand-Alone Mode. In both modes $\overline{\text{SYNC}}$ is an edge-triggered input that acts as a frame synchronization signal and chip enable. Data can only be transferred into the device while $\overline{\text{SYNC}}$ is low. To start the serial data transfer, $\overline{\text{SYNC}}$ should be taken low observing the minimum $\overline{\text{SYNC}}$ falling to SCLK falling edge setup time, t_3.

Stand-Alone Mode (DCEN = 0)

After $\overline{\text{SYNC}}$ goes low, serial data will be shifted into the device's input shift register on the falling edges of SCLK for 18 clock pulses. After the falling edge of the 18th SCLK pulse, data will automatically be transferred from the input shift register to the addressed DAC. $\overline{\text{BUSY}}$ goes low indicating that conversion has started. All SCLK pulses will be ignored while $\overline{\text{BUSY}}$ is low. At the end of a conversion $\overline{\text{BUSY}}$ goes high indicating that the update of the addressed DAC is complete. It is recommended that SCLK is not pulsed while $\overline{\text{BUSY}}$ is low. See the timing diagram in Figure 1.

$\overline{\text{SYNC}}$ must be taken high and low again for further serial data transfer. $\overline{\text{SYNC}}$ may be taken high after the falling edge of the 18th SCLK pulse, observing the minimum SCLK falling edge to $\overline{\text{SYNC}}$ rising edge time, t_6. If $\overline{\text{SYNC}}$ is taken high before the 18th falling edge of SCLK, the data transfer will be aborted and the addressed DAC will not be updated.

Daisy-Chain Mode (DCEN = 1)

In Daisy-Chain Mode the internal gating on SCLK is disabled. The SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 18 clock pulses are applied, the data ripples out of the shift register and appears on the D_{OUT} line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting this line to the D_{IN} input on the next device in the chain, a multi-device interface is constructed. 18 clock pulses are required for each device in the system. Therefore, the total number of clock cycles must equal 18N where N is the total number of devices in the chain. See the timing diagram in Figure 2.

When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ should be taken high. This prevents any further data being clocked into the input shift register. A burst clock containing the exact number of clock cycles may be used and $\overline{\text{SYNC}}$ taken high some time later. After the rising edge of $\overline{\text{SYNC}}$, data is automatically transferred from each device's input shift register to the addressed DAC. $\overline{\text{BUSY}}$ goes low indicating that conversion has started. All SCLK pulses will be ignored while $\overline{\text{BUSY}}$ is low. At the end of a conversion $\overline{\text{BUSY}}$ goes high indicating that the update of the addressed DACs is complete. It is recommended that SCLK is not pulsed while $\overline{\text{BUSY}}$ is low.

MSB ... LSB

0	0	A3	A2	A1	A0	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Mode Bits		Address Bits				Data Bits											

Figure 4. Mode1 data format

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

74-Lead LFBGA
(BC-74)