



# CMOS, Low Voltage 2.5 $\Omega$ Quad SPST Switches

## Preliminary Technical Data

## ADG781/ADG782/ADG783

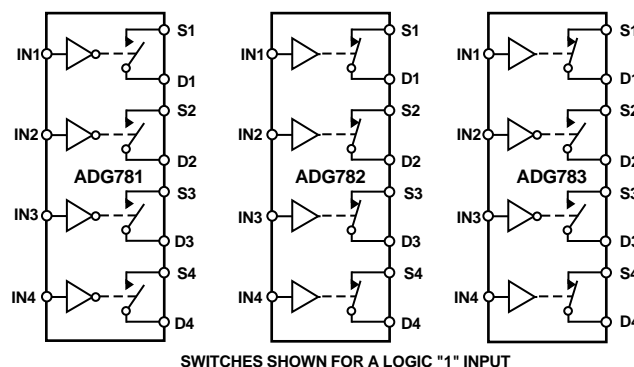
### FEATURES

1.8 V to 5.5 V Single Supply  
Low On-Resistance 2.5  $\Omega$   
On-Resistance Flatness  
-3dB Bandwidth >200MHz  
100 pA Leakage Currents  
14 ns Switching Times  
20-Lead Chip Scale Package  
Low Power Consumption  
TTL/CMOS-Compatible Inputs

### APPLICATIONS

Battery Powered Systems  
Communication Systems  
Sample and Hold Systems  
Audio Signal Routing  
Relay Replacement  
Video Switching

### FUNCTIONAL BLOCK DIAGRAMS



### GENERAL DESCRIPTION

The ADG781, ADG782 and ADG783 are monolithic CMOS devices containing four independently selectable switches. These switches are designed on an advanced submicron process that provides low power dissipation yet gives high switching speed, low on resistance, low leakage currents and high bandwidth.

They are designed to operate from a single +1.8 V to +5.5 V supply, making them ideal for use in battery powered instruments and with the new generation of DACs and ADCs from Analog Devices. Fast switching times and high bandwidth make the part suitable for video signal switching. The ADG781, ADG782 and ADG783 contain four independent single-pole/single throw (SPST) switches. The ADG781 and ADG782 differ only in that the digital control logic is inverted. The ADG781 switches are turned on with a logic low on the appropriate control input, while a logic high is required to turn on the switches of the ADG782. The ADG783 contains two switches whose digital control logic is similar to the ADG781, while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when ON. The ADG783 exhibits break-before-make switching

action. The ADG781/ADG782/ADG783 are available in 20-lead Chip Scale Packages

### PRODUCT HIGHLIGHTS

1. +1.8 V to +5.5 V Single Supply Operation. The ADG781, ADG782 and ADG783 offer high performance and are fully specified and guaranteed with +3V and +5 V supply rails.
2. Very Low  $R_{ON}$  (4.5  $\Omega$  max at +5 V, 8  $\Omega$  max at +3 V). At supply voltage of +1.8 V,  $R_{ON}$  is typically 35  $\Omega$  over the temperature range.
3. Low On-Resistance Flatness.
4. -3 dB Bandwidth >200 MHz.
5. Fast  $t_{ON}/t_{OFF}$ .
6. Break-Before-Make Switching. This prevents channel shorting when the switches are configured as a multiplexer (ADG783 only).

REV. PrB

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# ADG781/ADG782/ADG783—SPECIFICATIONS<sup>1</sup> ( $V_{DD} = 5\text{ V} \pm 10\%$ , GND = 0 V, unless otherwise noted)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 V to V <sub>DD</sub>	V	V <sub>S</sub> = 0 V to V <sub>DD</sub> , I <sub>DS</sub> = 10 mA; Test Circuit 1
On-Resistance (R <sub>ON</sub> )	2.5		Ω typ	
	4	4.5	Ω max	
On-Resistance Match Between Channels (ΔR <sub>ON</sub> )		0.05	Ω typ	V <sub>S</sub> = 0 V to V <sub>DD</sub> , I <sub>DS</sub> = 10 mA V <sub>S</sub> = 0 V to V <sub>DD</sub> , I <sub>DS</sub> = 10 mA
		0.3	Ω max	
On-Resistance Flatness (R <sub>FLAT(ON)</sub> )	0.5		Ω typ	
		1.0	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I <sub>S</sub> (OFF)	±0.01		nA typ	V <sub>DD</sub> = 5.5 V V <sub>D</sub> = 4.5 V/1 V, V <sub>S</sub> = 1 V/4.5 V; Test Circuit 2
	±10	±20	nA max	
Drain OFF Leakage I <sub>D</sub> (OFF)	±0.01		nA typ	V <sub>D</sub> = 4.5 V/1 V, V <sub>S</sub> = 1 V/4.5 V; Test Circuit 2
	±10	±20	nA max	
Channel ON Leakage I <sub>D</sub> , I <sub>S</sub> (ON)	±0.01		nA typ	V <sub>D</sub> = V <sub>S</sub> = 1 V, or 4.5 V, Test Circuit 3
	±10	±20	nA max	
DIGITAL INPUTS				
Input High Voltage, V <sub>INH</sub>		2.4	V min	V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>
Input Low Voltage, V <sub>INL</sub>		0.8	V max	
Input Current				
I <sub>INL</sub> or I <sub>INH</sub>	0.005		μA typ	
		±0.1	μA max	
C <sub>IN</sub> , Digital Input Capacitance	2		pF typ	
DYNAMIC CHARACTERISTICS <sup>2</sup>				
t <sub>ON</sub>	11		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF V <sub>S</sub> = 3 V, Test Circuit 4
		16	ns max	
t <sub>OFF</sub>	6		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF V <sub>S</sub> = 3 V, Test Circuit 4
		10	ns max	
Break-Before-Make Time Delay, t <sub>D</sub>	6		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF V <sub>S1</sub> =V <sub>S2</sub> = 3 V, Test Circuit 5
		1	ns min	
Charge Injection	±3		pC typ	V <sub>S</sub> = 2 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 1 nF; Test Circuit 6
Off Isolation	-58		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 10 MHz R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz; Test Circuit 7
	-78		dB typ	
Channel-to-Channel Crosstalk	-90		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 10 MHz Test Circuit 8
-3 dB Bandwidth	200		MHz typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, Test Circuit 9
C <sub>S</sub> (OFF)	10		pF typ	
C <sub>D</sub> (OFF)	10		pF typ	
C <sub>D</sub> , C <sub>S</sub> (ON)	22		pF typ	
POWER REQUIREMENTS				
I <sub>DD</sub>	0.001		μA typ	V <sub>DD</sub> = 5.5 V Digital Inputs = 0 V or 5.5 V
		1.0	μA max	

**NOTES**<sup>1</sup>Temperature range is as follows: B Version: -40°C to +85°C.<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS<sup>1</sup>(V<sub>DD</sub> = 3 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version		Unit	Test Conditions/Comments
	+258C	-40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 V to V <sub>DD</sub>	V	
On-Resistance (R <sub>ON</sub> )	5	5.5	Ω typ	V <sub>S</sub> = 0 V to V <sub>DD</sub> , I <sub>DS</sub> = 10 mA; Test Circuit 1
		8	Ω max	
On-Resistance Match Between Channels (ΔR <sub>ON</sub> )	0.1		Ω typ	V <sub>S</sub> = 0 V to V <sub>DD</sub> , I <sub>DS</sub> = 10 mA
		0.3	Ω max	
On-Resistance Flatness (R <sub>FLAT(ON)</sub> )		2.5	Ω typ	V <sub>S</sub> = 0 V to V <sub>DD</sub> , I <sub>DS</sub> = 10 mA
LEAKAGE CURRENTS				
Source OFF Leakage I <sub>S</sub> (OFF)	±0.01		nA typ	V <sub>DD</sub> = 3.3 V
	±10	±20	nA max	V <sub>S</sub> = 3 V/1 V, V <sub>D</sub> = 1 V/3 V; Test Circuit 2
Drain OFF Leakage I <sub>D</sub> (OFF)	±0.01		nA typ	V <sub>S</sub> = 3 V/1 V, V <sub>D</sub> = 1 V/3 V;
	±10	±20	nA max	Test Circuit 2
Channel ON Leakage I <sub>D</sub> , I <sub>S</sub> (ON)	±0.01		nA typ	V <sub>S</sub> = V <sub>D</sub> = 1 V or 3 V, Test Circuit 3
	±10	±20	nA max	
DIGITAL INPUTS				
Input High Voltage, V <sub>INH</sub>		2.0	V min	
Input Low Voltage, V <sub>INL</sub>		0.4	V max	
Input Current				
I <sub>INL</sub> or I <sub>INH</sub>	0.005		μA typ	V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>
		±0.1	μA max	
C <sub>IN</sub> , Digital Input Capacitance	2		pF typ	
DYNAMIC CHARACTERISTICS <sup>2</sup>				
t <sub>ON</sub>	13		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF
		20	ns max	V <sub>S</sub> = 2 V, Test Circuit 4
t <sub>OFF</sub>	7		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF
		12	ns max	V <sub>S</sub> = 2 V, Test Circuit 4
Break-Before-Make Time Delay, t <sub>D</sub>	7		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF
		1	ns min	V <sub>S1</sub> =V <sub>S2</sub> = 2 V, Test Circuit 5
Charge Injection	±3		pC typ	V <sub>S</sub> = 1.5 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 1 nF; Test Circuit 6
Off Isolation	-58		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 10 MHz
	-78		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	-90		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 10 MHz Test Circuit 8
-3 dB Bandwidth	200		MHz typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, Test Circuit 9
C <sub>S</sub> (OFF)	10		pF typ	
C <sub>D</sub> (OFF)	10		pF typ	
C <sub>D</sub> , C <sub>S</sub> (ON)	22		pF typ	
POWER REQUIREMENTS				
I <sub>DD</sub>	0.001		μA typ	V <sub>DD</sub> = 3.3 V
		1.0	μA max	Digital Inputs = 0 V or 3.3 V

## NOTES

<sup>1</sup>Temperature ranges are as follows: B Version: -40°C to +85°C.<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

## ADG781/ADG782/ADG783

ABSOLUTE MAXIMUM RATINGS<sup>1</sup>(T<sub>A</sub> = 25°C unless otherwise noted)

V <sub>DD</sub> to GND	-0.3 V to +6 V
Analog Inputs <sup>2</sup>	V <sub>SS</sub> - 0.3 V to V <sub>DD</sub> + 0.3 V or 30 mA, Whichever Occurs First
Digital Inputs <sup>2</sup>	-0.3 V to V <sub>DD</sub> + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D	30 mA
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
CSP Package, Power Dissipation	TBD mW
θ <sub>JA</sub> Thermal Impedance	TBD°C/W

θ <sub>JC</sub> Thermal Impedance	TBD°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

## NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

<sup>2</sup>Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG781/ADG782/ADG783 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG781BCP	-40°C to +85°C	Chip Scale Package (CSP)	CP-20
ADG782BCP	-40°C to +85°C	Chip Scale Package (CSP)	CP-20
ADG783BCP	-40°C to +85°C	Chip Scale Package (CSP)	CP-20

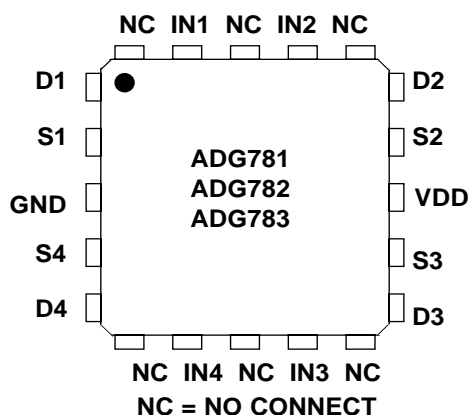
Table I. ADG781/ADG782 Truth Table

ADG781 In	ADG782 In	Switch Condition
0	1	ON
1	0	OFF

Table II. ADG783 Truth Table

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

## PIN CONFIGURATIONS



Exposed Pad tied to Substrate, GND

## TERMINOLOGY

$V_{DD}$	Most positive power supply potential.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
$R_{ON}$	Ohmic resistance between D and S.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
$\Delta R_{ON}$	On resistance match between any two channels, i.e. $R_{ONmax} - R_{ONmin}$ .
$I_S$ (OFF)	Source leakage current with the switch "OFF."
$I_D$ (OFF)	Drain leakage current with the switch "OFF."
$I_D, I_S$ (ON)	Channel leakage current with the switch "ON."
$V_D$ ( $V_S$ )	Analog voltage on terminals D, S.
$C_S$ (OFF)	"OFF" switch source capacitance. Measured with reference to ground.
$C_D$ (OFF)	"OFF" switch drain capacitance. Measured with reference to ground.
$C_D, C_S$ (ON)	"ON" switch capacitance. Measured with reference to ground.
$C_{IN}$	Digital Input Capacitance.
$t_{ON}$	Delay time between applying the digital control input and the switch turning on.
$t_{OFF}$	Delay time between applying the digital control input and the switch turning off.
$t_D$	"OFF" time measured between the 90% points of both switches when switching from one address state to another (ADG783 only).
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Bandwidth	The frequency at which the output is attenuated by 3 dBs.
On Response	The frequency response of the "ON" switch.
On Loss	The loss due to the ON resistance of the switch.
$V_{INL}$	Maximum input voltage for Logic "0."
$V_{INH}$	Minimum input voltage for Logic "1."
$I_{INL}$ ( $I_{INH}$ )	Input current of the digital input.
$I_{DD}$	Positive Supply Current.

## ADG781/ADG782/ADG783 Typical Performance Characteristics–

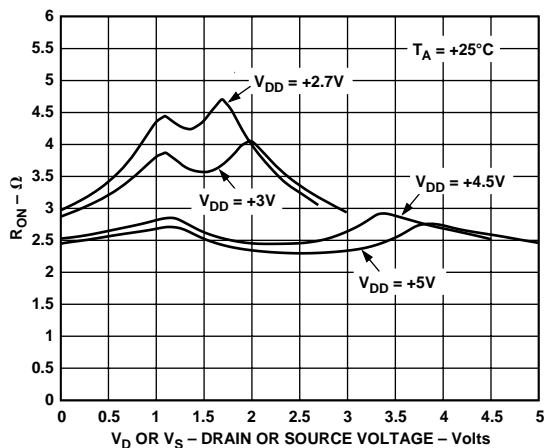


Figure 1. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Single Supply

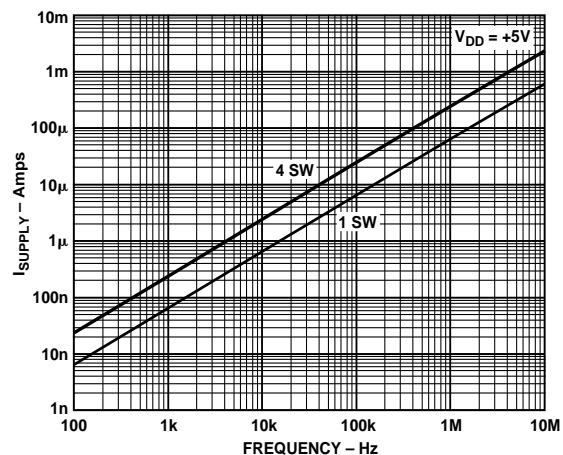


Figure 4. Supply Current vs. Input Switching Frequency

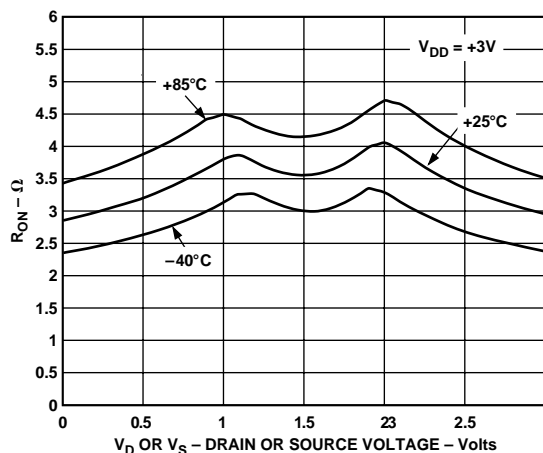


Figure 2. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures,  $V_{DD} = 3$  V.

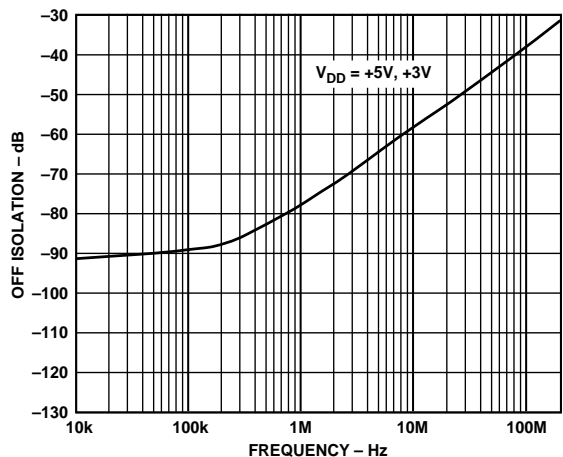


Figure 5. Off Isolation vs. Frequency

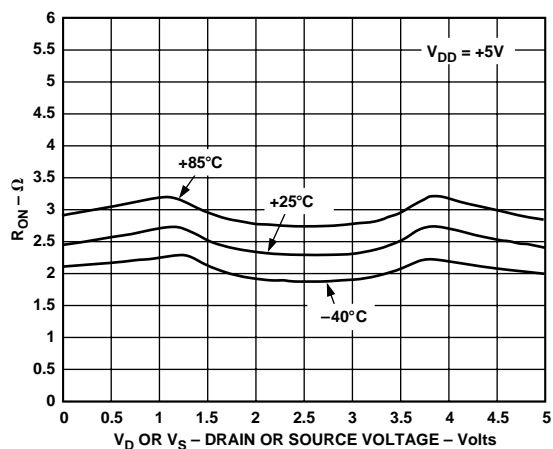


Figure 3. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures,  $V_{DD} = 5$  V.

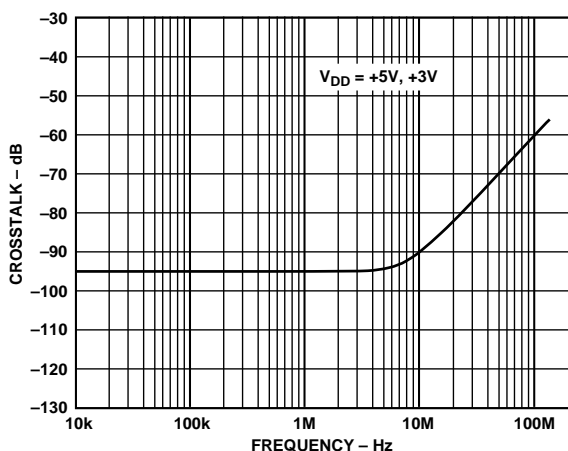


Figure 6. Crosstalk vs. Frequency

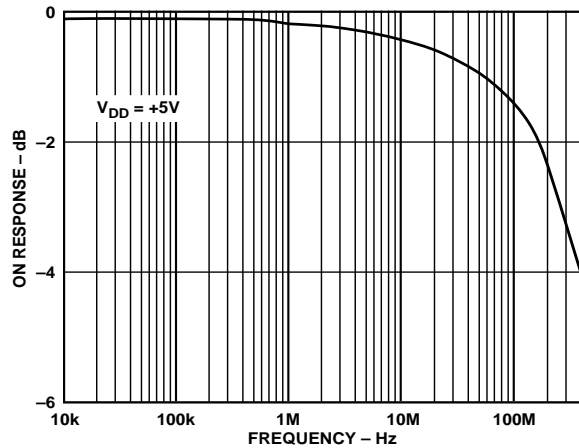


Figure 7. On Response vs. Frequency

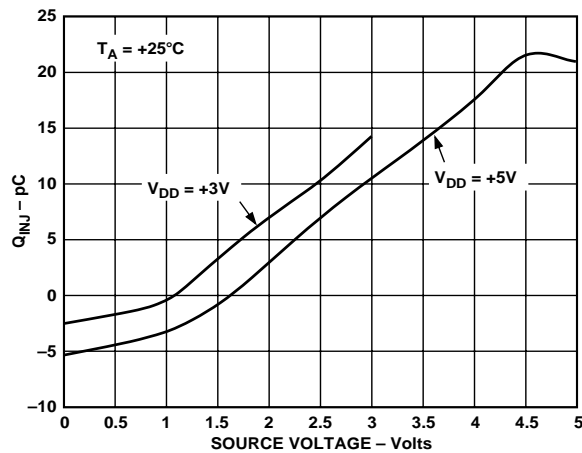


Figure 8. Charge Injection vs. Source Voltage

### APPLICATIONS

Figure 9 illustrates a photodetector circuit with programmable gain. With the resistor values shown in the circuit and using different combinations of switches, gains in the range of 2 to 16 can be achieved.

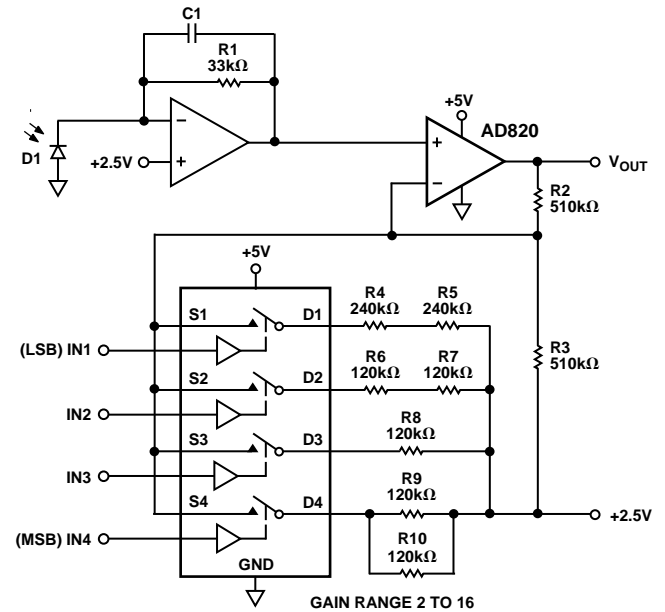
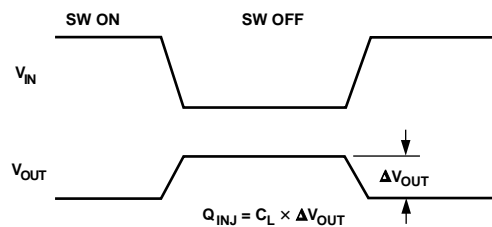
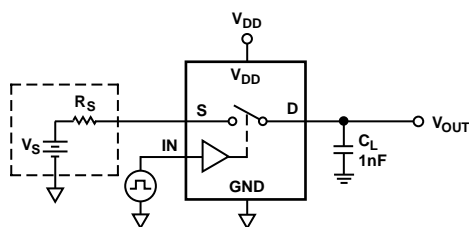
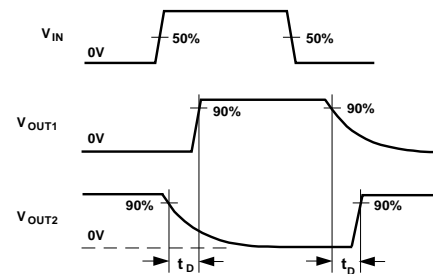
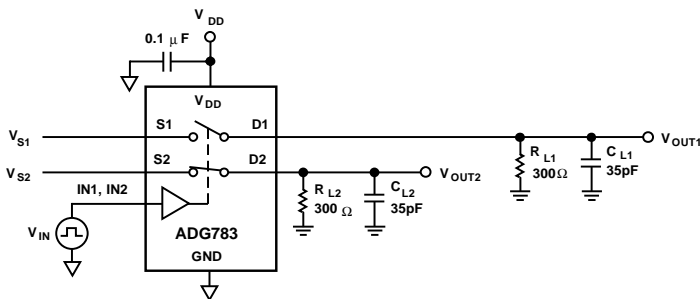
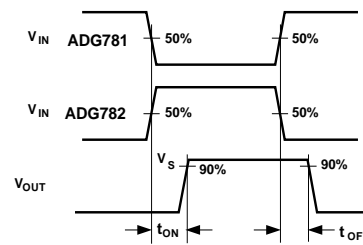
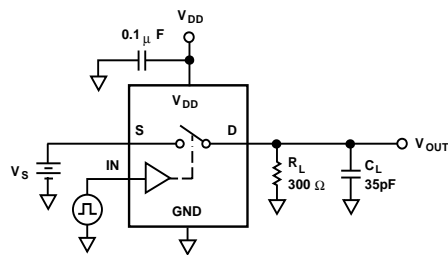
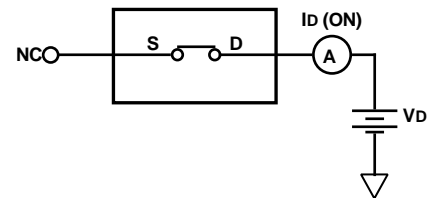
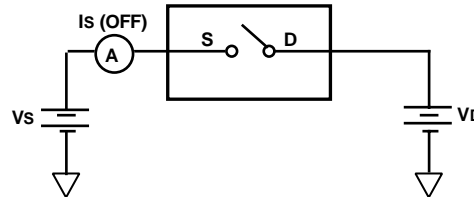
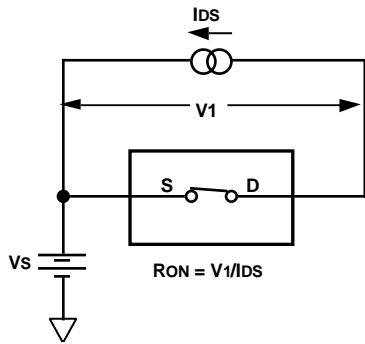


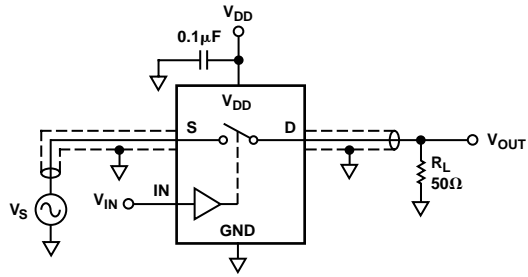
Figure 9. Photodetector Circuit with Programmable Gain

## ADG781/ADG782/ADG783

### Test Circuits







Test Circuit 7. OFF Isolation

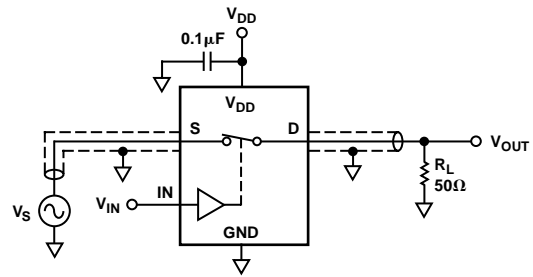
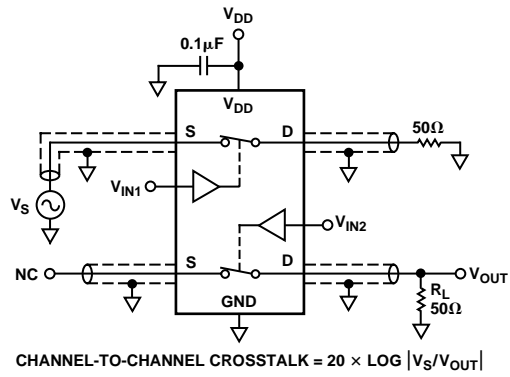


Figure 9. Bandwidth



Test Circuit 8. Channel-to-Channel Crosstalk

# PRELIMINARY TECHNICAL DATA

## ADG781/ADG782/ADG783

### OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

#### 20-Lead Chip Scale (CP-20)

