ANALOG DEVICES

DSP Microcomputer

Preliminary Technical Data ADSP-2188N

PERFORMANCE FEATURES
- 12.5 ns Instruction Cycle Time @1.8 V (Internal), 80 MIPS Sustained Performance
- Single-Cycle Instruction Execution
- Single-Cycle Context Switch
- 3-Bus Architecture Allows Dual Operand Fetches in Every Instruction Cycle
- Multifunction Instructions
- Power-Down Mode Featuring Low CMOS Standby Power Dissipation with 200 CLKIN Cycle Recovery from Power-Down Condition
- Low Power Dissipation in Idle Mode

INTEGRATION FEATURES
- ADSP-2100 Family Code Compatible (Easy to Use Algebraic Syntax), with Instruction Set Extensions
- 256K Bytes of On-Chip RAM, Configured as
  48K Words Program Memory RAM
  56K Words Data Memory RAM
- Dual-Purpose Program Memory for Both Instruction and Data Storage
- Independent ALU, Multiplier/Accumulator, and Barrel Shifter Computational Units
- Two Independent Data Address Generators
- Powerful Program Sequencer Provides Zero Overhead Looping Conditional Instruction Execution
- Programmable 16-Bit Interval Timer with Prescaler
- 100-Lead LQFP and 144-Ball Mini-BGA

SYSTEM INTERFACE FEATURES
- Flexible I/O Allows 1.8 V, 2.5 V or 3.3 V Operation All Inputs Tolerate up to 3.6 V Regardless of Mode
- 16-Bit Internal DMA Port for High-Speed Access to On-Chip Memory (Mode Selectable)
- 4-MByte Memory Interface for Storage of Data Tables and Program Overlays (Mode Selectable)
- 8-Bit DMA to Byte Memory for Transparent Program and Data Memory Transfers (Mode Selectable)
- I/O Memory Interface with 2048 Locations Supports Parallel Peripherals (Mode Selectable)
- Programmable Memory Strobe and Separate I/O Memory Space Permits "Glueless" System Design
- Programmable Wait State Generation
- Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering
- Automatic Booting of On-Chip Program Memory from Byte-Wide External Memory,e.g.,EPROM,or through Internal DMA Port
- Six External Interrupts
- 13 Programmable Flag Pins Provide Flexible System Signaling
- UART Emulation through Software SPORT Reconfiguration
- ICE-Port™ Emulator Interface Supports Debugging in Final Systems[1]

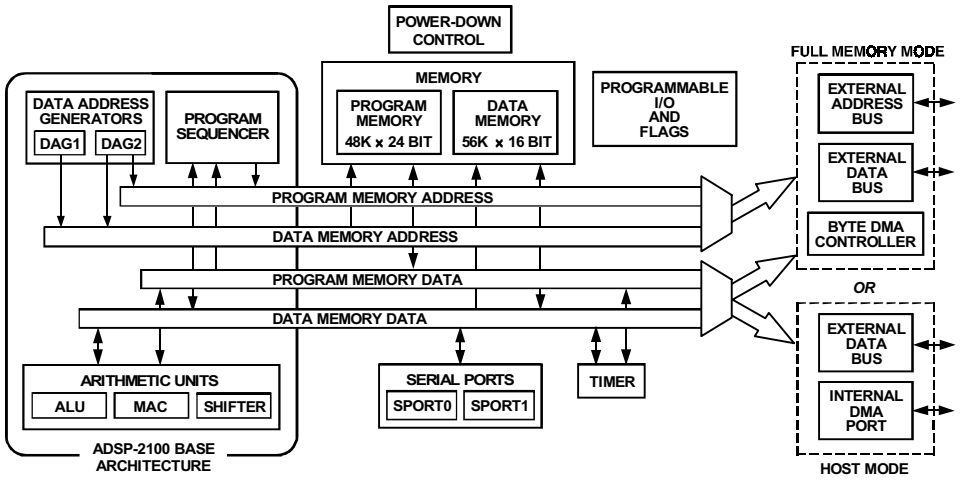

Figure 1. Functional Block Diagram

[1]ICE-Port is a trademark of Analog Devices, Inc.

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GENERAL DESCRIPTION

The ADSP-2188N is a single-chip microcomputer optimized for digital signal processing (DSP) and other high-speed numeric processing applications.

The ADSP-2188N combines the ADSP-2100 family base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities, and on-chip program and data memory.

The ADSP-2188N integrates 256K bytes of on-chip memory configured as 48K words (24-bit) of program RAM, and 56K words (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery-operated portable equipment. The ADSP-2188N is available in a 100-lead LQFP package and 144-Ball Mini-BGA.

In addition, the ADSP-2188N supports new instructions, which include bit manipulations—bit set, bit clear, bit toggle, bit test—new ALU constants, new multiplication instruction (x^2[squared]), biased rounding, result-free ALU operations, I/O memory transfers, and global interrupt masking, for increased flexibility.

Fabricated in a high-speed, low-power, CMOS process, the ADSP-2188N operates with a 12.5 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-2188N's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle, the ADSP-2188N can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This takes place while the processor continues to:

- Receive and transmit data through the two serial ports
- Receive and/or transmit data through the internal DMA port
- Receive and/or transmit data through the byte DMA port
- Decrement timer

DEVELOPMENT SYSTEM

Analog Devices' wide range of software and hardware development tools supports the ADSP-218x N Series. The DSP tools include an integrated development environment, an evaluation kit, and a serial port emulator.

VisualDSP* is an integrated development environment, allowing for fast and easy development, debug and deployment. The VisualDSP project management environment lets programmers develop and debug an application. This environment includes an easy-to-use assembler that is based on an algebraic syntax; an archiver (librarian/library builder); a linker; a loader; a cycle-accurate, instruction-level simulator; a C compiler; and a C run-time library that includes DSP and mathematical functions.

Debugging both C and assembly programs with the VisualDSP debugger, programmers can:

- View mixed C and assembly code (interleaved source and object information)
- Insert break points
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- Fill and dump memory
- Source level debugging

The VisualDSP IDE lets programmers define and manage DSP software development. The dialog boxes and property pages let programmers configure and manage all of the ADSP-218x development tools, including the syntaxhighlighting in the VisualDSP editor. This capability controls how the development tools process inputs and generate outputs.

The ADSP-2189M EZ-KIT Lite(tm) provides developers with a cost-effective method for initial evaluation of the powerful ADSP-218x DSP family architecture. The ADSP-2189M EZ-KIT Lite includes a stand-alone ADSP-2189M DSP board and fundamental code generation debug software. With this EZ-KIT Lite, users can learn about DSP hardware and software development and evaluate potential applications of the ADSP-218x N series. The ADSP-2189M EZ-KIT Lite provides an evaluation suite of the VisualDSP development environment with the C compiler, assembler, and linker. All software tools are limited to use with the EZ-KIT Lite product.

The EZ-KIT Lite includes the following features:

- 75 MHz ADSP-2189M
- Full 16-Bit Stereo Audio I/O with AD73322 Codec
- RS-232 Interface
- EZ-ICE Connector for Emulator Control
- DSP Demonstration Programs
- Evaluation Suite of VisualDSP

The ADSP-218x EZ-ICE ® Emulator provides an easier and more cost-effectivemethod for engineers to develop and optimize DSP systems, shortening product development cycles for faster time-to-market. The ADSP-2188N integrates on-chip emulation support with a 14-pin ICE-Port interface. This interface provides a simpler target board connection that requires fewer mechanical clearance considerations than other ADSP-2100 Family EZ-ICEs. The ADSP-2188N device need not be removed from the target

system when using the EZ-ICE, nor are any adapters needed. Due to the small footprint of the EZ-ICE connector, emulation can be supported in final board designs.The EZ-ICE performs a full range of functions, including:

- In-target operation
- Up to 20 breakpoints
- Single-step or full-speed operation
- Registers and memory values can be examined and altered
- PC upload and download functions
- Instruction-level emulation of program booting and execution
- Complete assembly and disassembly of instructions
- C source-level debugging

Additional Information

This data sheet provides a general overview of ADSP-2188N functionality. For additional information on the architecture and instruction set of the processor, refer to the ADSP-218x DSP Hardware Reference.

ARCHITECTURE OVERVIEW

The ADSP-2188N instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-2188N assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Figure 1 on page 1 is an overall block diagram of the ADSP-2188N. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations.

The shifter can be used to efficiently implement numeric format control, including multiword and block floating-point representations.

The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2188N executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAG) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting the ADSP-2188N to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-2188N can fetch an operand from program memory and the next instruction in the same cycle.

In lieu of the address and data bus for external memory connection, the ADSP-2188N may be configured for 16-bit Internal DMA port (IDMA port) connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSP's on-chip program and data RAM.

An interface to low-cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$, and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-2188N to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

The ADSP-2188N can respond to eleven interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports

(SPORT), the Byte DMA port, and the power-down circuitry. There is also a master $\overline{\text{RESET}}$ signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

Each port can generate an internal programmable serial clock or accept an external serial clock.

The ADSP-2188N provides up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, eight flags are programmable as inputs or outputs, and three flags are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) decrements every n processor cycle, where n is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

The ADSP-2188N incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the ADSP-2188N SPORTs. For additional information on Serial Ports, refer to the *ADSP-218x DSP Hardware Reference*.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulse widths and timings.
- SPORTs support serial data word lengths from 3 to 16 bits and provide optional A-law and μ-law companding, according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 or 32 word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts ($\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$) and the FI and FO signals. The internally generated serial clock may still be used in this configuration.

PIN DESCRIPTIONS

The ADSP-2188N is available in a 100-lead LQFP package and a 144-Ball Mini-BGA package. In order to maintain maximum functionality and reduce package size and pin count, some serial port, programmable flag, interrupt and external bus pins have dual, multiplexed functionality. The external bus pins are configured during $\overline{\text{RESET}}$ only, while serial port pins are software configurable during program execution. Flag and interrupt functionality is retained concurrently on multiplexed pins. In cases where pin functionality is reconfigurable, the default state is shown in plain text in Table 1; alternate functionality is shown in *italics*.

Table 1. Common-Mode Pins

Pin Name	# of Pins	I/O	Function
$\overline{\text{RESET}}$	1	I	Processor Reset Input
$\overline{\text{BR}}$	1	I	Bus Request Input
$\overline{\text{BG}}$	1	O	Bus Grant Output
$\overline{\text{BGH}}$	1	O	Bus Grant Hung Output
$\overline{\text{DMS}}$	1	O	Data Memory Select Output
$\overline{\text{PMS}}$	1	O	Program Memory Select Output
$\overline{\text{IOMS}}$	1	O	Memory Select Output
$\overline{\text{BMS}}$	1	O	Byte Memory Select Output
$\overline{\text{CMS}}$	1	O	Combined Memory Select Output

Table 1. Common-Mode Pins (Continued)

Pin Name	# of Pins	I/O	Function
$\overline{RD}$	1	O	Memory Read Enable Output
$\overline{WR}$	1	O	Memory Write Enable Output
$\overline{IRQ2}$	1	I	Edge- or Level-Sensitive Interrupt Request[1]
PF7		I/O	Programmable I/O pin
$\overline{IRQL1}$	1	I	Level-Sensitive Interrupt Requests[1]
PF6		I/O	Programmable I/O Pin
$\overline{IRQL0}$	1	I	Level-Sensitive Interrupt Requests[1]
PF5		I/O	Programmable I/O Pin
$\overline{IRQE}$	1	I	Edge-Sensitive Interrupt Requests[1]
PF4		I/O	Programmable I/O Pin
Mode D	1	I	Mode Select Input—Checked Only During $\overline{RESET}$
PF3		I/O	Programmable I/O Pin During Normal Operation
Mode C	1	I	Mode Select Input—Checked Only During $\overline{RESET}$
PF2		I/O	Programmable I/O Pin During Normal Operation
Mode B	1	I	Mode Select Input—Checked Only During $\overline{RESET}$
PF1		I/O	Programmable I/O Pin During Normal Operation
Mode A	1	I	Mode Select Input—Checked Only During $\overline{RESET}$
PF0		I/O	Programmable I/O Pin During Normal Operation
CLKIN, XTAL	2	I	Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output
SPORT0	5	I/O	Serial Port I/O Pins
SPORT1	5	I/O	Serial Port I/O Pins
$\overline{IRQ1:0}$, FI, FO			Edge- or Level-Sensitive Interrupts, FI, FO[2]
$\overline{PWD}$	1	I	Power-Down Control Input
PWDACK	1	O	Power-Down Control Output
FL0, FL1, FL2	3	O	Output Flags
V_{DDINT}	2	I	Internal V_{DD} (1.8 V) Power (LQFP)
V_{DDEXT}	4	I	External V_{DD} (1.8 V, 2.5 V or 3.3 V) Power (LQFP)
GND	10	I	Ground (LQFP)
V_{DDINT}	4	I	Internal V_{DD} (1.8 V) Power (Mini-BGA)

Table 1. Common-Mode Pins (Continued)

Pin Name	# of Pins	I/O	Function
V_{DDEXT}	7	I	External V_{DD} (1.8 V, 2.5 V or 3.3 V) Power (Mini-BGA)
GND	20	I	Ground (Mini-BGA)
EZ-Port	9	I/O	For Emulation Use

[1]Interrupt/Flag pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices or set as a programmable flag.

[2]SPORT configuration determined by the DSP System Control Register. Software configurable.

Memory Interface Pins

The ADSP-2188N processor can be used in one of two modes: Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities.

The operating mode is determined by the state of the Mode C pin during $\overline{\text{RESET}}$ and cannot be changed while the processor is running. Table 2 and Table 3 list the active signals at specific pins of the DSP during either of the two operating modes (Full Memory or Host). A signal in one table shares a pin with a signal from the other table, with the active signal determined by the mode that is set. For the shared pins and their alternate signals (e.g., A4/IAD3), refer to the package pinouts in Table 26 on page 41 and Table 27 on page 43.

Table 2. Full Memory Mode Pins (Mode C = 0)

Pin Name	# of Pins	I/O	Function
A13:0	14	O	Address Output Pins for Program, Data, Byte, and I/O Spaces
D23:0	24	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces (8 MSBs are also used as Byte Memory Addresses.)

Table 3. Host Mode Pins (Mode C = 1)

Pin Name	# of Pins	I/O	Function
IAD15:0	16	I/O	IDMA Port Address/Data Bus
A0	1	O	Address Pin for External I/O, Program, Data, or Byte Access[1]
D23:8	16	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces
$\overline{\text{IWR}}$	1	I	IDMA Write Enable
$\overline{\text{IRD}}$	1	I	IDMA Read Enable
IAL	1	I	IDMA Address Latch Pin
$\overline{\text{IS}}$	1	I	IDMA Select
$\overline{\text{IACK}}$	1	O	IDMA Port Acknowledge Configurable in Mode D; Open Drain

[1]In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{\text{CMS}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{IOMS}}$ signals.

Terminating Unused Pins

Table 4 shows the recommendations for terminating unused pins.

Table 4. Unused Pin Terminations

Pin Name[1]	I/O 3-State (Z)[2]	Reset State	Hi-Z[3] Caused By	Unused Configuration
XTAL	I	I		Float
CLKOUT	O	O		Float[4]
A13:1 or	O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
IAD 12:0	I/O (Z)	Hi-Z	$\overline{IS}$	Float
A0	O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
D23:8	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
D7 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IWR}$	I	I		High (Inactive)
D6 or	I/O (Z)	Hi-z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IRD}$	I	I	$\overline{BR}$, $\overline{EBR}$	High (Inactive)
D5 or	I/O (Z)	Hi-Z		Float
IAL	I	I		Low (Inactive)
D4 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IS}$	I	I		High (Inactive)
D3 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IACK}$				Float
D2:0 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float---Float
IAD15:13	I/O (Z)	Hi-Z	$\overline{IS}$	Float
$\overline{PMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{DMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IOMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{CMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{RD}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{WR}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BR}$	I	I		High (Inactive)
$\overline{BG}$	O (Z)	O	EE	Float

Table 4. Unused Pin Terminations (Continued)

Pin Name[1]	I/O 3-State (Z)[2]	Reset State	Hi-Z[3] Caused By	Unused Configuration
$\overline{\text{BGH}}$	O	O		Float
$\overline{\text{IRQ2}}$/*PF7*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float[5]
$\overline{\text{IRQL1}}$/*PF6*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float[5]
$\overline{\text{IRQL0}}$/*PF5*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float[5]
$\overline{\text{IRQE}}$/*PF4*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float[5]
SCLK0	I/O	I		Input = High or Low, Output = Float
RFS0	I/O	I		High or Low
DR0	I	I		High or Low
TFS0	I/O	I		High or Low
DT0	O	O		Float
SCLK1	I/O	I		Input = High or Low, Output = Float
RFS1/$\overline{\text{IRQ0}}$	I/O	I		High or Low
DR1/FI	I	I		High or Low
TFS1/$\overline{\text{IRQ1}}$	I/O	I		High or Low
DT1/FO	O	O		Float
EE	I	I		Float
$\overline{\text{EBR}}$	I	I		Float
$\overline{\text{EBG}}$	O	O		Float
$\overline{\text{ERESET}}$	I	I		Float
$\overline{\text{EMS}}$	O	O		Float
$\overline{\text{EINT}}$	I	I		Float
ECLK	I	I		Float
ELIN	I	I		Float
ELOUT	O	O		Float

[1]CLKIN, $\overline{\text{RESET}}$, and PF3:0/Mode D:A are not included in Table 4 because these pins must be used.

[2]All bidirectional pins have three-stated outputs. When the pin is configured as an output, the output is Hi-Z (high impedance) when inactive.

[3]Hi-Z = High Impedance.

[4]If the CLKOUT pin is not used, turn it OFF, using CLKODIS in SPORT0 autobuffer control register.

[5]If the Interrupt/Programmable Flag pins are not used, there are two options: Option 1: When these pins are configured as INPUTS at reset and function as interrupts and input flag pins, pull the pins High (inactive). Option 2: Program the unused pins as OUTPUTS, set them to 1 prior to enabling interrupts, and let pins float.

Interrupts

The interrupt controller allows the processor to respond to the 11 possible interrupts and reset with minimum overhead. The ADSP-2188N provides four dedicated external interrupt input pins: $\overline{\text{IRQ2}}$, $\overline{\text{IRQL0}}$, $\overline{\text{IRQL1}}$, and $\overline{\text{IRQE}}$ (shared with the PF7:4 pins). In addition, SPORT1 may be reconfigured for $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, FI and FO, for a total of six external interrupts. The ADSP-2188N also supports internal interrupts from the timer, the byte DMA port, the two serial ports, software, and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power-down and reset). The $\overline{\text{IRQ2}}$, $\overline{\text{IRQ0}}$, and $\overline{\text{IRQ1}}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ are level-sensitive and $\overline{\text{IRQE}}$ is edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table 5.

Table 5. Interrupt Priority and Interrupt Vector Addresses

Source Of Interrupt	Interrupt Vector Address (Hex)
Reset (or Power-Up with PUCR = 1)	0x0000 (Highest Priority)
Power-Down (Nonmaskable)	0x002C
$\overline{\text{IRQ2}}$	0x0004
$\overline{\text{IRQL1}}$	0x0008
$\overline{\text{IRQL0}}$	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
$\overline{\text{IRQE}}$	0x0018
BDMA Interrupt	0x001C
SPORT1 Transmit or $\overline{\text{IRQ1}}$	0x0020
SPORT1 Receive or $\overline{\text{IRQ0}}$	0x0024
Timer	0x0028 (Lowest Priority)

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

The ADSP-2188N masks all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ external interrupts to be either edge- or level-sensitive. The $\overline{\text{IRQE}}$ pin is an external edge-sensitive interrupt and can be forced and cleared. The $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ pins are external level sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are twelve levels deep to allow interrupt, loop, and subroutine nesting. The following instructions allow global enable or disable servicing of the interrupts (including power-down), regardless of the state of IMASK. Disabling the interrupts does not affect serial port autobuffering or DMA.

```
ENA INTS;
DIS INTS;
```

When the processor is reset, interrupt servicing is enabled.

LOW-POWER OPERATION

The ADSP-2188N has three low-power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

The ADSP-2188N processor has a low-power feature that lets the processor enter a very low-power dormant state through hardware or software control. Following is a brief list of power-down features. Refer to the ADSP-218x DSP Hardware Reference, “System Interface” chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 200 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 200 CLKIN cycle recovery.

- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits approximately 4096 CLKIN cycles for the crystal oscillator to start or stabilize), and letting the oscillator run to allow 200 CLKIN cycle start-up.
- Power-down is initiated by either the power-down pin ($\overline{\text{PWD}}$) or the software power-down force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate power-down.
- Power-down acknowledge pin indicates when the processor has entered power-down.

Idle

When the ADSP-2188N is in the Idle Mode, the processor waits indefinitely in a low-power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle mode IDMA, BDMA and autobuffer cycle steals still occur.

Slow Idle

The IDLE instruction is enhanced on the ADSP-2188N to let the processor's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction.

The format of the instruction is:

```
IDLE (N);
```

where n = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT, and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the IDLE (n) instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by n, the clock divisor. When an enabled interrupt is received, the ADSP-2188N will remain in the idle state for up to a maximum of n processor cycles (n = 16, 32, 64, or 128) before resuming normal operation.

When the IDLE (n) instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of n processor cycles).

SYSTEM INTERFACE

Figure 2 shows typical basic system configurations with the ADSP-2188N, two serial devices, a byte-wide EPROM, and optional external program and data overlay memories (mode-selectable). Programmable wait state generation allows the processor to connect easily to slow peripheral devices. The ADSP-2188N also provides four external interrupts and two serial ports or six external interrupts and one serial port. Host Memory Mode allows access to the full external data bus, but limits addressing to a single address bit (A0). Through the use of external hardware, additional system peripherals can be added in this mode to generate and latch address signals.

Clock Signals

The ADSP-2188N can be clocked by either a crystal or a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation, nor operated below the specified frequency during normal operation. The only exception is while the processor is in the power-down state. For additional information, refer to the ADSP-218x DSP Hardware Reference, for detailed information on this power-down feature.

If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input must be left unconnected.

The ADSP-2188N uses an input clock with a frequency equal to half the instruction rate; a 40 MHz input clock yields a 12.5 ns processor cycle (which is equivalent to 80 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because the ADSP-2188N includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 3. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 Autobuffer Control Register.

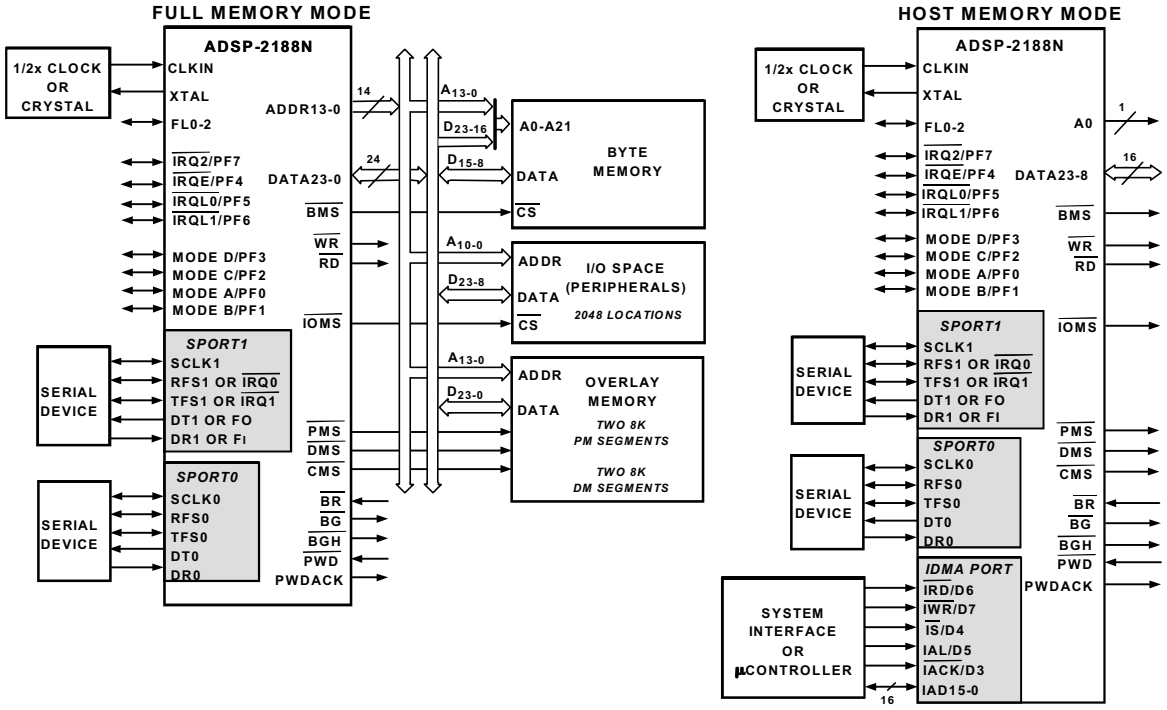


Figure 2. Basic System Interface

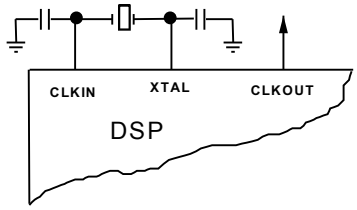


Figure 3. External Crystal Connections

RESET

The $\overline{\text{RESET}}$ signal initiates a master reset of the ADSP-2188N. The $\overline{\text{RESET}}$ signal must be asserted during the power-up sequence to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked but does not include the crystal oscillator start-up time. During this power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse-width specification, t_{RSP}.

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if an RC circuit is used to generate the $\overline{\text{RESET}}$ signal, the use of an external Schmidt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts, and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting, the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

POWER SUPPLIES

The ADSP-2188N has separate power supply connections for the internal (V_{DDINT}) and external (V_{DDEXT}) power supplies. The internal supply must meet the 1.8 V requirement. The external supply can be connected to either a 1.8 V, 2.5 V or 3.3 V supply. All external supply pins must be connected to the same supply. All input and I/O pins can tolerate input voltages up to 3.6 V, regardless of the external supply voltage. This feature provides maximum flexibility in mixing 1.8 V, 2.5 V or 3.3 V components.

MODES OF OPERATION

The ADSP-2188N modes of operation appear in Table 6.

Table 6. Modes of Operation

Mode D	Mode C	Mode B	Mode A	Booting Method
X	0	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Full Memory Mode.[1]
X	0	1	0	No automatic boot operations occur. Program execution starts at external memory location 0. Chip is configured in Full Memory Mode. BDMA can still be used, but the processor does not automatically use or wait for these operations.
0	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode. $\overline{\text{IACK}}$ has active pull-down. (REQUIRES ADDITIONAL HARDWARE.)
0	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until the host writes to internal program memory location 0. Chip is configured in Host Mode. $\overline{\text{IACK}}$ has active pull-down.[1]
1	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode; $\overline{\text{IACK}}$ requires external pull-down. (REQUIRES ADDITIONAL HARDWARE.)
1	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until the host writes to internal program memory location 0. Chip is configured in Host Mode. $\overline{\text{IACK}}$ requires external pull-down.[1]

[1]Considered as standard operating settings. Using these configurations allows for easier design and better memory management.

Setting Memory Mode

Memory Mode selection for the ADSP-2188N is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP's PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are active and passive.

Passive Configuration

Passive Configuration involves the use of a pull-up or pull-down resistor connected to the Mode C pin. To minimize power consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down resistance, on the order of 10 kΩ, can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor's output driver. For minimum power consumption during power-down, reconfigure PF2 to be an input, as the pull-up or pull-down resistance will hold the pin in a known state, and will not switch.

Active Configuration

Active Configuration involves the use of a three-statable external driver connected to the Mode C pin. A driver's output enable should be connected to the DSP's $\overline{\text{RESET}}$ signal such that it only drives the PF2 pin when $\overline{\text{RESET}}$ is active (low). When $\overline{\text{RESET}}$ is deasserted, the driver should be three-state, thus allowing full use of the PF2 pin as either an input or output. To minimize power consumption during power-down, configure the programmable flag as an output when connected to a three-stated buffer. This ensures that

the pin will be held at a constant level, and will not oscillate should the three-state driver's level hover around the logic switching point.

IDMA ACK Configuration

Mode D = 0 and in host mode: $\overline{\text{IACK}}$ is an active, driven signal and cannot be "wire ORed." Mode D = 1 and in host mode: $\overline{\text{IACK}}$ is an open drain and requires an external pull-down, but multiple $\overline{\text{IACK}}$ pins can be "wire ORed" together.

MEMORY ARCHITECTURE

The ADSP-2188N provides a variety of memory and peripheral interface options. The key functional groups are Program Memory, Data Memory, Byte Memory, and I/O. Refer to Figure 4, Figure 8, Table 7, and Table 9 for PM and DM memory allocations in the ADSP-2188N.

Program Memory

Program Memory (Full Memory Mode) is a 24-bit-wide space for storing both instruction opcodes and data. The ADSP-2188N has 48K words of Program Memory RAM on chip, and the capability of accessing up to two 8K external memory overlay spaces using the external data bus.

Program Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0). External program execution is not available in host mode due to a restricted data bus that is 16 bits wide only.

Table 7. PMOVLAY Bits

PMOVLAY	Memory	A13	A12:0
0, 4, 5, 6, 7	Internal	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address Between 0x2000 and 0x3FFF
2	External Overlay 2	1	13 LSBs of Address Between 0x2000 and 0x3FFF

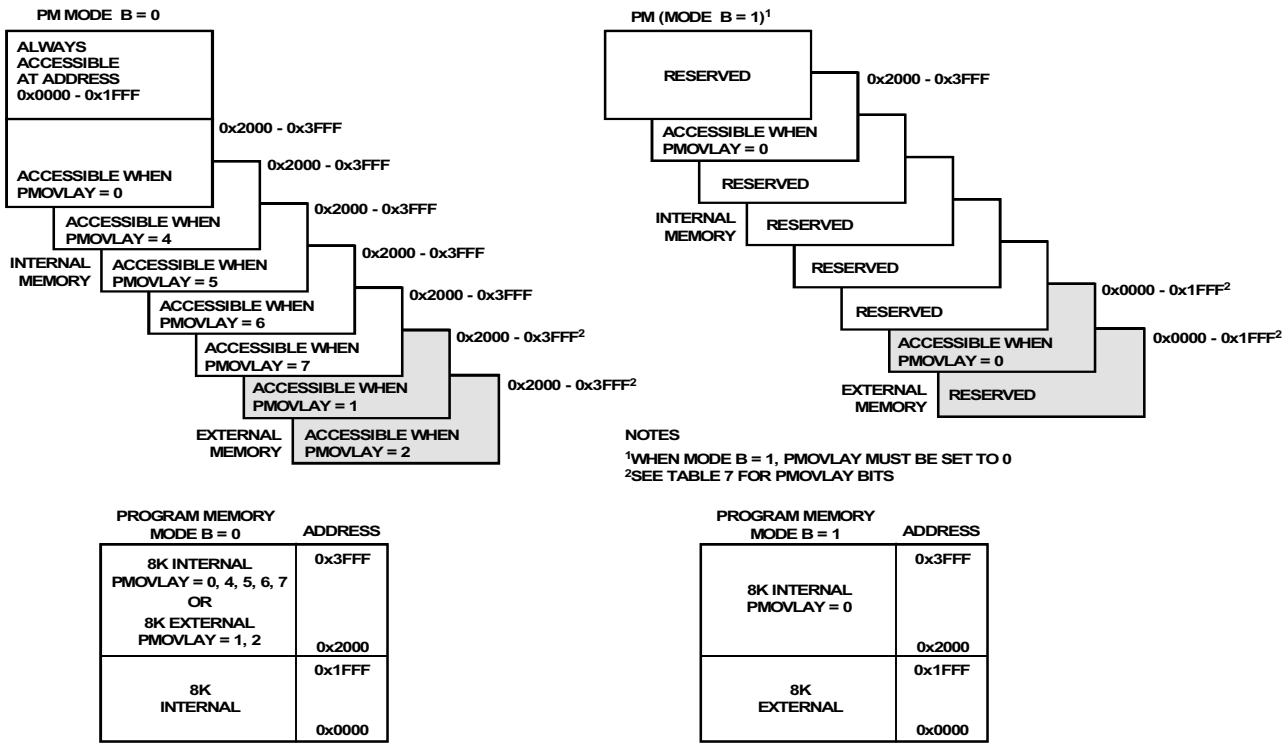


Figure 4. Program Memory

Data Memory

Data Memory (Full Memory Mode) is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-2188N has 56K words of Data Memory RAM on-chip. Part of this space is used by 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external data bus. All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register and the wait state mode bit.

Data Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0).

Memory Mapped Registers (New to the ADSP-218xM and N series)

The ADSP-2188N has three memory-mapped registers that differ from other ADSP-21xx Family DSPs. The slight modifications to these registers (Wait State Control, Programmable Flag and Composite Select Control, and System Control) provide the ADSP-2188N's wait state and $\overline{\text{BMS}}$ control features. Default bit values at reset are shown; if no value is shown, the bit is undefined at reset. Reserved bits are shown on a grey field. These bits should always be written with zeros.

I/O Space (Full Memory Mode)

The ADSP-2188N supports an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit wide data. The lower eleven bits of the external address bus are used; the upper three bits are undefined. Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated three-bit wait state registers, IOWAIT0:3, which in combination with the wait state mode bit, specify up to 15 wait states to be automatically generated for each of four regions. The wait states act on address ranges as shown in Table 8.

Table 8. Wait States

Address Range	Wait State Register
0x000–0x1FF	IOWAIT0 and Wait State Mode Select Bit

Table 8. Wait States (Continued)

Address Range	Wait State Register
0x200–0x3FF	IOWAIT1 and Wait State Mode Select Bit
0x400–0x5FF	IOWAIT2 and Wait State Mode Select Bit
0x600–0x7FF	IOWAIT3 and Wait State Mode Select Bit

Table 9. DMOVLAY Bits

DMOVLAY	Memory	A13	A12:0
0, 4, 5, 6, 7, 8	Internal	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address Between 0x2000 and 0x3FFF
2	External Overlay 2	1	13 LSBs of Address Between 0x2000 and 0x3FFF

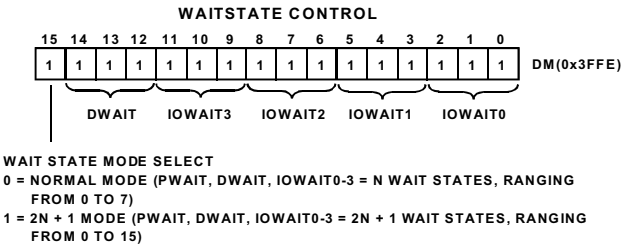


Figure 5. Wait State Control Register

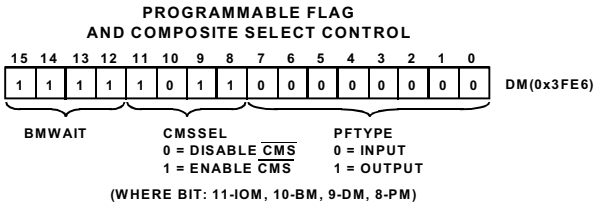


Figure 6. Programmable Flag and Composite Control Register

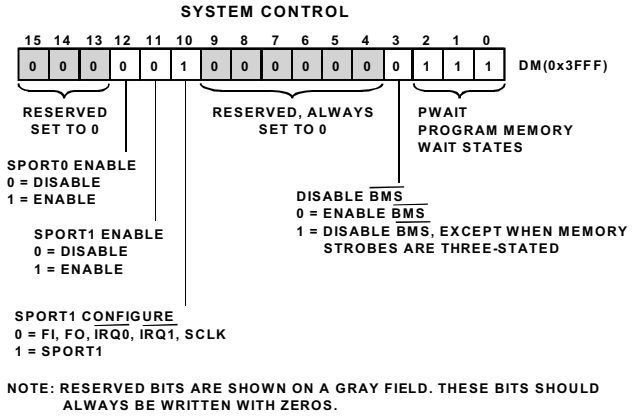


Figure 7. System Control Register

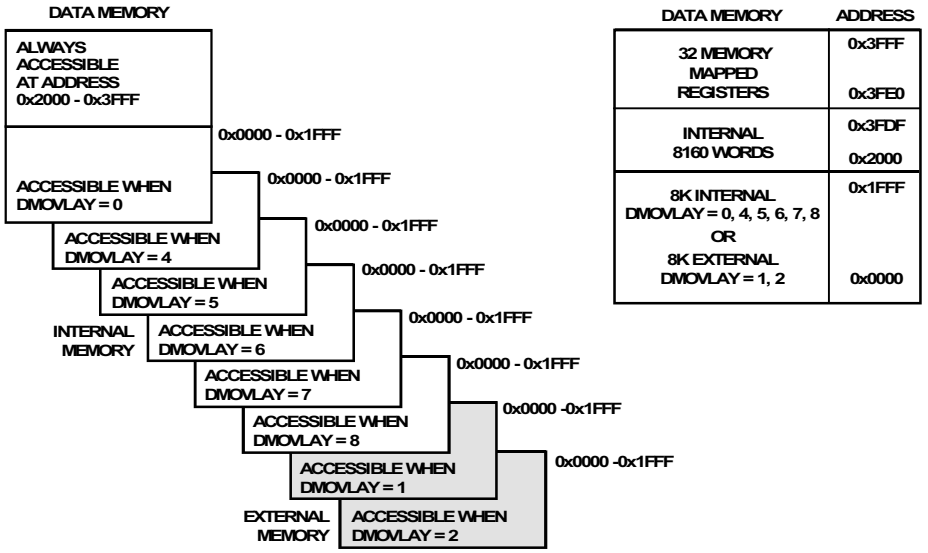


Figure 8. Data Memory Map

Composite Memory Select

The ADSP-2188N has a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality. Each bit in the CMSSEL register, when set, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory, and use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All enable bits default to 1 at reset, except the $\overline{\text{BMS}}$ bit.

Byte Memory Select

The ADSP-2188N's $\overline{\text{BMS}}$ disable feature combined with the $\overline{\text{CMS}}$ pin allows use of multiple memories in the byte memory space. For example, an EPROM could be attached to the $\overline{\text{BMS}}$ select, and an SRAM could be connected to $\overline{\text{CMS}}$. Because at reset $\overline{\text{BMS}}$ is enabled, the EPROM would be used for booting. After booting, software could disable $\overline{\text{BMS}}$ and set the $\overline{\text{CMS}}$ signal to respond to $\overline{\text{BMS}}$, enabling the SRAM.

Byte Memory

The byte memory space is a bidirectional, 8-bit-wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The byte memory space consists of 256 pages, each of which is 16K × 8 bits.

The byte memory space on the ADSP-2188N supports read and write operations as well as four different data formats. The byte memory uses data bits 15:8 for data. The byte memory uses data bits 23:16 and address bits 13:0 to create a 22-bit address. This allows up to a 4 meg × 8 (32 megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BMWAIT register and the wait state mode bit.

Byte Memory DMA (BDMA, Full Memory Mode)

The byte memory DMA controller allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit is able to access the byte memory space while the processor is operating normally and steals only one DSP cycle per 8-, 16-, or 24-bit word transferred.

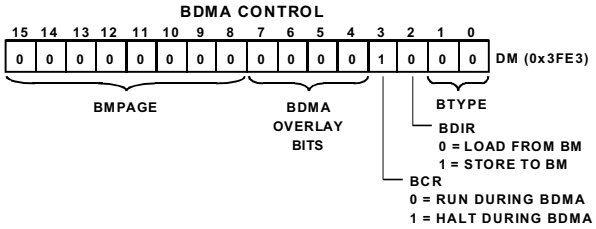


Figure 9. BDMA Control Register

The BDMA circuit supports four different data formats that are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table 10 shows the data formats supported by the BDMA circuit.

Table 10. Data Formats

BTYPE	Internal Memory Space	Word Size	Alignment
00	Program Memory	24	Full Word
01	Data Memory	16	Full Word
10	Data Memory	8	MSBs
11	Data Memory	8	LSBs

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte memory space. The 8-bit BMPAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally, the 14-bit BWCOUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BWCOUNT register.

The BWCOUNT register is updated after each transfer so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BMPAGE and BEAD registers must not be accessed by the DSP during BDMA operations.

The source or destination of a BDMA transfer will always be on-chip program or data memory.

When the BWCOUNT register is written with a nonzero value the BDMA circuit starts executing byte memory accesses with wait states set by BMWAIT. These accesses continue until the count reaches zero. When enough accesses have occurred to create a destination word, it is transferred to or from on-chip memory. The transfer takes one DSP cycle. DSP accesses to external memory have priority over BDMA byte memory accesses.

The BDMA Context Reset bit (BCR) controls whether the processor is held off while the BDMA accesses are occurring. Setting the BCR bit to 0 allows the processor to continue operations. Setting the BCR bit to 1 causes the processor to stop execution while the BDMA accesses are occurring, to clear the context of the processor, and start execution at address 0 when the BDMA accesses have completed.

The BDMA overlay bits specify the OVLAY memory blocks to be accessed for internal memory.

The BMWAIT field, which has 4 bits on ADSP-2188N, allows selection up to 15 wait states for BDMA transfers.

Internal Memory DMA Port (IDMA Port; Host Memory Mode)

The IDMA Port provides an efficient means of communication between a host system and the ADSP-2188N. The port is used to access the on-chip program memory and data memory of the DSP with only one DSP cycle per word overhead. The IDMA port cannot, however, be used to write to the DSP's memory-mapped control registers. A typical IDMA transfer process is described as follows:

1. Host starts IDMA transfer.
2. Host checks $\overline{\text{IACK}}$ control line to see if the DSP is busy.

3. Host uses $\overline{IS}$ and IAL control lines to latch either the DMA starting address (IDMAA) or the PM/DM OVLAY selection into the DSP's IDMA control registers. If Bit 15 = 1, the value of bits 7:0 represent the IDMA overlay; bits 14:8 must be set to 0. If Bit 15 = 0, the value of Bits 13:0 represent the starting address of internal memory to be accessed and Bit 14 reflects PM or DM for access.
4. Host uses $\overline{IS}$ and $\overline{IRD}$ (or $\overline{IWR}$) to read (or write) DSP internal memory (PM or DM).
5. Host checks $\overline{IACK}$ line to see if the DSP has completed the previous IDMA operation.
6. Host ends IDMA transfer.

The IDMA port has a 16-bit multiplexed address and data bus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written while the ADSP-2188N is operating at full speed.

The DSP memory address is latched and then automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA Port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location, the destination type specifies whether it is a DM or PM access. The falling edge of the IDMA address latch signal (IAL) or the missing edge of the IDMA select signal ($\overline{IS}$) latches this value into the IDMAA register.

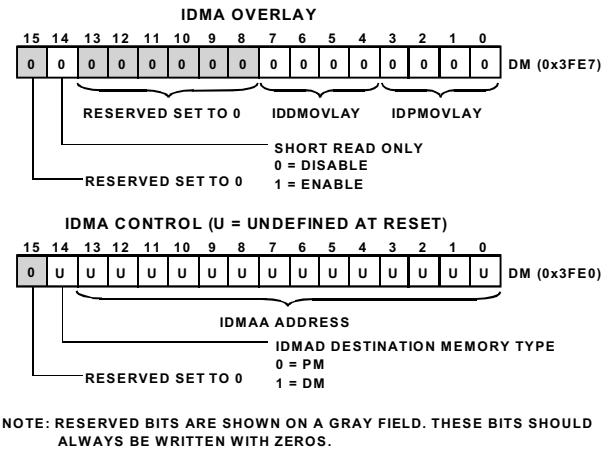
Once the address is stored, data can be read from, or written to, the ADSP-2188N's on-chip memory. Asserting the select line ($\overline{IS}$) and the appropriate read or write line ($\overline{IRD}$ and $\overline{IWR}$ respectively) signals the ADSP-2188N that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented, and another access can occur.

Through the IDMAA register, the DSP can also specify the starting address and data format for DMA operation. Asserting the IDMA port select ($\overline{IS}$) and address latch enable (IAL) directs the ADSP-2188N to write the address onto the IAD0:14 bus into the IDMA Control Register. If Bit 15 is set to 0, IDMA latches the address. If Bit 15 is set to 1, IDMA latches into the OVLAY register. This register, shown in Figure 10, is memory-mapped at address DM (0x3FE0). Note that the latched address (IDMAA) cannot be read back by the host.

When Bit 14 in 0x3FE7 is set to zero, short reads use the timing shown in Figure 24 on page 36. When Bit 14 in 0x3FE7 is set to one, timing in Figure 25 on page 37 applies for short reads in short read only mode. Refer to the ADSP-218x DSP Hardware Reference for additional details.

Refer to Figure 10 for more information on IDMA and DMA memory maps.



NOTE: RESERVED BITS ARE SHOWN ON A GRAY FIELD. THESE BITS SHOULD ALWAYS BE WRITTEN WITH ZEROS.

Figure 10. IDMA Control/OVLAY Registers

Bootstrap Loading (Booting)

The ADSP-2188N has two mechanisms to allow automatic loading of the internal program memory after reset. The method for booting is controlled by the Mode A, B, and C configuration bits.

When the mode pins specify BDMA booting, the ADSP-2188N initiates a BDMA boot sequence when reset is released.

The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD, and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24-bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory. These 32 words are used to set up the BDMA to load in the remaining program code. The BCR bit is also set to 1, which causes program execution to be held off until all 32 words are loaded into on-chip program memory. Execution then begins at address 0.

The ADSP-2100 Family development software (Revision 5.02 and later) fully supports the BDMA booting feature and can generate byte memory space-compatible boot code.

The IDLE instruction can also be used to allow the processor to hold off execution while booting continues through the BDMA interface. For BDMA accesses while in Host

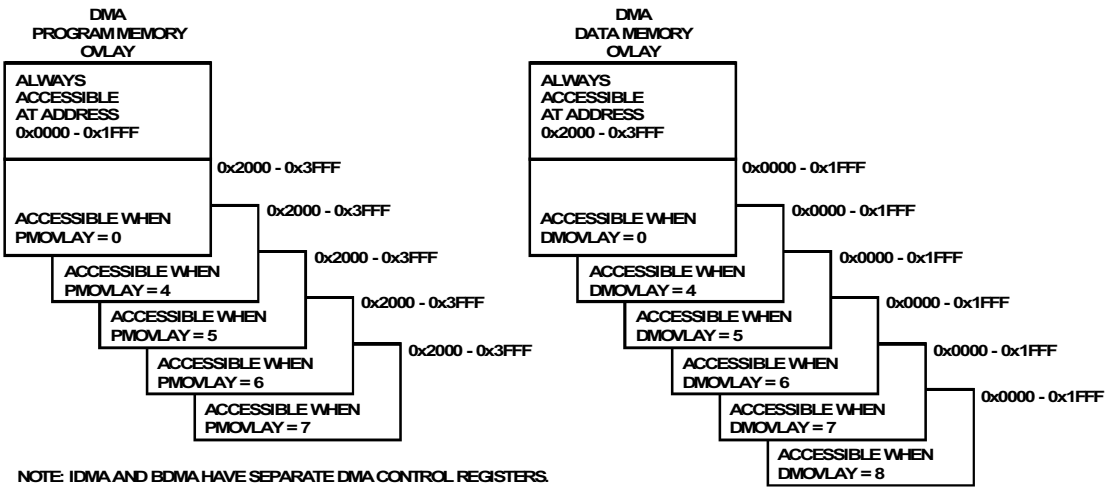


Figure 11. Direct Memory Access—PM and DM Memory Maps

Mode, the addresses to boot memory must be constructed externally to the ADSP-2188N. The only memory address bit provided by the processor is A0.

IDMA Port Booting

The ADSP-2188N can also boot programs through its Internal DMA port. If Mode C = 1, Mode B = 0, and Mode A = 1, the ADSP-2188N boots from the IDMA port. IDMA feature can load as much on-chip memory as desired. Program execution is held off until the host writes to on-chip program memory location 0.

BUS REQUEST AND BUS GRANT

The ADSP-2188N can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the Bus Request ($\overline{BR}$) signal. If the ADSP-2188N is not performing an external memory access, it responds to the active $\overline{BR}$ input in the following processor cycle by:

- Three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- Asserting the bus grant ($\overline{BG}$) signal, and
- Halting program execution.

If Go Mode is enabled, the ADSP-2188N will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-2188N is performing an external memory access when the external device asserts the $\overline{BR}$ signal, it will not three-state the memory interfaces nor assert the $\overline{BG}$ signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, re-enables the output drivers, and continues program execution from the point at which it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The $\overline{BGH}$ pin is asserted when the ADSP-2188N requires the external bus for a memory or BDMA access, but is stopped. The other device can release the bus by deasserting bus request. Once the bus is released, the ADSP-2188N deasserts $\overline{BG}$ and $\overline{BGH}$ and executes the external memory access.

FLAG I/O PINS

The ADSP-2188N has eight general purpose programmable input/output flag pins. They are controlled by two memory-mapped registers. The PFTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the ADSP-2188N's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

In addition to the programmable flags, the ADSP-2188N has five fixed-mode flags, FI, FO, FL0, FL1, and FL2. FL0:FL2 are dedicated output flags. FI and FO are available as an alternate configuration of SPORT1.

Note: Pins PF0, PF1, PF2, and PF3 are also used for device configuration during reset.

INSTRUCTION SET DESCRIPTION

The ADSP-2188N assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize on-chip memory and conform to the ADSP-2188N's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction with up to two fetches or one write to processor memory space during a single instruction cycle.

DESIGNING AN EZ-ICE-COMPATIBLE SYSTEM

The ADSP-2188N has on-chip emulation support and an ICE-Port, a special set of pins that interface to the EZ-ICE. These features allow in-circuit emulation without replacing the target system processor by using only a 14-pin connection from the target system to the EZ-ICE. Target systems must have a 14-pin connector to accept the EZ-ICE's in-circuit probe, a 14-pin plug.

Issuing the chip reset command during emulation causes the DSP to perform a full chip reset, including a reset of its memory mode. Therefore, it is vital that the mode pins are set correctly PRIOR to issuing a chip reset command from the emulator user interface. If a passive method of maintaining mode information is being used (as discussed in "Setting Memory Mode" on page 12), it does not matter that the mode information is latched by an emulator reset. However, if the $\overline{\text{RESET}}$ pin is being used as a method of setting the value of the mode pins, the effects of an emulator reset must be taken into consideration.

One method of ensuring that the values located on the mode pins are those desired is to construct a circuit like the one shown in Figure 12. This circuit forces the value located on the Mode A pin to logic high, regardless of whether it is latched via the $\overline{\text{RESET}}$ or $\overline{\text{ERESET}}$ pin.

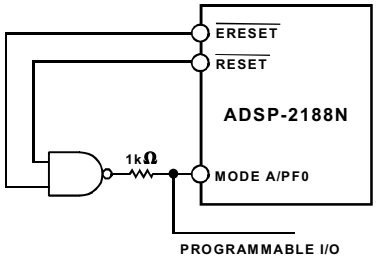


Figure 12. Mode A Pin/EZ-ICE Circuit

The ICE-Port interface consists of the following ADSP-2188N pins: $\overline{\text{EBR}}$, $\overline{\text{EINT}}$, EE, $\overline{\text{EBG}}$, ECLK, $\overline{\text{ERESET}}$, ELIN, $\overline{\text{EMS}}$, and ELOUT.

These ADSP-2188N pins must be connected only to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the ADSP-2188N and the connector must be kept as short as possible, no longer than 3 inches.

The following pins are also used by the EZ-ICE: $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{RESET}}$, and GND.

The EZ-ICE uses the EE (emulator enable) signal to take control of the ADSP-2188N in the target system. This causes the processor to use its $\overline{\text{ERESET}}$, $\overline{\text{EBR}}$, and $\overline{\text{EBG}}$ pins instead of the $\overline{\text{RESET}}$, $\overline{\text{BR}}$, and $\overline{\text{BG}}$ pins. The $\overline{\text{BG}}$ output is three-stated. These signals do not need to be jumper-isolated in your system.

The EZ-ICE connects to your target system via a ribbon cable and a 14-pin female plug. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.

Target Board Connector for EZ-ICE Probe

The EZ-ICE connector (a standard pin strip header) is shown in Figure 13. You must add this connector to your target board design if you intend to use the EZ-ICE. Be sure to allow enough room in your system to fit the EZ-ICE probe onto the 14-pin connector.

The 14-pin, 2-row pin strip header is keyed at the Pin 7 location— you must remove Pin 7 from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. The pin strip header must have at least 0.15 inch clearance on all sides to accept the EZ-ICE probe plug.

Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

Target Memory Interface

For your target system to be compatible with the EZ-ICE emulator, it must comply with the memory interface guidelines listed below.

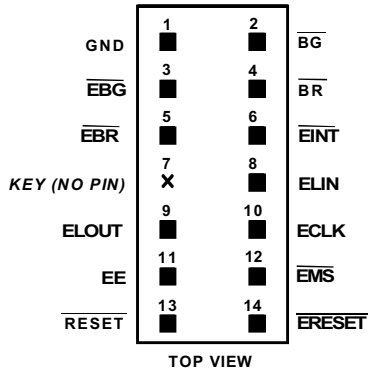


Figure 13. Target Board Connector for EZ-ICE

PM, DM, BM, IOM, AND CM

Design your Program Memory (PM), Data Memory (DM), Byte Memory (BM), I/O Memory (IOM), and Composite Memory (CM) external interfaces to comply with worst-case device timing requirements and switching characteristics as specified in this data sheet. The performance of the EZ-ICE may approach published worst-case specification for some memory access timing requirements and switching characteristics.

Note: If your target does not meet the worst-case chip specification for memory access parameters, you may not be able to emulate your circuitry at the desired CLKIN frequency. Depending on the severity of the specification violation, you may have trouble manufacturing your system, as DSP components statistically vary in switching characteristic and timing requirements, within published limits.

Restriction: All memory strobe signals on the ADSP-2188N ($\overline{RD}$, $\overline{WR}$, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, and $\overline{IOMS}$) used in your target system must have 10 kΩ pull-up resistors connected when the EZ-ICE is being used. The pull-up resistors are necessary because there are no internal pull-ups to guarantee their state during prolonged three-state conditions resulting from typical EZ-ICE debugging sessions. These resistors may be removed when the EZ-ICE is not being used.

Target System Interface Signals

When the EZ-ICE board is installed, the performance on some system signals change. Design your system to be compatible with the following system interface signal changes introduced by the EZ-ICE board:

- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{RESET}$ signal.
- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{BR}$ signal.
- EZ-ICE emulation ignores $\overline{RESET}$ and $\overline{BR}$ when single-stepping.
- EZ-ICE emulation ignores $\overline{RESET}$ and $\overline{BR}$ when in Emulator Space (DSP halted).
- EZ-ICE emulation ignores the state of target $\overline{BR}$ in certain modes. As a result, the target system may take control of the DSP's external memory bus only if bus grant ($\overline{BG}$) is asserted by the EZ-ICE board's DSP.

SPECIFICATIONS

Specifications subject to change without notice.

RECOMMENDED OPERATING CONDITIONS

Parameter			Unit
	Min	Max	
V_{DDINT}	1.71	1.89	V
V_{DDEXT}	1.71	3.6	V
V_{INPUT}[1]	V_{IL}= –0.3	V_{IH}= +3.6	V
T_{AMB}	0	+70	°C

[1]The ADSP-2188N is 3.3 V tolerant (always accepts up to 3.6 V max V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}, because V_{OH} (max) approximately equals V_{DDEXT} (max). This 3.3 V tolerance applies to bidirectional pins (D0:D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1:A13, PF0:PF7) and input-only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions				Unit
			Min	Typ	Max	
V_{IH}	Hi-Level Input Voltage[1, 2]	@ V_{DDINT} = max	1.5			V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DDINT} = max	1.5			V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DDINT} = min			0.5	V
V_{OH}	Hi-Level Output Voltage[1,4,5]	@ V_{DDEXT} ≥ min, I_{OH} = –0.5 mA	TBD			V
		@ V_{DDEXT} ≥ 2.5 V, I_{OH} = –0.5 mA	2.0			
		@ V_{DDEXT} ≥ 3.0 V, I_{OH} = –0.5 mA	2.4			V
		@ V_{DDEXT} ≥ min, I_{OH} = –100 µA[6]		V_{DDEXT}–0.3		V
V_{OL}	Lo-Level Output Voltage[1, 4, 5]	@ V_{DDEXT} = min, I_{OL} = 2 mA			0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 3.6 V			10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 0 V			10	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 3.6 V[8]			10	µA

ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I_{OZL}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 0 V[8]			10	µA
I_{DD}	Supply Current (Idle)[9]	@ V_{DDINT} = 1.8, t_{CK} = 12.5 ns, T_{AMB} = 25°C		TBD		mA
I_{DD}	Supply Current (Dynamic)[10]	@ V_{DDINT} = 1.8, t_{CK} = 12.5 ns[11], T_{AMB} = 25°C		TBD		mA
I_{DD}	Supply Current (Power-Down)[12]	@ V_{DDINT} = 1.8, T_{AMB} = 25°C in Lowest Power Mode		TBD		µA
C_I	Input Pin Capacitance[3, 6]	@ V_{IN} = 1.8 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			8	pF
C_O	Output Pin Capacitance[6, 7, 12, 13]	@ V_{IN} = 1.8 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			8	pF

[1]Bidirectional pins: D0:D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1:A13, PF0:PF7.

[2]Input only pins: $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[3]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[4]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2:0, $\overline{\text{BGH}}$.

[5]Although specified for TTL outputs, all ADSP-2188N outputs are CMOS-compatible and will drive to V_{DDEXT} and GND, assuming no dc loads.

[6]Guaranteed but not tested.

[7]Three-statable pins: A0:A13, D0:D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF0:PF7.

[8]0 V on $\overline{\text{BR}}$.

[9]Idle refers to ADSP-2188N state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

[10]I_{DD} measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (Types 1, 4, 5, 12, 13, 14), 30% are Type 2 and Type 6, and 20% are idle instructions.

[11]VIN = 0 V and 3 V. For typical values for supply currents, refer to *Power Dissipation* section.

[12]See *ADSP-218x DSP Hardware Reference* for details.

[13]Output pin capacitance is the capacitive load for any three-stated output pin.

ABSOLUTE MAXIMUM RATINGS

Parameter[1]	Min	Max	Unit
Internal Supply Voltage (V_{DDINT})	–0.3	+2.5	V
External Supply Voltage (V_{DDEXT})	–0.3	+4.0	V
Input Voltage[2]	–0.5	+4.0	V
Output Voltage Swing[3]	–0.5	V_{DDEXT} + 0.5	V

ABSOLUTE MAXIMUM RATINGS (CONTINUED)

Parameter[1]	Min	Max	Unit
Operating Temperature Range	0	+70	°C
Storage Temperature Range	–65	+150	°C
Lead Temperature (5 sec) LQFP		280	°C

[1]Stresses greater than those listed may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Applies to Bidirectional pins (D0:D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1:A13, PF0:PF7) and Input only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).

[3]Applies to Output pins ($\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2:0, $\overline{\text{BGH}}$).

ESD SENSITIVITY

CAUTION: ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-2188N features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

POWER DISSIPATION

To determine total power dissipation in a specific application, the following equation should be applied for each output: $C \times V_{DD}^2 \times f$

where: C = load capacitance, f = output switching frequency.

Example: In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- Application operates at V_{DDEXT} = 3.3 V and t_{CK} = 30 ns.

Total Power Dissipation = $P_{INT} + (C \times V_{DDEXT}^2 \times f)$

P_{INT}= internal power dissipation from Figure 18

$(C \times V_{DDEXT}^2 \times f)$ is calculated for each output, as in the example in Table 11.

Table 11. Example Power Dissipation Calculation

Parameters	# of Pins	× C (pF)	× V_{DDEXT}^2 (V)	× f (MHz)	PD (mW)
Address	7	10	3.3^2	16.67	12.7
Data Output, $\overline{\text{WR}}$	9	10	3.3^2	16.67	16.3
$\overline{\text{RD}}$	1	10	3.3^2	16.67	1.8
CLKOUT, $\overline{\text{DMS}}$	2	10	3.3^2	33.3	7.2
					38.0

Total power dissipation for this example is P_{INT} + 38.0 mW.

ENVIRONMENTAL CONDITIONS

Table 12. Thermal Resistance

Rating Description[1]	Symbol	LQFP	Mini-BGA
Thermal Resistance (Case-to-Ambient)	θ_{CA}	48°C /W	63.3°C /W
Thermal Resistance (Junction-to-Ambient)	θ_{JA}	50°C /W	70.7°C /W
Thermal Resistance (Junction-to-Case)	θ_{JC}	2°C /W	7.4°C /W

[1]Where the Ambient Temperature Rating (T_{AMB}) is:
$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W

TEST CONDITIONS

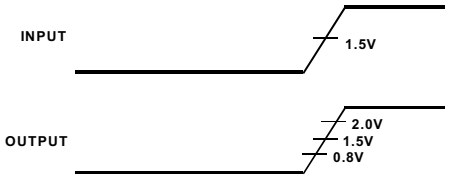


Figure 14. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

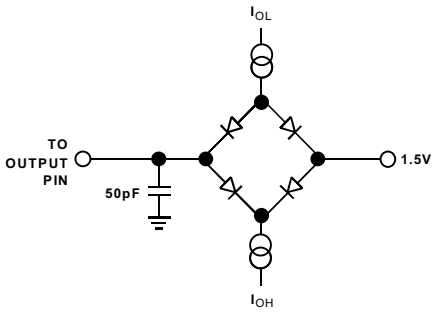


Figure 15. Equivalent Loading for AC Measurements (Including All Fixtures)

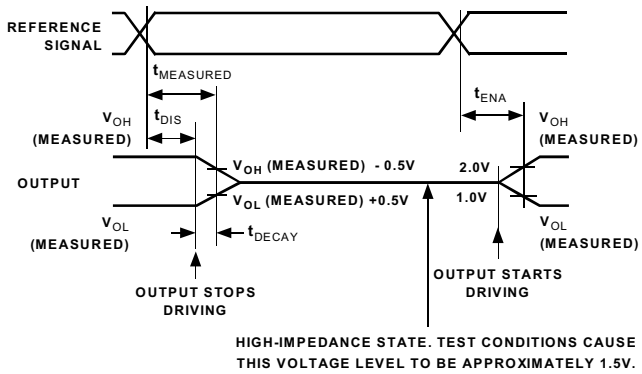


Figure 16. Output Enable/Disable

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 16. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 16. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

TIMING SPECIFICATIONS

This section contains timing information for the DSP's external signals.

General Notes

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

Timing Notes

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Memory Timing Specifications

Table 13 shows common memory device specifications and the corresponding ADSP-2188N timing parameters, for your convenience.

Table 13. Memory Timing Specifications

Memory Device Specification	Parameter	Timing Parameter Definition[1]
Address Setup to Write Start	t_{ASW}	A0:A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low
Address Setup to Write End	t_{AW}	A0:A13, $\overline{xMS}$ Setup before $\overline{WR}$ Deasserted
Address Hold Time	t_{WRA}	A0:A13, $\overline{xMS}$ Hold before $\overline{WR}$ Low
Data Setup Time	t_{DW}	Data Setup before $\overline{WR}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{WR}$ High
OE to Data Valid	t_{RDD}	$\overline{RD}$ Low to Data Valid
Address Access Time	t_{AA}	A0:A13, $\overline{xMS}$ to Data Valid

[1] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$ or $\overline{IOMS}$.

Frequency Dependency For Timing Specifications

t_{CK} is defined as 0.5 t_{CKI}. The ADSP-2188N uses an input clock with a frequency equal to half the instruction rate. For example, a 40 MHz input clock (which is equivalent to 25 ns) yields a 12.5 ns processor cycle (equivalent to 80 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain the specification value.

Example: t_{CKH} = 0.5 t_{CK} – 2 ns = 0.5 (12.5 ns) – 2 ns = 4.25 ns

Output Drive Currents

Figure 17 shows typical I-V characteristics for the output drivers on the ADSP-2188N. The curves represent the current drive capability of the output drivers as a function of output voltage.

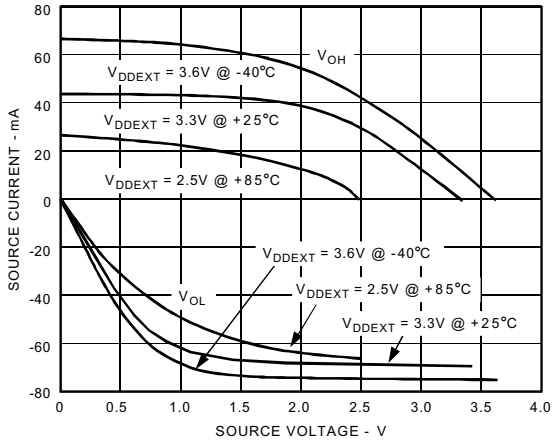


Figure 17. Typical Output Driver Characteristics

TBD

Figure 18. Power vs.Frequency

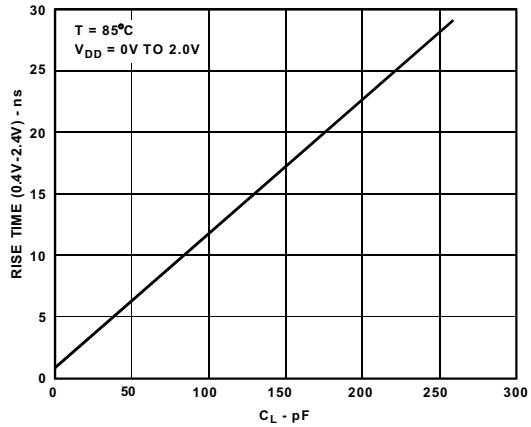


Figure 19. Typical Output Rise Time vs.Load Capacitance (at Maximum Ambient Operating Temperature)

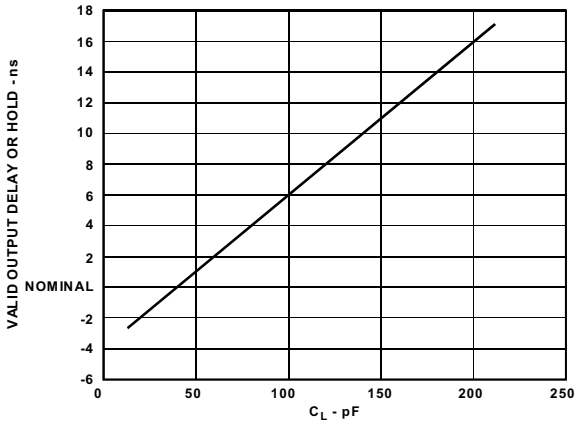


Figure 20. Typical Output Valid Delay or Hold vs.Load Capacitance, CL (at Maximum Ambient Operating Temperature)

Capacitive Loading

Figure 19 and Figure 20 show the capacitive loading characteristics of the ADSP-2188N.

Clock Signals and Reset

Table 14. Clock Signals and Reset

Parameter	Description	Min	Max	Unit
Timing Requirements:				
t_{CKI}	CLKIN Period	25	50	ns
t_{CKIL}	CLKIN Width Low	8		ns
t_{CKIH}	CLKIN Width High	8		ns
Switching Characteristics:				
t_{CKL}	CLKOUT Width Low	$0.5t_{CK} - 2$		ns
t_{CKH}	CLKOUT Width High	$0.5t_{CK} - 2$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	12	ns
Control Signals Timing Requirements:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low	$5t_{CK}$[1]		ns
t_{MS}	Mode Setup before $\overline{\text{RESET}}$ High	2		ns
t_{MH}	Mode Hold after $\overline{\text{RESET}}$ High	5		ns

[1]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles, assuming stable CLKIN (not including crystal oscillator start-up time).

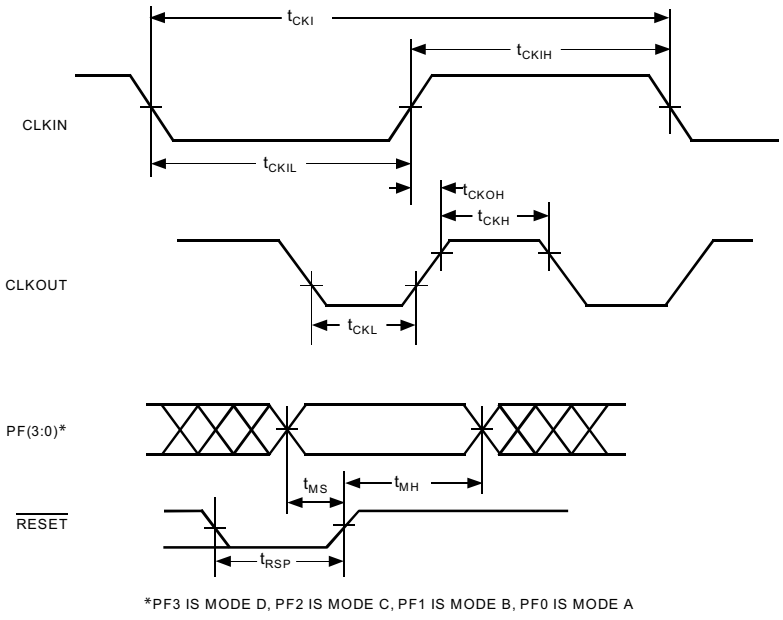


Figure 21. Clock Signals

Table 15. Interrupts and Flags

Parameter	Description	Min	Max	Unit
Timing Requirements:				
t_{IFS}	$\overline{IRQx}$, FI, or PFx Setup before CLKOUT Low[1, 2, 3, 4]	$0.25t_{CK} + 8$		ns
t_{IFH}	$\overline{IRQx}$, FI, or PFx Hold after CLKOUT High[1, 2, 3, 4]	$0.25t_{CK}$		ns
Switching Characteristics:				
t_{FOH}	Flag Output Hold after CLKOUT Low[5]	$0.5t_{CK} - 5$		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[5]		$0.5t_{CK} + 4$	ns

[1]If IRQx and FI inputs meet tIFS and tIFH setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the *Program Control* chapter of the *ADSP-218x DSP Hardware Reference* for further information on interrupt servicing.)

[2]Edge-sensitive interrupts require pulse widths greater than 10 ns; level-sensitive interrupts must be held low until serviced.

[3]$\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, $\overline{IRQLE}$.

[4]PFx = PF0, PF1, PF2, PF3, PF4, PF5, PF6, PF7.

[5]Flag Outputs = PFx, FL0, FL1, FL2, FO.

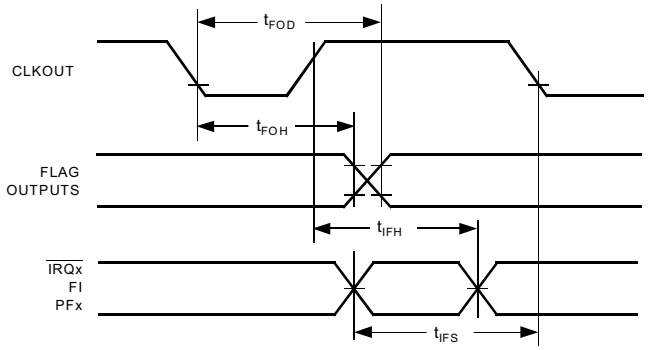


Figure 22. Interrupts and Flags

Bus Request–Bus Grant

Table 16. Bus Request–Bus Grant

Parameter	Description	Min	Max	Unit
Timing Requirements:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK} + 2$		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK} + 8$		ns
Switching Characteristics:				
t_{SD}	CLKOUT High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable[2]		$0.25t_{CK} + 8$	ns
t_{SDB}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK} - 3$		ns
t_{SDBH}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[3]	0		ns
t_{SEH}	$\overline{BGH}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable[3]	0		ns

[1]$\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual* for $\overline{BR}$/BG cycle relationships.

[2]$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

[3]$\overline{BGH}$ is asserted when the bus is granted and the processor or BDMA requires control of the bus to continue.

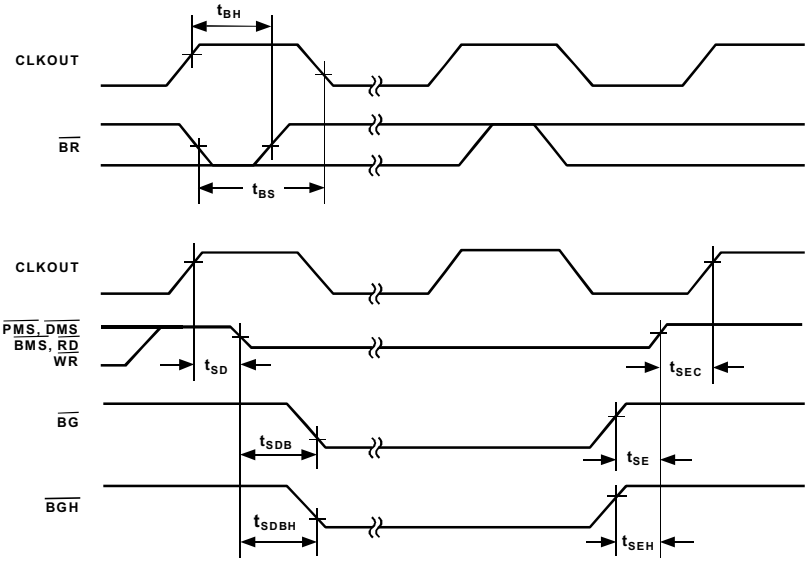


Figure 23. Bus Request –Bus Grant

Memory Read

Table 17. Memory Read

Parameter	Description	Min	Max	Unit
Timing Requirements:				
t_{RDD}	$\overline{RD}$ Low to Data Valid[1]		$0.5t_{CK} - 5 + w$	ns
t_{AA}	A0:A13, $\overline{xMS}$ to Data Valid[2]		$0.75t_{CK} - 6 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristics:				
t_{RP}	$\overline{RD}$ Pulse width	$0.5t_{CK} - 3 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 2$	$0.25t_{CK} + 4$	ns
t_{ASR}	A0:A13, $\overline{xMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 3$		ns
t_{RDA}	A0:A13, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 3$		ns

[1]w = wait states x t_{CK}.

[2]$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

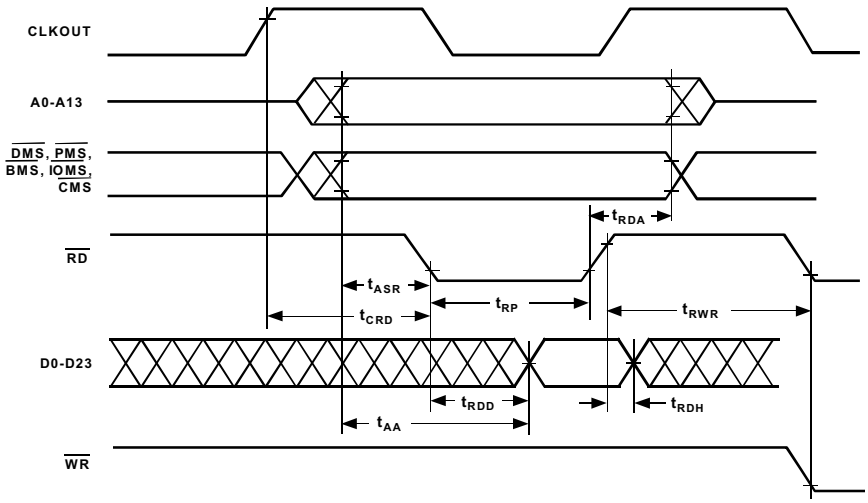


Figure 24. Memory Read

Memory Write

Table 18. Memory Write

Parameter	Description	Min	Max	Unit
Switching Characteristics:				
t_{DW}	Data Setup before $\overline{WR}$ High[1]	$0.5t_{CK}$– 4 + w		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK}$ – 1		ns
t_{WP}	$\overline{WR}$ Pulse width	$0.5t_{CK}$ – 3 + w		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0:A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low[2]	$0.25t_{CK}$ – 3		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK}$ – 3		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK}$ – 2	$0.25t_{CK}$ + 4	ns
t_{AW}	A0:A13, $\overline{xMS}$ Setup before $\overline{WR}$ Deasserted	$0.75t_{CK}$–5+w		ns
t_{WRA}	A0:A13, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK}$ – 1		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK}$ – 3		ns

[1]w = wait states x t_{CK}.

[2]$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

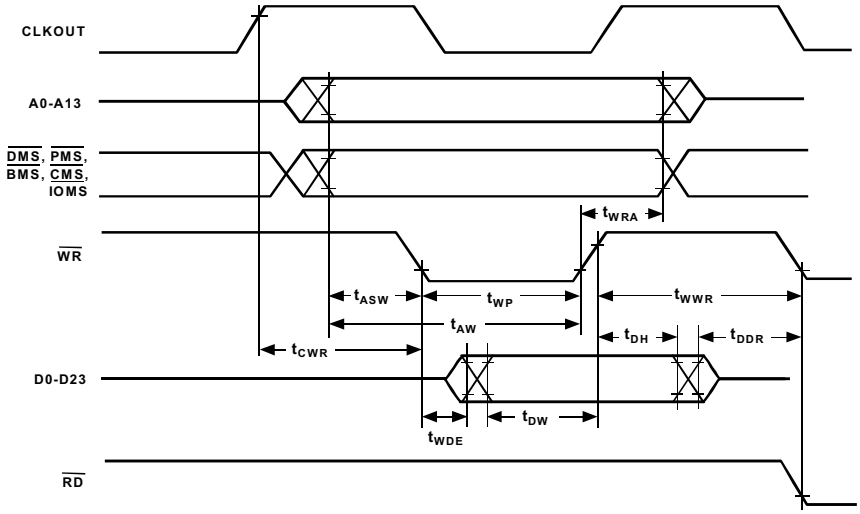


Figure 25. Memory Write

Table 19. Serial Ports

Parameter	Description	Min	Max	Unit
Timing Requirements:				
t_{SCK}	SCLK Period	30		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	7		ns
t_{SCP}	SCLKIN Width	12		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to SCLKOUT	$0.25t_{CK}$	$0.25t_{CK}$ + 6	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		12	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		12	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		12	ns
t_{SCDD}	SCLK High to DT Disable		12	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		12	ns

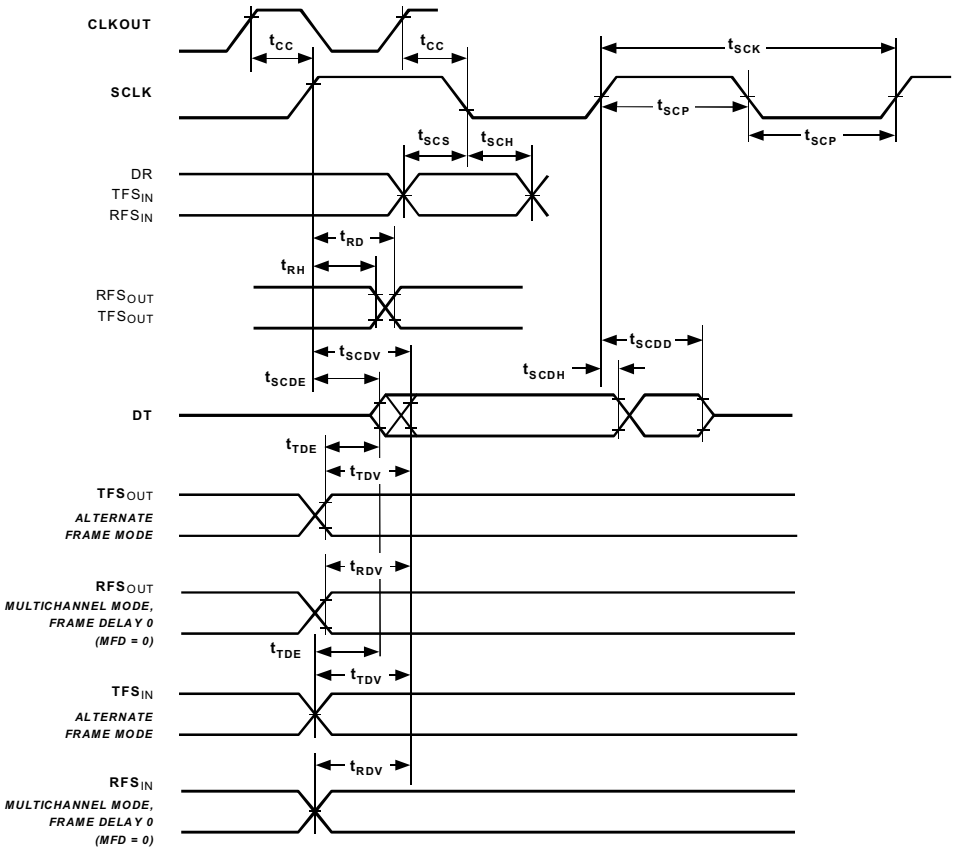


Figure 26. Serial Ports

IDMA Address Latch

Table 20. IDMA Address Latch

Parameter	Description	Min	Max	Unit
Timing Requirements:				
t_{IALP}	Duration of Address Latch[1, 2]	10		ns
t_{IASU}	IAD15:0 Address Setup before Address Latch End[2]	5		ns
t_{IAH}	IAD15:0 Address Hold after Address Latch End[2]	3		ns
t_{IKA}	$\overline{IACK}$ Low before Start of Address Latch[2, 3]	0		ns
t_{IALS}	Start of Write or Read after Address Latch End[2, 3]	3		ns
t_{IALD}	Address Latch Start after Address Latch End[1, 2]	2		ns

[1]Start of Address Latch = $\overline{IS}$ Low and IAL High.

[2]End of Address Latch = $\overline{IS}$ High or IAL Low.

[3]Start of Write or Read = $\overline{IS}$ Low and $\overline{IWR}$ Low or $\overline{IRD}$ Low.

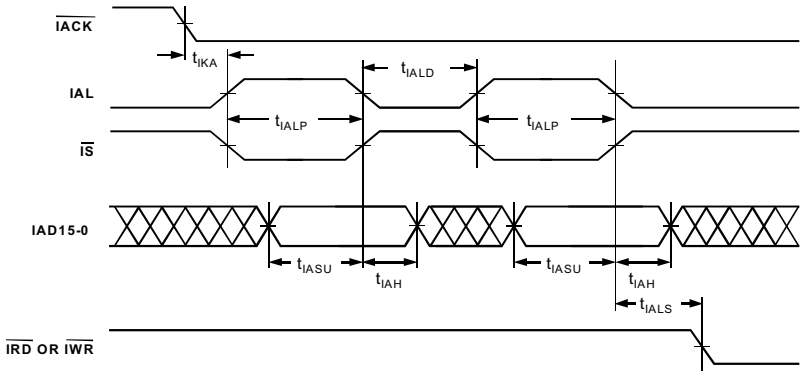


Figure 27. IDMA Address Latch

IDMA Write, Short Write Cycle

Table 21. IDMA Write, Short Write Cycle

Parameter	Description	Min	Max	Unit
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low before Start of Write[1]	0		ns
t_{IWP}	Duration of Write[1, 2]	10		ns
t_{IDSU}	IAD15:0 Data Setup before End of Write[2, 3, 4]	3		ns
t_{IDH}	IAD15:0 Data Hold after End of Write[2, 3, 4]	2		ns
Switching Characteristic:				
t_{IKHW}	Start of Write to $\overline{IACK}$ High		10	ns

[1]Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.

[2]End of Write = $\overline{IS}$ High or $\overline{IWR}$ High.

[3]If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.

[4]If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.

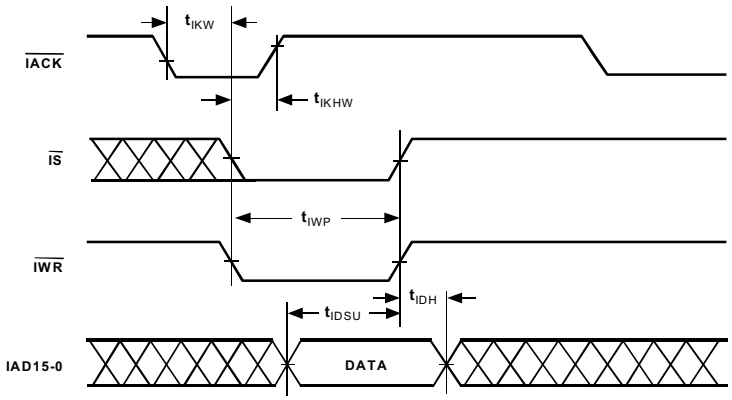


Figure 28. IDMA Write, Short Write Cycle

IDMA Write, Long Write Cycle

Table 22. IDMA Write, Long Write Cycle

Parameter	Description	Min	Max	Unit
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low before Start of Write[1]	0		ns
t_{IKSU}	IAD15:0 Data Setup before End of Write[2, 3, 4]	$0.5t_{CK}$ + 5		ns
t_{IKH}	IAD15:0 Data Hold after End of Write[2, 3, 4]	0		ns
Switching Characteristics:				
t_{IKLW}	Start of Write to $\overline{IACK}$ Low[4]	$1.5t_{CK}$		ns
t_{IKHW}	Start of Write to $\overline{IACK}$ High		10	ns

[1]Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.

[2]If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.

[3]If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.

[4]This is the earliest time for $\overline{IACK}$ Low from Start of Write. For IDMA Write cycle relationships, please refer to the *ADSP-2100 Family User's Manual*.

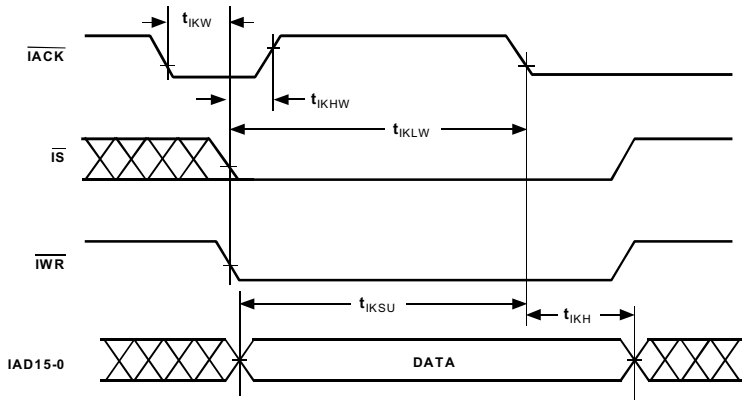


Figure 29. IDMA Write, Long Write Cycle

IDMA Read, Long Read Cycle

Table 23. IDMA Read, Long Read Cycle

Parameter	Description	Min	Max	Unit
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[1]	0		ns
t_{IRK}	End of read after $\overline{IACK}$ Low[2]	2		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[1]		10	ns
t_{IKDS}	IAD15:0 Data Setup before $\overline{IACK}$ Low	$0.5t_{CK} - 2$		ns
t_{IKDH}	IAD15:0 Data Hold after End of Read[2]	0		ns
t_{IKDD}	IAD15:0 Data Disabled after End of Read[2]		10	ns
t_{IRDE}	IAD15:0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15:0 Previous Data Valid after Start of Read		11	ns
t_{IRDH1}	IAD15:0 Previous Data Hold after Start of Read (DM/PM1)[3]	$2t_{CK} - 5$		ns
t_{IRDH2}	IAD15:0 Previous Data Hold after Start of Read (PM2)[4]	$t_{CK} - 5$		ns

[1]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.

[2]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

[3]DM read or first half of PM read.

[4]4 Second half of PM read.

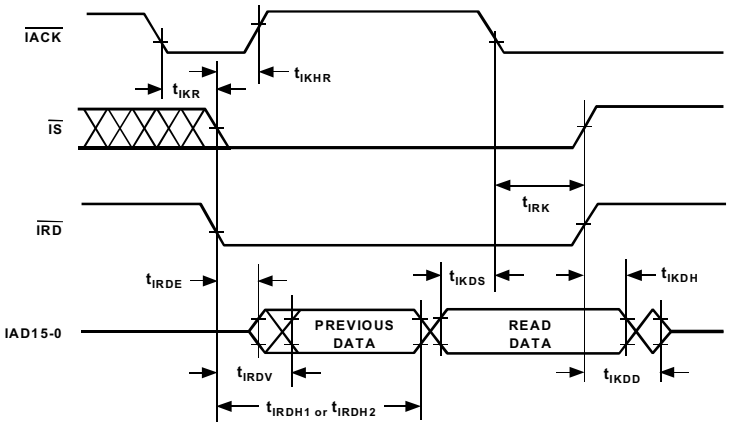


Figure 30. IDMA Read, Long Read Cycle

IDMA Read, Short Read Cycle

Table 24. IDMA Read, Short Read Cycle

Parameter[1, 2]	Description	Min	Max	Unit
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[3]	0		ns
t_{IRP1}	Duration of Read (DM/PM1)[4]	10	$2t_{CK} - 5$	ns
t_{IRP2}	Duration of Read (PM2)[5]	10	$t_{CK} - 5$	ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[3]		10	ns
t_{IKDH}	IAD15:0 Data Hold after End of Read[6]	0		ns
t_{IKDD}	IAD15:0 Data Disabled after End of Read[6]		10	ns
t_{IRDE}	IAD15:0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15:0 Previous Data Valid after Start of Read		10	ns

[1]Short Read Only must be disabled in the IDMA Overlay memory mapped register.

[2]Consider using the Short Read Only mode, instead, because Short Read mode is not applicable at high clock frequencies.

[3]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.

[4]DM Read or first half of PM Read.

[5]Second half of PM Read.

[6]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

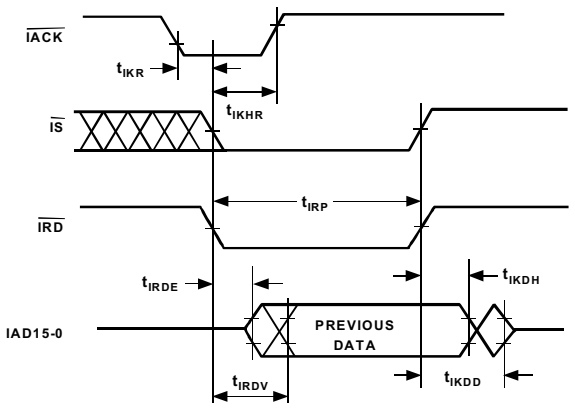


Figure 31. IDMA Read, Short Read Cycle

IDMA Read, Short Read Cycle in Short Read Only Mode

Table 25. IDMA Read, Short Read Cycle in Short Read Only Mode

Parameter[1]	Description	Min	Max	Unit
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[2]	0		ns
t_{IRP}	Duration of Read[3]	10		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[2]		10	ns
t_{IKDH}	IAD15:0 Previous Data Hold after End of Read[3]	0		ns
t_{IKDD}	IAD15:0 Previous Data Disabled after End of Read[3]		10	ns
t_{IRDE}	IAD15:0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15:0 Previous Data Valid after Start of Read		10	ns

[1]Short Read Only is enabled by setting Bit 14 of the IDMA Overlay Register to 1 (0x3FE7). Short Read Only can be enabled by the processor core writing to the register or by an external host writing to the register. Disabled by default.

[2]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low. Previous data remains until end of read.

[3]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

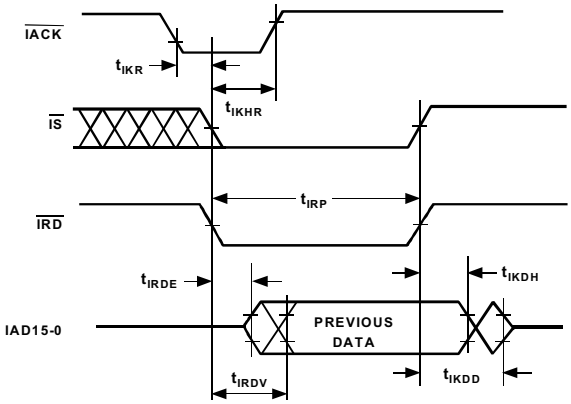


Figure 32. IDMA Read, Short Read Only Cycle

LQFP Package Pinout

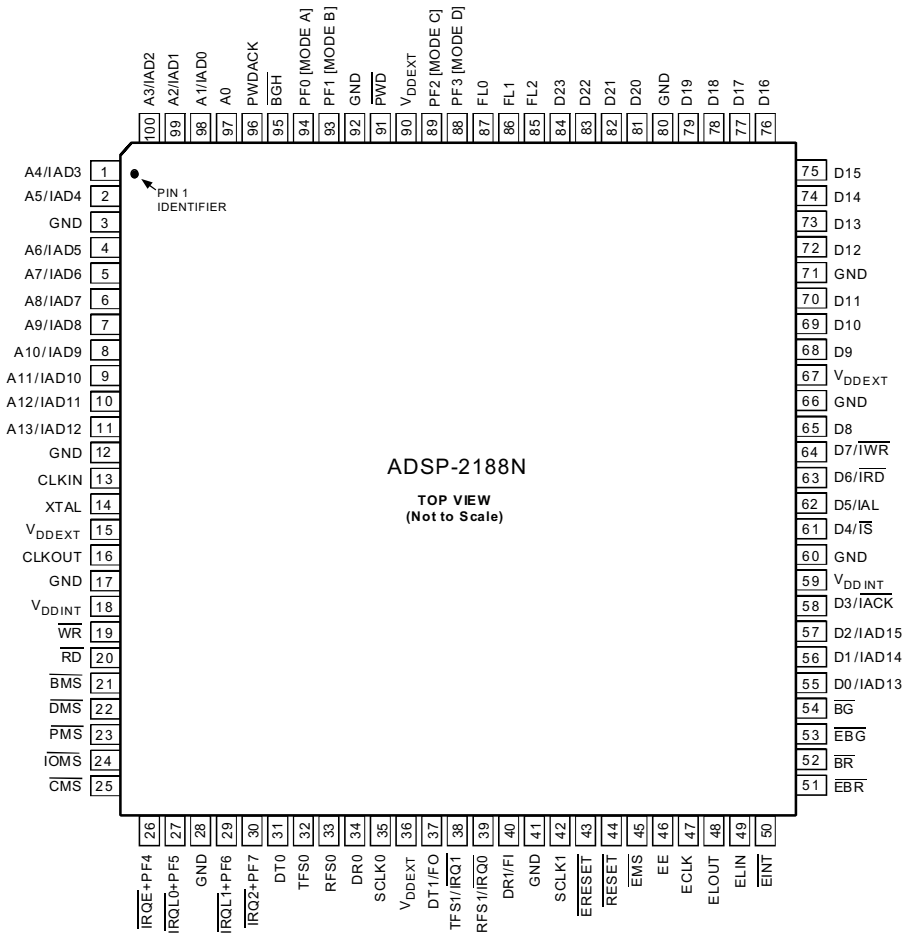


Figure 33. 100-Lead LQFP Pin Configuration

The LQFP package pinout is shown in Figure 33 and Table 26. Pin names in bold text in the table replace the plain-text-named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$. The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default, upon reset.

Table 26. LQFP Package Pinout

Pin #	Pin Name
1	A4/**IAD3**
2	A5/**IAD4**
3	GND
4	A6/**IAD5**
5	A7/**IAD6**
6	A8/**IAD7**
7	A9/**IAD8**
8	A10/**IAD9**
9	A11/**IAD10**
10	A12/**IAD11**
11	A13/**IAD12**
12	GND
13	CLKIN
14	XTAL
15	V_{DDEXT}
16	CLKOUT
17	GND
18	V_{DDINT}
19	$\overline{WR}$
20	$\overline{RD}$
21	$\overline{BMS}$
22	$\overline{DMS}$
23	$\overline{PMS}$
24	$\overline{IOMS}$
25	$\overline{CMS}$
26	$\overline{IRQE}$ + PF4
27	$\overline{IRQL0}$ + PF5
28	GND
29	$\overline{IRQL1}$ + PF6
30	$\overline{IRQ2}$ + PF7

Table 26. LQFP Package Pinout (Continued)

Pin #	Pin Name
31	DT0
32	TFS0
33	RFS0
34	DR0
35	SCLK0
36	V_{DDEXT}
37	DT1/FO
38	TFS1/$\overline{IRQ1}$
39	RFS1/$\overline{IRQ0}$
40	DR1/FI
41	GND
42	SCLK1
43	$\overline{ERESET}$
44	$\overline{RESET}$
45	$\overline{EMS}$
46	EE
47	ECLK
48	ELOUT
49	ELIN
50	$\overline{EINT}$
51	$\overline{EBR}$
52	$\overline{BR}$
53	$\overline{EBG}$
54	$\overline{BG}$
55	D0/**IAD13**
56	D1/**IAD14**
57	D2/**IAD15**
58	D3/**$\overline{IACK}$**
59	V_{DDINT}
60	GND

Table 26. LQFP Package Pinout (Continued)

Pin #	Pin Name
61	D4/**$\overline{IS}$**
62	D5/**IAL**
63	D6/**$\overline{IRD}$**
64	D7/**$\overline{IWR}$**
65	D8
66	GND
67	V_{DDEXT}
68	D9
69	D10
70	D11
71	GND
72	D12
73	D13
74	D14
75	D15
76	D16
77	D17
78	D18
79	D19
80	GND
81	D20
82	D21
83	D22
84	D23
85	FL2
86	FL1
87	FL0
88	PF3 [Mode D]
89	PF2 [Mode C]
90	V_{DDEXT}

Table 26. LQFP Package Pinout (Continued)

Pin #	Pin Name
91	$\overline{PWD}$
92	GND
93	PF1 [Mode B]
94	PF0 [Mode A]
95	$\overline{BGH}$
96	PWDACK
97	A0
98	A1/**IAD0**
99	A2/**IAD1**
100	A3/**IAD2**

Mini-BGA Package Pinout

The Mini-BGA package pinout is shown in Figure 34 and Table 27. Pin names in bold text in the table replace the plain text named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$. The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default upon reset.

12	11	10	9	8	7	6	5	4	3	2	1	
GND	GND	D22	NC	NC	NC	GND	NC	A0	GND	A1/IAD0	A2/IAD1	A
D16	D17	D18	D20	D23	V_{DDEXT}	GND	NC	NC	GND	A3/IAD2	A4/IAD3	B
D14	NC	D15	D19	D21	V_{DDEXT}	$\overline{\text{PWD}}$	A7/IAD6	A5/IAD4	$\overline{\text{RD}}$	A6/IAD5	PWDACK	C
GND	NC	D12	D13	NC	PF2 [MODE C]	PF1 [MODE B]	A9/IAD8	$\overline{\text{BGH}}$	NC	$\overline{\text{WR}}$	NC	D
D10	GND	V_{DDEXT}	GND	GND	PF3 [MODE D]	FL2	PF0 [MODE A]	FL0	A8/IAD7	V_{DDEXT}	V_{DDEXT}	E
D9	NC	D8	D11	D7/$\overline{\text{IWR}}$	NC	NC	FL1	A11/IAD10	A12/IAD11	NC	A13/IAD12	F
D4/$\overline{\text{IS}}$	NC	NC	D5/IAL	D6/$\overline{\text{IRD}}$	NC	NC	NC	A10/IAD9	GND	NC	XTAL	G
GND	NC	GND	D3/$\overline{\text{IACK}}$	D2/IAD15	TFS0	DT0	V_{DDINT}	GND	GND	GND	CLKIN	H
V_{DDINT}	V_{DDINT}	D1/IAD14	$\overline{\text{BG}}$	RFS1/$\overline{\text{IRQ0}}$	D0/IAD13	SCLK0	V_{DDEXT}	V_{DDEXT}	NC	V_{DDINT}	CLKOUT	J
$\overline{\text{EBG}}$	$\overline{\text{BR}}$	$\overline{\text{EBR}}$	$\overline{\text{ERESET}}$	SCLK1	TFS1/$\overline{\text{IRQ1}}$	RFS0	$\overline{\text{DMS}}$	$\overline{\text{BMS}}$	NC	NC	NC	K
$\overline{\text{EINT}}$	ELOUT	ELIN	$\overline{\text{RESET}}$	GND	DR0	$\overline{\text{PMS}}$	GND	$\overline{\text{IOMS}}$	$\overline{\text{IRQL1}}$ + PF6	NC	$\overline{\text{IRQE}}$ + PF4	L
ECLK	EE	$\overline{\text{EMS}}$	NC	GND	DR1/FI	DT1/FO	GND	$\overline{\text{CMS}}$	NC	$\overline{\text{IRQ2}}$ + PF7	$\overline{\text{IRQL0}}$ + PF5	M

Figure 34. 144-Ball Mini-BGA Package Pinout (Bottom View)

Table 27. Mini-BGA Package Pinout

Ball #	Pin Name
A01	A2/**IAD1**
A02	A1/**IAD0**
A03	GND
A04	A0
A05	NC
A06	GND
A07	NC
A08	NC
A09	NC
A10	D22
A11	GND
A12	GND
B01	A4/**IAD3**
B02	A3/**IAD2**
B03	GND
B04	NC
B05	NC
B06	GND
B07	V_{DDEXT}
B08	D23
B09	D20
B10	D18
B11	D17
B12	D16
C01	PWDACK
C02	A6/**IAD5**
C03	$\overline{RD}$
C04	A5/**IAD4**
C05	A7/**IAD6**
C06	$\overline{PWD}$

Table 27. Mini-BGA Package Pinout (Continued)

Ball #	Pin Name
C07	V_{DDEXT}
C08	D21
C09	D19
C10	D15
C11	NC
C12	D14
D01	NC
D02	$\overline{WR}$
D03	NC
D04	$\overline{BGH}$
D05	A9/**IAD8**
D06	PF1 [MODE B]
D07	PF2 [MODE C]
D08	NC
D09	D13
D10	D12
D11	NC
D12	GND
E01	V_{DDEXT}
E02	V_{DDEXT}
E03	A8/**IAD7**
E04	FL0
E05	PF0 [MODE A]
E06	FL2
E07	PF3 [MODE D]
E08	GND
E09	GND

Table 27. Mini-BGA Package Pinout (Continued)

Ball #	Pin Name
E10	V_{DDEXT}
E11	GND
E12	D10
F01	A13/**IAD12**
F02	NC
F03	A12/**IAD11**
F04	A11/**IAD10**
F05	FL1
F06	NC
F07	NC
F08	D7/$\overline{\textbf{IWR}}$
F09	D11
F10	D8
F11	NC
F12	D9
G01	XTAL
G02	NC
G03	GND
G04	A10/**IAD9**
G05	NC
G06	NC
G07	NC
G08	D6/$\overline{\textbf{IRD}}$
G09	D5/**IAL**
G10	NC
G11	NC
G12	D4/$\overline{\textbf{IS}}$
H01	CLKIN
H02	GND
H03	GND

Table 27. Mini-BGA Package Pinout (Continued)

Ball #	Pin Name
H04	GND
H05	V_{DDINT}
H06	DT0
H07	TFS0
H08	D2/**IAD15**
H09	D3/$\overline{\textbf{IACK}}$
H10	GND
H11	NC
H12	GND
J01	CLKOUT
J02	V_{DDINT}
J03	NC
J04	V_{DDEXT}
J05	V_{DDEXT}
J06	SCLK0
J07	D0/**IAD13**
J08	RFS1/$\overline{IRQ0}$
J09	$\overline{BG}$
J10	D1/**IAD14**
J11	V_{DDINT}
J12	V_{DDINT}
K01	NC
K02	NC
K03	NC
K04	$\overline{BMS}$
K05	$\overline{DMS}$
K06	RFS0
K07	TFS1/$\overline{IRQ1}$
K08	SCLK1
K09	$\overline{ERESET}$

Table 27. Mini-BGA Package Pinout (Continued)

Ball #	Pin Name
K10	$\overline{\text{EBR}}$
K11	$\overline{\text{BR}}$
K12	$\overline{\text{EBG}}$
L01	$\overline{\text{IRQE}}$ + PF4
L02	NC
L03	$\overline{\text{IRQL1}}$ + PF6
L04	$\overline{\text{IOMS}}$
L05	GND
L06	$\overline{\text{PMS}}$
L07	DR0
L08	GND
L09	$\overline{\text{RESET}}$
L10	ELIN
L11	ELOUT
L12	$\overline{\text{EINT}}$
M01	$\overline{\text{IRQL0}}$ + PF5
M02	$\overline{\text{IRQL2}}$ + PF7
M03	NC
M04	$\overline{\text{CMS}}$
M05	GND
M06	DT1/FO
M07	DR1/FI
M08	GND
M09	NC
M10	$\overline{\text{EMS}}$
M11	EE
M12	ECLK

OUTLINE DIMENSIONS

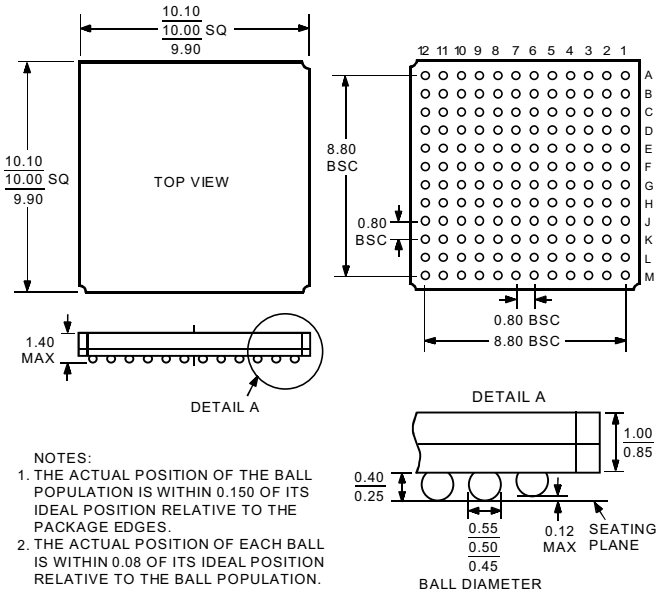


Figure 35. 144-Ball Mini-BGA (CA-144)

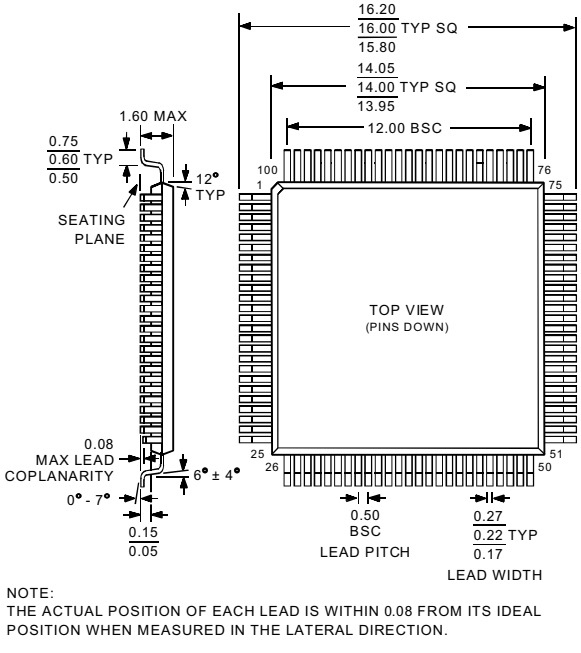


Figure 36. 100-lead Metric Thin Plastic Quad Flatpack (LQFP) (ST-100)

ORDERING GUIDE

Table 28. Ordering Guide

Part Number	Ambient Temperature Range	Instruction Rate	Package Description[1]	Package Option
ADSP-2188NKST-300X	0°C to 70°C	80	100-Lead LQFP	ST-100
ADSP-2188NKCA-300X	0°C to 70°C	80	144-Ball Mini-BGA	CA-144

[1]In 1998, JEDEC reevaluated the specifications for the TQFP package designation, assigning it to packages 1.0 mm thick. Previously-labeled TQFP packages (1.6 mm thick) are now designated as LQFP.