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NTE1888
Integrated Circuit
Horizontal and Vertical Deflection Monitor

Features:
- Direct Line Darlington Drive
- Direct Frame Yoke Drive (± 1A)
- Composite Video Signal Input Capability
- Frame Output Protection Against Short Circuits
- PLL

Description:
The NTE1888 is both a horizontal and a vertical deflection circuit in one 16–Lead DIP package.

Absolute Maximum Ratings:
Supply Voltage $V_{CC}1$ 30V
Flyback Generator Supply Voltage V_2 . . . . . 35V
Frame Power Supply Voltage V_7 . . . . . 60V
Frame Output Current, I_8
Non–Repetitive . . . . . ±1.5A
Continuous . . . . . ±1.0A
Line Output Voltage (External), V_{14} 60V
Line Output Peak Current, I_{P14} 0.8A
Line Output Continuous Current, I_{C14} 0.4A
Storage Temperature Range, T_{stg} . . . . . –40° to +150°C
Maximum Operating Junction Temperature, T_j . . . . . +150°C
Maximum Thermal Resistance, Junction–to–Case, R_{thJC} . . . . . 15°C/W
Typical Thermal Resistance, Junction–to–Ambient, R_{thJA}
(soldered on a 35µm thick 45cm^2 PC board copper area) . . . . . 45°C/W
Maximum Recommended Junction Temperature, T_J . . . . . +120°C

Electrical Characteristics: (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Supply Current	$I_{CC}1$	@ Pin16		10	–	20	mA
Supply Voltage	$V_{CC}1$		$I_{CC}1$ = 15mA	9.0	9.8	10.5	V
Voltage Variation	$\Delta V_{CC}1$		$I_{CC}1$ = 10mA→20mA	–280	50	+280	mV
Starting Threshold for Line Output Pulses	LPS			–	–	5	V

Electrical Characteristics (Cont'd): (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Reference Voltage	V_{15}	@ Pin15	I_{15} = –1µA	1.4	1.75	2.0	V
Minimum Width of Frame Pulse (when synchronized with TTL signal)	MWF			50	–	–	µs
Low Threshold Voltage	LT_9	@ Pin9		2.8	3.2	3.6	V
High Threshold Voltage	HT_9			6.4	6.6	7.8	V
Bias Current	BI_9			–	100	–	nA
Discharge Impedance	DR_9			1.0	1.4	1.8	kΩ
Free Running Line Period	FLP1		R = 34.9kΩ to $V_{cc}1$, C = 2.2nF to GND	62	64	66	µs
	FLP2		R = 13.7kΩ, C = 2.2nF	–	27	–	µs
Oscilator Threshold for Line Output Pulse Triggering	OT_9			–	4.6	–	V
Horizontal Frequency Drift ^{W}/Temperature	$\frac{DF}{\Delta\Theta}$			–	2	–	Hz/°C
Saturation Voltage	LV_{14}	@ Pin14	I_{14} = 200mA	–	1.1	1.6	V
Output Pulse Width	OPW		Line Period = 64µs	20	22	24	µs
Bias Voltage	V_{11}	@ Pin11		1.8	2.4	3.2	V
Input Impedance	Z_{11}			4.5	5.8	8.0	kΩ
Output Current During Synchro Pulse	I_{10}	@ Pin10		250	450	800	µA
Current Ratio	RI_{10}		Positive/Negative	0.95	1.0	1.05	
Leakage Current	LI_{10}			–2	–	+2	µA
Control Range Voltage	CV_{10}			2.6	–	7.1	V
Low Threshold Voltage	LT_1	@ Pin1		1.6	2.0	2.3	V
High Threshold Voltage	HT_1			2.6	3.1	3.6	V
Bias Current	BI_1			–	30	–	nA
Discharge Impedance	DR_1			300	470	700	W
Free Running Frame Period	FFP1	@ Pin1	R = 845kΩ to $V_{cc}1$, C = 180nF to GND	20.5	23.0	25.0	ms
Minimum Frame Period	MFP		I_{15} = –100µA, R = 845kΩ to $V_{cc}1$, C = 180nF to GND	–	12.8	–	ms
Free Running Frame Period	FFP2		R = 408kΩ, C = 220nF	–	14.3	–	ms
Frame Period Ratio	FPR		Note 1	1.7	1.8	1.9	
Frame Sawtooth Gain	FG		Between Pin1 and Non–Inverting input of the Frame Amplifier	–	–0.4	–	
Vertical Frequency Drift ^{W}/Temperature	$\frac{DF}{\Delta\Theta}$	@ Pin1		–	4.1^{-3}	–	Hz/°C
Operating Voltage	V_7	@ Pin7	^{W}/Flyback Generator	10	–	58	V

Note 1. Frame Period Ratio = $\frac{FFP}{MFP}$

Electrical Characteristics (Cont'd): (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Supply Current	I_7	@ Pin7	V_7 = 30V	–	–	22	mA
Operating Voltage	V_2	@ Pin2		10	–	30	V
Saturation Voltage to GND	LV_{8A}	@ Pin8	V_7 = 80V, I_8 = 0.1A	–	0.06	0.6	V
	LV_{8B}		V_7 = 80V, I_8 = 1A	–	0.37	1.0	V
Saturation Voltage to V_7	HV_{8A}		V_7 = 30V, I_8 = –0.1A	–	1.3	1.6	V
	HV_{8B}		V_7 = 30V, I_8 = –1A	–	1.7	2.4	V
Saturation Voltage to V_7 in Flyback Mode	FV_{8A}		$V_8 > V_7$, I_8 = 0.1A	–	1.6	2.1	V
	FV_{8B}		$V_8 > V_7$, I_8 = 1A	–	2.5	4.5	V
Flyback Transistor ON (Output = High State)	F_{2DA}	@ Pin2 & Pin3, V_2 = 30V	$V_{2/3}$ with $I_3 \rightarrow_2$ = 0.1A	–	1.5	2.1	V
	F_{2DB}		$V_{2/3}$ with $I_3 \rightarrow_2$ = 1A	–	3.0	4.5	V
	FSVA		$V_{3/2}$ with $I_2 \rightarrow_3$ = 0.1A	–	0.8	1.1	V
	FSVB		$V_{3/2}$ with $I_2 \rightarrow_3$ = 0.1A	–	2.2	4.5	V
Flyback Transistor OFF (Output = $V_7 – V_8$)	FCI	@ Pin2 & Pin3	$V_7 = V_2$ = 30V, Leakage Current Pin2	–	–	170	µA

Note 1. Frame Period Ratio = $\frac{FFP}{MFP}$

Application Notes:

The NTE1888 performs all the video and power functions required to provide signals for the direct drive of the line darlington and frame yoke. It contains:

- A shunt regulator
- A synchronization separator
- An integrated frame separator without external components
- A saw–tooth generator for the frame
- A power amplifier for direct drive of frame yoke (short circuit protected)
- An open collector output for the line darlington drive
- A line phase detector and a voltage control oscillator

Synchronization Separator

The slice level of sync separation is fixed by the value of external resistors controlled by an internally fixed voltage.

Frame Separator

The sync–pulse allows the discharge of the external capacitor by a 2 x I current. Capacitor discharge is held by $V_Z/2$, and a frame sync pulse permits the complete discharge of the capcitor to provide current for the other parts of the circuit.

Line Oscillator

The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on a internal resistor.

Phase Comparator

The sync–pulse drives the current in the comparator. The line flyback integrated by the external network gives a sawtooth on Pin11. The comparator output provides a positive current for the part of the signal on Pin11 greater than V_{CC} and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternatively negative and positive current. The frame sync–pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning.

Application Notes (Cont'd):

Line Output (Pin14)

It is an open collector output which is able to drive a pulse current of 800mA for a rapid discharging of the darlington base. The output pulse time is 22µs for a 64µs period.

Frame Oscillator

The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last half free run period. The input current during the charge of the capacitor is less than 100nA.

Frame Output Amplifier

This amplifier is able to directly drive the frame yoke. Its output is short circuit and overload protected; it contains also thermal protection

Pin Connection Diagram