
ON-CHIP DEBUGGER SPECIFICATION

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On-Chip Debugger Specification

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On-Chip Debugger Specification

Chapter 1. Overview

1.1 Introduction

This chapter provides an overview of the on-chip debugger.



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1.2 Highlights

Topics covered in this chapter are:

- On-Chip Debugger Definition
- Debugger vs. Emulator

1.3 On-Chip Debugger Definition

An on-chip debugger is special hardware and software that works with specific PICmicro[®] devices to give developers a low cost method for debugging their code. These PICmicro MCU's must (1) contain special on-chip logic supporting debugging functionality and (2) provide In-Circuit Serial Programming[™] (ICSP[™]) capabilities.

The ICSP capability allows in-circuit programming of the PICmicro MCU via specific hardware pins designated for this purpose. ICSP is described in detail in the *In-Circuit Serial Programming (ICSP) Guide (DS30277)*. Additionally, ICSP-related technical briefs and application notes, as well as device programming specifications, may be found at our website (www.microchip.com).

The on-chip debug capability provides breakpointing, single stepping, and external breaking. Breaks are treated as a special form of interrupt that vector to debug executive software implemented by the developer. The same hardware pins used by the ICSP capability are preserved by the on-chip debug capability while servicing the debug break, allowing them to be used to implement communications between the debug executive software and a host processor.

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1.4 Debugger vs. Emulator

Traditionally, embedded systems engineers use in-circuit emulators (ICE) to develop and debug their designs. The on-chip debug facilities in some PICmicro devices provide a low cost alternative to a more expensive ICE.

When implemented, the on-chip debugger logic is part of the actual microcontroller silicon. As a result, there is a trade-off between the cost of producing this silicon on every chip (even though only a few will actually use this logic) and the power of the logic itself. It would be possible to put an entire emulator with complex breakpoints and tracing capabilities on a chip, but the cost would be prohibitively high. Usually the on-chip debugger provides the means to set simple breakpoints, query the internal state of the chip, and single step through code.

A microcontroller utilizing its on-chip debug facilities has these benefits:

- Low cost
- Requires a minimum of extra hardware
- Does not require expensive sockets or adapters
- Able to debug a production line board

In order to have the above benefits, on-chip debuggers have these trade-offs compared to ICEs:

- Use of some target system resources such as pins, program and/or data memory, and stack space may mean that some portions of an embedded application cannot be debugged.
- Triggering and breakpointing are limited to the capabilities of the on-chip debug silicon.
- The target chip must actually be running with a clock and a supply voltage. Often an emulator probe can run without any external hardware.

Overall, an in-circuit emulator usually provides the most powerful debugging solution, but as chips get faster and more complex, emulators require increasingly expensive high speed logic and high priced adapters to connect to the denser chip packages.

Chapter 2. PIC16F87X Debugger Control

2.1 Introduction

This chapter describes the hardware and software requirements for on-chip debugging using the PIC16F87X.

2.2 Highlights

Topics covered in this chapter are:

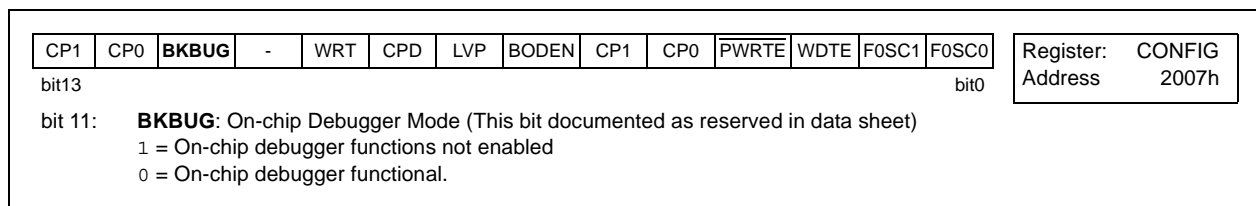
- Enabling/Disabling the On-Chip Debugger
- Using the On-Chip Debugger Registers
- Communicating with the Target Device
- Resetting and Running Programs
- Halting Execution
- Additional Considerations

2.3 Enabling/Disabling the On-Chip Debugger

The configuration bit **BKBUG** (bit 11 in the configuration word) is used to enable/disable the on-chip debugger (Figure 2.1).

See the programming specifications for PIC16C87X devices (DS39025) for more information on programming the configuration word.

Figure 2.1: CONFIGURATION WORD



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2.4 Using the On-Chip Debugger Registers

There are two registers associated with debugger control: the `ICKBUG` and `BIGBUG` registers (Figure 2.2 and Figure 2.3.) Between these two registers, there are 3 bits for debugger control and 13 bits for breakpoint address specification.

INBUG - Set/cleared automatically when entering/exiting debug executive. A four (4) instruction cycle delay will prevent the new state of zero from being recognized by the core to allow a safe debugger exit. When set, interrupts are disabled (regardless of the state of the `GIE` bit) and the debugger `HALT` is disabled. This prevents reentry into the debugger while communicating with computer software.

FREEZ - When `FREEZ` is set, `TMR0`, `TMR1` and `TMR2` and their prescalers freeze at a break (suspend counting). The `SSP`, `A/D` converter and `USART` state machines will also suspend upon the assertion of the `FREEZ` bit. Status flag bits that are altered by register read operations are unaffected while `FREEZ` is asserted.

SSTEP - Enables single step operation. After a return to normal operation (`INBUG=0`), if `SSTEP` is set, the on-chip logic will allow one user instruction to execute before the on-chip debugger is reentered.

BKAnn - Break address `nn`. These bits are cleared at POR. No other reset clears the bits, (i.e., a `MCLR` cannot change the breakpoint address value).

Figure 2.2: ICKBUG Register (Address 18Eh)

	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INBUG	FREEZ	SSTEP	BKA12	BKA11	BKA10	BKA09	BKA08
bit7								bit0
bit 7:	INBUG: On-chip debugger activity status 1 = Device is executing on-chip debugger code 0 = Device is executing user code (This bit is read only; set from on-chip halt or breakpoint occurrence; only clear by RETURN)							
bit 6:	FREEZ: on-chip debugger freeze mode 1 = Peripherals will freeze when <code>INBUG=1</code> 0 = Peripherals will not freeze when <code>INBUG=1</code>							
bit 5:	SSTEP: Single Step Enable 1 = Program will execute 1 instruction word of user code upon RETURN from debug code 0 = Program will execute multiple instruction words of user code							
bit 4-0:	BKA: Breakpoint Address When writing, represents the requested breakpoint address. When reading, represents the value of the PC at last breakpoint, halt, or single step operation.							

R = Readable bit
 W = Writable bit
 U = Unimplemented bit, read as '0'
 - n = Value at POR reset

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Figure 2.3: BIGBUG Register (Address 18Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BKA07	BKA06	BKA05	BKA04	BKA03	BKA02	BKA01	BKA00

bit7 bit0

bit 7-0: **BKA**: Breakpoint Address
When writing, represents the requested breakpoint address.
When reading, represents the value of the PC at last breakpoint, halt, or single step operation.

R = Readable bit
W = Writable bit
U = Unimplemented bit,
read as '0'
- n = Value at POR reset

2.5 Communicating with the Target Device

The debug executive establishes the communication channel between the target device (RB<7:6>) and computer software (e.g., MPLAB IDE.)

Since the debugger will issue read-modify-write instructions (BSF, BCF) on PORTB for communication with the debugger interface module, addresses 0x106 and 0x186 should be used to modify PORTB<7:6> and TRISB<7:6> so that bits <5:0> are not corrupted. If the user requests a read or a write of PORTB or TRISB, addresses 0x006 and 0x086 can be used to access the RB<5:0> portions of the register.

2.6 Resetting and Running Programs

In the debug environment, the target device reset pin can be activated by the module/target connector or by the target system resources. After reset, the target device will begin running the target program. To begin debugger execution, initiate a hardware halt (on I/O pin.)

Note: A hardware halt after reset will execute location 0x0000 and then skip to 0x0001. Therefore, a NOP is recommended at location 0x0000.

2.7 Halting Execution

If BKBUG is programmed to 0, the INBUG flag is clear, and a halt signal occurs, normal program execution is halted and the on-chip debugger is entered. A halt signal will be generated when either:

- RB6 transitions from high to low
- the current PC value matches the value of BKA<12:0>
- the SSTEP bit is set

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When normal program execution is halted, the current instruction will be executed and then the program will be stopped at the address of the next instruction. The processor will go through what appears to be a normal interrupt cycle, except it will not disturb the contents of the `GIE` bit. On-chip debugger logic will control sequencing of the key interrupt signals in the core logic.

Once in debug mode, the `INBUG` flag is set. The PC is pushed onto the stack and stored in `BKAnn`. This allows proper reporting of the current state of the PC (next instruction to be executed) when the on-chip debugger is entered. The PC is then set to `0x2004`.

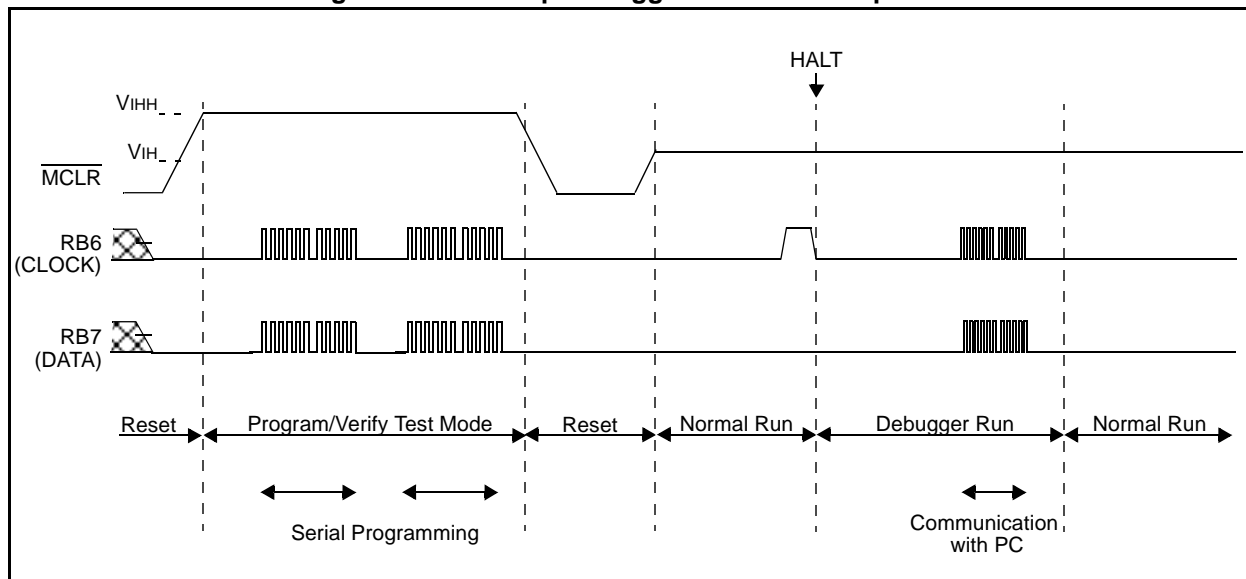
As the processor vectors to `0x2004`, the CPU will fetch and execute the instruction at this address. Therefore, address 2004 must be programmed with a `GOTO` opcode, where `opcode` is pointing to the beginning address of the debug code. Then the on-chip debugger routine will commence. `PCLATH` will be undisturbed, and the PC at breakpoint is at the top of the stack.

The debugger software will use a `RETURN` instruction to return to the mainline code. The `RETURN` will cause the `INBUG` bit to be cleared and will also release peripheral freeze at the proper time, if the `FREEZ` bit had been set.

2.7.1 Halting Execution by I/O Pin

For the conditions specified in Section 2.7, an edge detection circuit will generate a `HALT` signal pulse when `RB6` transitions from high to low. This is also known as external or hardware halting.

Figure 2.4: On-chip Debugger Execution Sequence



2.7.2 Halting Execution by Address Breakpoint

For the conditions specified in Section 2.7, another HALT method is by address breakpoint. The `ICKBUG` and `BIGBUG` registers contain a 13-bit value (`BKAnn`) that is compared against the current PC value. When the values are equal, then the circuit will generate a halt signal on that cycle.

Power-up initializations the state of the `ICKBUG` and `BIGBUG` registers to `0x0000`, equal to the reset vector.

Note: A hardware halt after reset will execute location `0x0000` and then skip to `0x0001`. Therefore, a `NOP` is recommended at location `0x0000`.

Disabling the breakpoints is implemented by setting a breakpoint address that lies in the address space of the on-chip debugger (ex: `0x1F00`.)

2.7.3 Halting Execution by Single Stepping

For the conditions specified in Section 2.7, another HALT method is by single step. Upon exit of the debug routine by the `return` instruction, if the `SSTEP` bit is set, the on-chip debugger logic will generate a HALT signal timed to allow one instruction execution. After this, the device will reenter the on-chip debugger routine in the same fashion as the external (I/O pin) halt.

2.8 Additional Considerations

In addition to the logic required to support the on-chip debugger as described in the above sections, there are several issues of which to be aware.

- Watchdog Timer will still be functional with no special modes associated with on-chip debugger.
- The reset, POR and BOR logic will still be functional with no special modes associated with the on-chip debugger.

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