Notes on using Analog Devices' DSP, audio, & video components from the Computer Products Division
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HOW TO USE AD1819A VARIABLE SAMPLE RATE SUPPORT

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Overview

This Engineer's Note will cover the AD1819A's variable sample rate support. One advantage the AD1819A has over other AC `97 codecs is that it can support any sample rate between 7 kHz and 48 kHz with one Hz precision. Two different sample rates may be used, and either may be assigned to any of the four converter channels in the AD1819A. In addition, one of the sample rates may be multiplied by a constant factor of 10/7 or 8/7 for generation of irrational sample rates used in V.34 modems. The variable sample rate support in the AD1819A eliminates the burden of digital re-sampling imposed on DC `97 controllers by the AC `97 specification, without any loss in audio performance.

REGISTERS

Four vendor-defined registers in the AD1819A control its pair of sample rate generators (SRGs). Two (78h and 7Ah) contain the sample rates to be generated. Another (76h) assigns one of the two sample rates to each conversion channel, and enables the 10/7 or 8/7 multipliers for modem support. The last (74h) enables DAC request
bits, which are required for proper transfer of DAC data at sample rates less than the 48 kHz serial frame rate.

Sample Rate registers

Registers 78h and 7Ah contain the sample rates currently assigned to each SRG in Hz. Behavior of the SRGs is undefined if sample rates less than 7 kHz (1B58h) or greater than the default rate of 48 kHz (BB80h) are used. Sample rate changes take effect immediately after either register is written.

Miscellaneous Control Bits Register

Register 76h contains four bits which assign one of the two SRGs (Sample Rate Generators) to each conversion channel, and two bits to enable the 10/7 or 8/7 multipliers for irrational modem rates.

Bit	Name	Description
0	ARSR	ADC right sample rate generator select
2	DRSR	DAC right sample rate generator select
5	SRX8D7	multiply SR1 rate by 8/7
6	SRX10D7	multiply SR1 rate by 10/7
8	ALSR	ADC left sample rate generator select
10	DLSR	DAC left sample rate generator select

Other bits are reserved or used for other purposes, so this register should be read, the result modified as necessary, and then written back.

If the *ALSR*, *ARSR*, *DLSR*, or *DRSR* bits are zero then the corresponding converter channels are assigned to *SRG0*, and use the sample rate in
register 78h. If any of those bits are ones then corresponding channels are assigned to SRG1, and use the sample rate in register 7Ah. The default state of all of these bits is zero in the AD1819A,
but that may change in later parts. Hence, software should always set these bits instead of assuming they are reset to a fixed value.

If the *SRX8D7* or *SRX10D7* bits are set then the sample rate generated by *SRG1* is multiplied by a constant factor of 8/7 or 10/7, respectively. The rate generated by *SRG0* is unaffected by these bits. The result is undefined if both bits are set. Care must be taken to ensure that neither the base sample rate (if both *SRX* bits are clear) nor the multiplied sample rate (if one of the *SRX* bits is set) are ever outside of the allowed 7 kHz to 48 kHz range; this should not be a problem for any of the V.34 irrational rates.

Serial Configuration register

Register 74h contains one bit to enable DAC requests, and six *read-only* bits for the DAC request bits themselves.

Bit	Name	Description
0	DRRQ0	Master codec DAC right request
1	DRRQ1	Slave 1 codec DAC right request
2	DRRQ2	Slave 2 codec DAC right request
8	DLRQ0	Master codec DAC left request
9	DLRQ1	Slave 1 codec DAC left request

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10	*DLRQ2*	*Slave 2 codec DAC left request*
11	*DRQEN*	*Enable DAC requests in serial frame*

Other bits are reserved or used for other purposes, so this register should be read, the result modified as necessary, and then written back. If there is only one codec in the system then it is the master codec; multi-codec systems are covered elsewhere.

DAC request bits are asserted whenever the associated DAC channel is able to accept data in the next serial frame. This information is required because it is possible to provide more samples to a DAC channel than it can accept when the DAC channel is running at a rate less than the serial frame rate of 48 kHz. If a DAC request bit is deasserted then the controller should not send a DAC sample for that channel in the next frame.

If the DRQEN bit is set then the AD1819A produces DAC request bits at two different points in the input serial frame. Those two points are in the bottom half of the status address slot, and in the status data slot.

The DAC request bits in the status address slot are compatible with the recently released AC `97 2.0 extensions. They are active-low (send sample if zero), and are output in the same order as the output slots for the corresponding DAC channels.

Slot	*Bit*	*SDATA_IN*	*Controls slot*
1	*19*	*0*	
1	*18:12*	*status address*	
1	*11*	*DLRQ0#*	*3*
1	*10*	*DRRQ0#*	*4*
1	*9*	*DLRQ1#*	*5*
1	*8*	*DRRQ1#*	*6*
1	*7*	*DLRQ2#*	*7*
1	*6*	*DRRQ2#*	*8*
1	*5:0*	*0*	

DAC requests are also produced in the status address and data slots by emulating register reads of register 74h. Once DRQEN is set, every input frame (except those following an output frame containing a read command) will contain 74h in the status address slot and the contents of register 74h in the status data slot. This mode is provided for use with controllers that cannot propagate data from the low half of the status address slot. It is preferable to use the DAC request bits from the status address slot instead of those from the status data slot, because the latter are obscured whenever a real register read command is issued.

DIFFERENCES BETWEEN THE AD1819A AND AC `97 2.0

Many features of the AC `97 2.0 variable sample rate extensions are based on features introduced by Analog Devices in the AD1819A, but there are some differences with which systems using the AD1819A must cope.

First is the sample rate registers themselves. The AD1819A's sample rate registers are at indices 78h and 7Ah instead of at 2Ch through 34h, and there is no fixed mapping of converter channels to SRGs. Also, the AD1819A relies on the user not to write sample rates outside of the acceptable range to the sample rate registers; AC `97 2.0 codecs handle invalid settings by forcing the register to the nearest acceptable value.

AC `97 2.0 codecs require that a bit (VRA, register 2Ah) be set before sample rates may be changed, while the AD1819A's variable sample rate support is always enabled. VRA also enables DAC request bits in the status address slot on AC `97 2.0 codecs, while the AD1819A uses the DRQEN bit in register 74h to enable DAC requests in both the status address and status data slots.

Future AC `97 codecs from Analog Devices will comply with the AC `97 2.0 variable sample rate extensions, while retaining as much compatibility with the AD1819A as possible.

SYNCHRONIZATION OF AUDIO DATA

Some controllers or applications require that all stereo ADC or DAC samples be delivered in (left, right) pairs. The AD1819A will deliver ADC samples and DAC requests in pairs as long as some simple rules are followed.

The ADCs will deliver samples in pairs as long as both ADC channels are assigned to the same SRG (ALSR = ARSR in register 76h) and loopback mode is disabled (LPBK = 0 in register 20h). The ADCs must be powered down and back up again whenever ALSR and ARSR are changed or LPBK is cleared in order to guarantee that samples will be delivered in pairs.

DAC requests will be issued in pairs as long as both DAC channels are assigned to the same SRG (DLSR = DRSR in register 76h), loopback mode

is disabled (LPBK = 0 in register 20h), and DAC samples are delivered in pairs. The DACs must be powered down and up again whenever DLSR
and DRSR are changed or LPBK is cleared in order to guarantee that DAC requests will be delivered in pairs.

Power cycling the ADCs or DACs is unnecessary if they are powered down when the changes are made; the altered settings will take effect when the converters are next powered up.