Notes

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Introduction

This document is intended to assist customers in using IDT77V7101, which is a complete 1.25Gbps Ethernet Serializer/Deserializer (SERDES) transceiver in a single IC and is compatible with IEEE 802.3z Gigabit Ethernet Standard. This part is designed to provide the Physical Medium Attachment (PMA) portion of the IEEE 802.3z PHY layer. The IDT77V7101 is +3.3V part available in 10x10mm and 14x14mm PQFP package. The transmitter is designed to serialize a 8b/10b encoded 10bit wide word and transmit it across either cable or to an external fiber optic transceiver. The receiver takes the serialized data and reconstructs the 10bit parallel word. The transceiver contains all the necessary high frequency circuitry, PLL, multiplexer, demultiplexer, clock and data recovery circuitry, cable driver and equalizer. This application note will help customers to get the best possible performance from the IC and ensure first time success in implementing a functional design with optimal signal quality. It is intended that this document will be used in conjunction with the product Data Sheet. An elementary knowledge of high-speed printed circuit layout techniques is assumed. Details concerning PCB layout and differential impedance design are provided. The critical issues of controlled impedance of traces and connectors, differential routing, termination techniques, and DC balance must all be considered to get the best performance from the IC.

Differential Impedance Design

The high speed interconnects of SERDES are differential signals so these traces should be designed as differential pair. These signals have very fast rise/fall times on the order of pico seconds, so these interconnects should be treated as transmission lines rather than simple wire connections. The characteristics of transmission lines determine the layout practice. One of the fundamental properties of a transmission line (a mathematical model for a trace on a PCB with power/ground planes) is characteristic impedance, Zo. For a single line, Zo is the number that represents the ratio of voltage to current traveling in each direction on the line. The characteristic impedance of the transmission line is determined by the relative dielectric constant of the PC board material, thickness of the dielectric, and the width of the transmission line. The impedance is also affected when the thickness of the copper strip becomes significant compared to the thickness of the dielectric, which is height to the plane. For a single line configuration, relatively simple closed form equations exist that give fairly accurate impedance. The best method for calculating the impedance, however, is to use a field solver, which is a program that uses fundamental electromagnetic theory (Maxwell's equations) to calculate impedances and other parameters. Typically, high end signal integrity software includes a field solver. The most common mistake while terminating the differential pair is not to account for mutual coupling in differential pairs. Mutual coupling lowers the differential impedance. If the termination is not correct, the result will be increased reflections and noise. When differential pairs are designed as transmission line, Zo for each trace in the pair is no longer a single number, but it is now a 2x2 matrix because of the coupling present between traces. Differential impedance is the value of the line-to-line resistor that will optimally terminate pure differential signals.

Designing a Differential Pair

- Selection of transmission line geometry is the first step. There are many ways of designing a transmission line for differential pairs. The broadside coupled differential pair geometry, also known as Over Under, gives very strong coupling between traces, but it is not recommended because it requires extra layers and there are layer registration issues in manufacturing. The stackup thickness is hard to control for different builds, which results in variation of differential impedance. The edge side coupled differential pair geometry, also known as side-to-side, designed for Microstrip or Stripline configurations will control impedance and avoid adjacent layer coupling with the use of

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solid ground planes.

- The target differential impedance should be determined based on the specific application. For backplane application, the differential pairs should be designed to match the differential impedance specified for the connector.
- Determine target layer impedance for net without coupling, using nominal width and stackup. Nominal uncoupled trace impedance should be about 5 to 10ohms higher than one half of the desired differential impedance.
- Compute the differential impedance.
- Adjust the spacing and reroute until the proper differential impedance is achieved OR adjust the trace width and reroute until the proper differential impedance is achieved.

Differential Impedance Design Example

The stackup shown in Figure 1 will be used to demonstrate some parameters that affect the impedance of the board while designing transmission lines. It is shown in the eight-layer stackup that 12mil of trace on the top layer will achieve around 53.4ohms of impedance when separated by a dielectric of 7mils from the plane. It is also shown that 7mil of trace on an internal signal layer will achieve 50.1ohms of impedance when separated by 8mils of dielectric on both sides. These parameters are taken from the Hyperlynx Signal Integrity Line SIM tool. During the design of differential transmission lines, both traces have to be coupled, weakly coupled or strongly coupled. Coupling will depend on the distance between two traces forming a differential transmission line.

Figure 2 represents the coupled transmission line created for modeling 100ohm Microstrip edge coupled differential transmission line. Figure 3 represents the parameters for achieving 100ohm of differential impedance. If both of these 53.4 ohms of characteristic impedance Microstrip transmission lines are separated by 15mils on top layer, then the resulting differential Impedance between these lines will be 99.8ohms +/- 10%.

Figure 4 represents the parameters for achieving 100ohm of differential impedance for Stripline edge coupled differential transmission line. If both of these 50.1 ohms of characteristic impedance Stripline transmission lines are separated by 15mils on internal layer, then the resulting differential Impedance between these lines will be 99.1ohms +/- 10%.

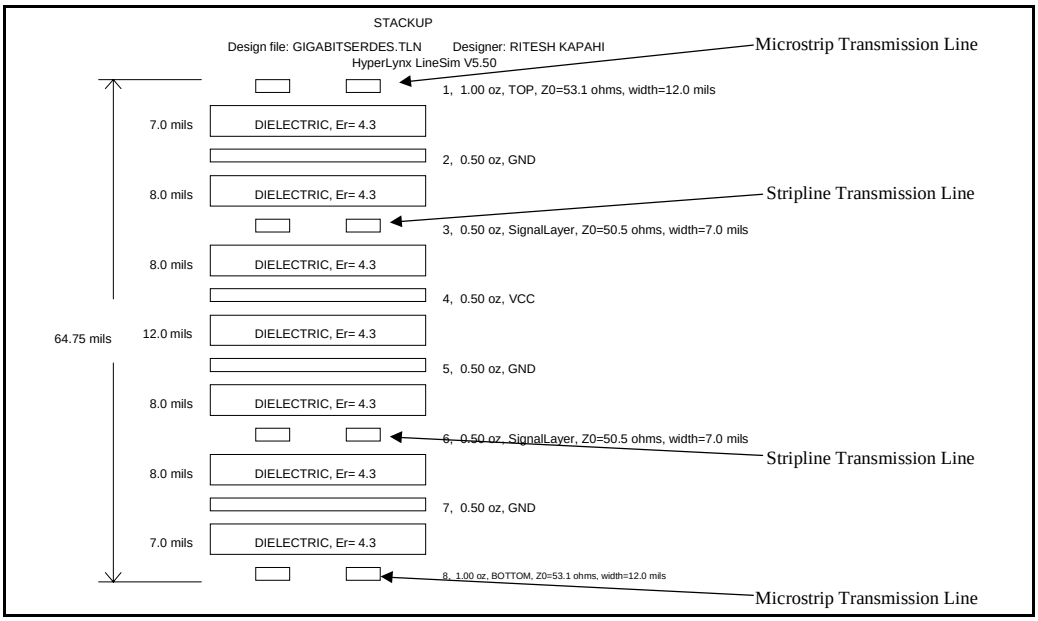

Figure 1 Board Stackup for eight layers

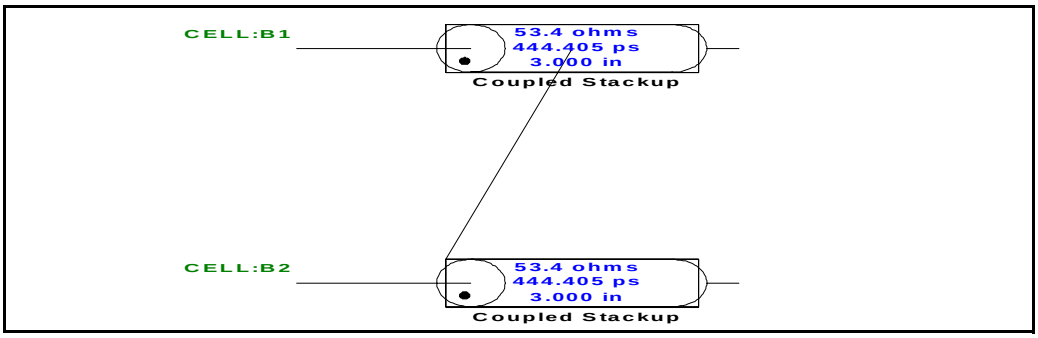

Figure 2 Weakly Coupled Transmission Line for Microstrip Differential Transmission Line

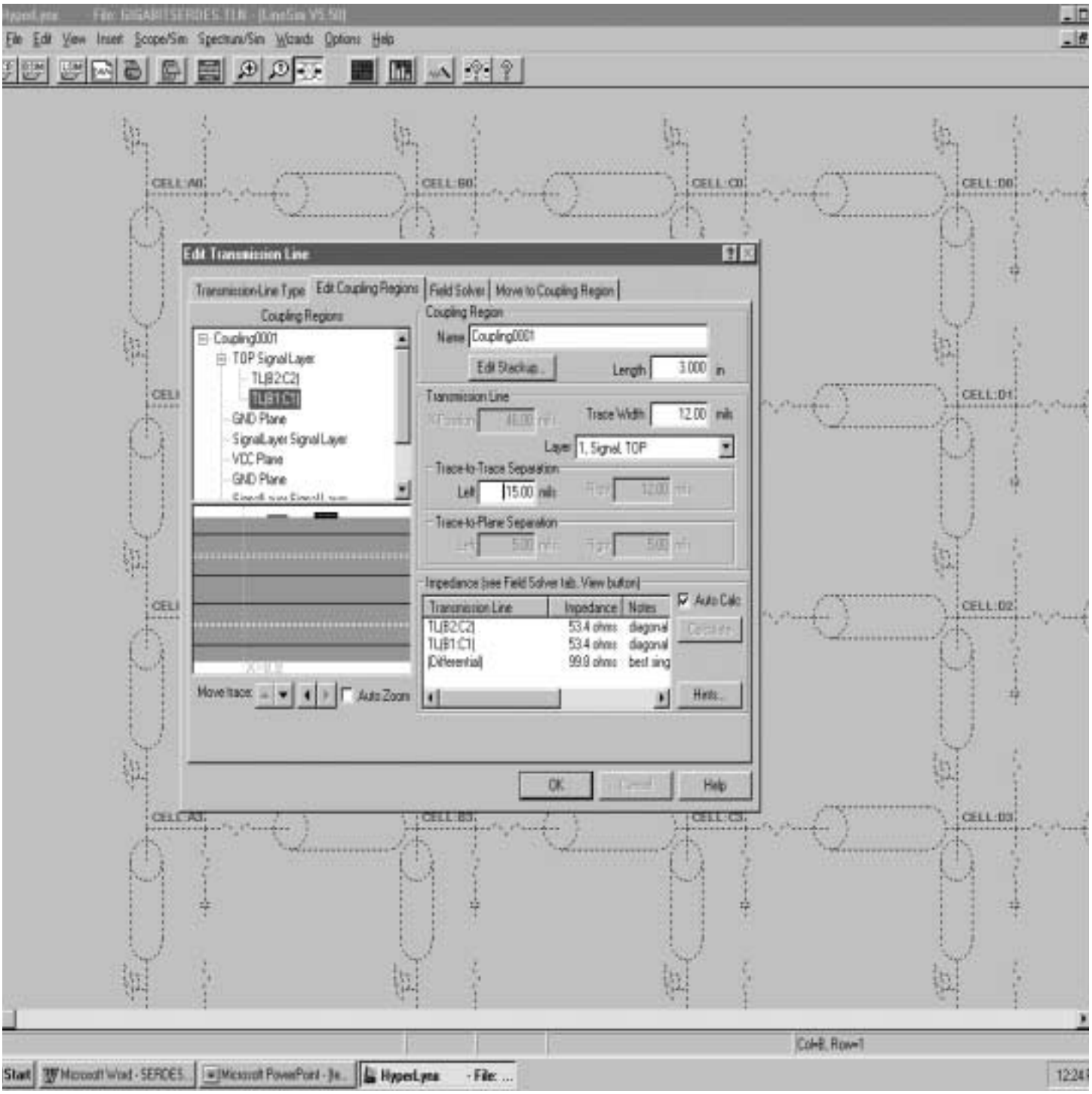

Figure 3 100ohm Microstrip Edge Coupled Differential Transmission Line

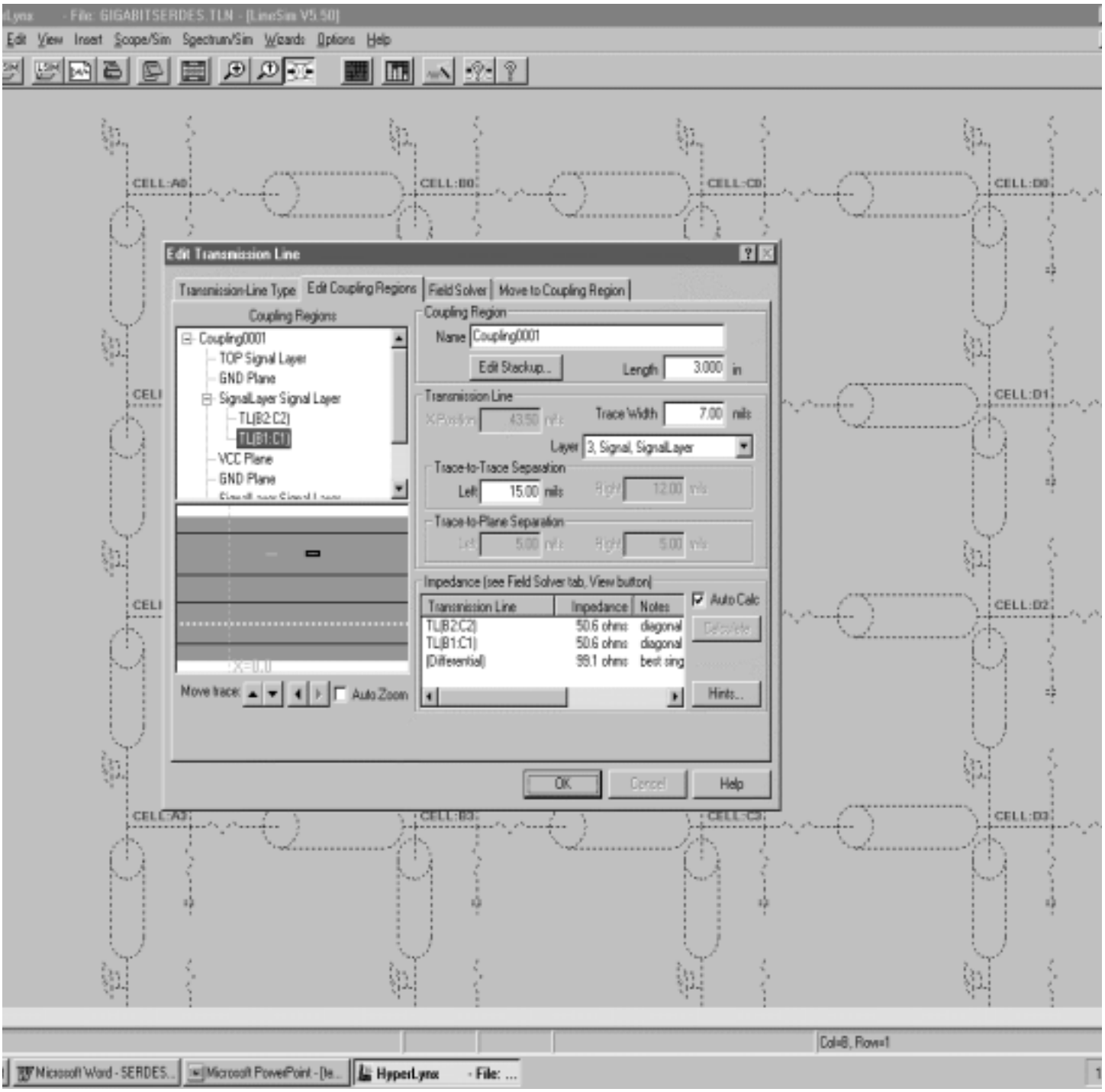

Figure 4 100 ohm Stripline Edge Coupled Differential Transmission Line

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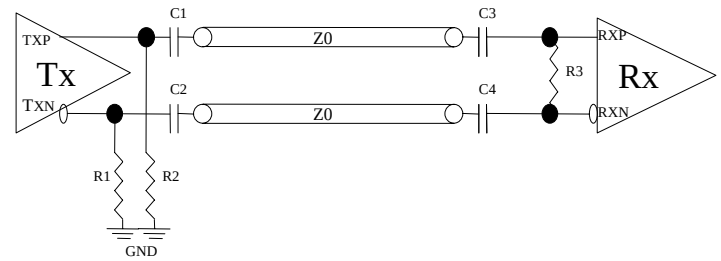
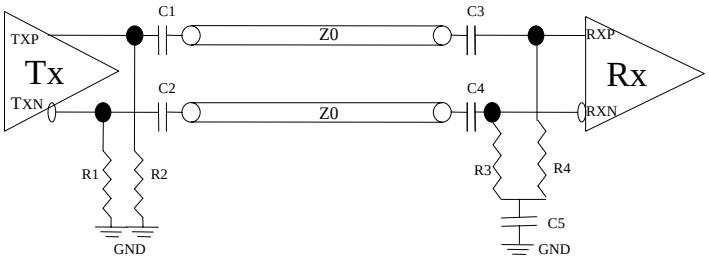
High-Speed I/O Interface

The high-speed serial lines are Positive ECL (PECL) output voltage swings and these are designed to be AC Coupled. The high-speed serial connections are shown in Figure 5. Resistors R1 and R2 (150 ohms) set the DC bias current through TXP/TXN. The value of R3 and R4 depends on the transmission line that the transmitter drives. If the transmission lines are designed for 100ohm differential impedance, then a single differential termination resistor of 115ohms can be used to achieve 100ohms of differential impedance, as there is 714ohms of DC impedance present between the RXP and RXN internal to the chip because of internal biasing. If the transmission lines are designed for 150ohm differential impedance, then a single differential termination resistor of 191 ohms can be used.



High Speed Tx tp Rx Connection using single termination resistor

R1 = R2 = 50 ohms C1 = C2 = C3 = C4 = 0.01uF
R3 = 115 ohms for 100 ohm Differential Termination (714 || 115) = 100
R3 = 191 ohms for 150 ohm Differential Termination (714 || 191) = 150



High Speed Tx tp Rx Connection using single termination resistor

R1 = R2 = 50 ohms C1 = C2 = C3 = C4 = C5 = 0.01uF
R3 = R4 = 57 - 59 ohms for 100 ohm Differential Termination
R3 = R4 = 95 - 97 ohms for 150 ohm Differential Termination

Figure 5 High-speed I/O Interconnection showing Differential Termination

Design and Layout Consideration for SERDES

Proper PCB layout is important in order to minimize parasitic capacitance and inductance, which can cause ringing and poor VSWR match on the high-speed serial lines. When implementing a 1.25Gb/s serial communications link, the importance of layout cannot be overstressed. However, following general simple-to-use guidelines will increase the chances of success and prove easier than most designers anticipate. The prioritization of signals is as follows:

- High speed serial I/O lines
- Transmit Clock
- Power Supply & Bypass Capacitors
- Data buses

Careful placement of components and the use of passives on both the top and bottom side will generally ensure optimal layout. A solid ground plane and power plane are quite useful in distributing clean power and providing buried capacitance with no inductance which is essential for the high speed designs. A useful in-depth analysis of design and layout techniques is "High-Speed Digital Design: A Handbook of Black Magic" by Dr. Howard Johnson and Martin Graham, Prentice Hall, ISBN 0-13-395724-1.

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High Speed Serial I/O Design and Layout Considerations

SERDES signals contain digital data at frequencies between 125MHz to 625MHz and require excellent frequency and phase response up to at least the 3rd harmonic. Improved signal quality and longer practical transmission distances will result if the designer follows the general rules below.

- The board design should be a controlled impedance board design for the high-speed signals of SERDES. The high-speed signal traces should be designed for desired differential impedance. The design engineer should work very closely with the fabrication house to get the board material thickness, so that he can use these parameters to decide on the thickness and width of traces to get the desired impedance on the board.
- Keep traces as short as possible. Initial component placement must be carefully considered. Eliminate/reduce stub lengths.
- Impedance matching termination resistors (i.e. 115ohm for 100ohm differential termination) should be located as close as possible to the input pin of the receiver in order to minimize stub length. On the receiver, placing the termination resistors at the end of trace about 0.25" beyond the package pin provides a high quality, feed-through termination. Do not group all the passive components together. Bunching of passive components results in impedance discontinuities due to the capacitance of pads which, at the frequencies encountered in Gigabit Ethernet, results in unwanted reductions in impedance. Using surface mount 0603 components reduces this effect. The layout of the high-speed serial lines for the receive interface is shown in Figure 6.
- The impedance of the traces running on the backplane and the cards connected to the backplane must match that of termination resistors and connectors in order to reduce reflections due to impedance mismatches.
- The differential pair traces should be kept on the same side and on the same layer of the PCB to minimize impedance discontinuities. Both the signals in pair should also have equal number of vias. However, you may try implementing the pairs with no vias for backplane applications, since the signals already have two drill holes because of connectors in the path. The recommended layout for the device for the high-speed serial interface with no vias is shown in Figure 6.
- While routing the differential pairs, keep the trace length identical between the two traces. Differences in trace length directly translate into signal skew. In differential mode, the signals travel in opposite direction, also known as odd mode (i.e., two current directions so there is noise cancellation due to coupled complementary fields). The field cancellation of differential signals reduces far field emissions. Differential skew is the only source of emissions, so controlling skew through routing is key to reduced EMI levels.
- It is recommended to route the differential pair as strongly coupled transmission lines. Any mutual coupling will increase the common mode impedance and decrease the differential impedance. If tighter coupling is desired, the differential impedance must be calculated rather than assuming the impedance is twice the single-ended impedance with the help of at least two dimensional field solvers. For a differential transmission line with the pairs spaced far apart electrically (weak coupling), the mutual coupling will approach zero. Differential impedance must be maintained in Zd ohm differential application. Routing two Zd/2 ohm traces is not adequate. The two traces must be separated by enough distance to maintain Zd ohm differential impedance. A good rule of thumb is that the trace separation should be at least 2.5 times the trace width while implementing a differential pair with weak coupling.
- Reduce, if not eliminate, the number of vias to minimize impedance discontinuities. Remember that vias and their clearance holes in power/ground planes can cause impedance discontinuities in nearby signals. Keep vias away from traces by 2.5 times the trace width as minimum.
- Use surface mounted components for lower lead inductance and capacitance. Smaller form factor components are best (i.e., 0603 is better than 0805).
- Use rounded corners rather than 90 degree or 45 degree corners.
- Use the Power/Ground planes as an effective power supply bypass capacitor. The capacitance is proportional to the area of the two planes and inversely proportional to the distance of the two planes. Typical values with a 0.01" separation are 100pF/inch square. This capacitance is more

effective than capacitor of equivalent value because the planes have no inductance or ESR (Equivalent series resistance).

- Keep high-speed signal traces far from other signals which might capacitively couple noise into the signals. A good rule of thumb is that "far" means tens times the width of the trace.
- Do not route the digital signals from other circuits across the area of the transmitter and receiver.
- Place vias and clearances to maintain the integrity of the plane. Return current of vias spaced closely together often overlap clearances, forming a large hole in the plane. Return currents are forced around the holes, increasing the loop area and resulting in more EMI emissions. This is a common error while routing 10bit or 20bit buses between chips, where the PCB designer often places all the vias for the bus together.
- The use of grounded guarded traces is generally not effective at important signal quality. A ground plane is more effective. However, a common use of guard traces is to route them during the layout but remove them prior to design completion. This has the benefit of enforcing "Keep Out Areas" around sensitive high-speed signals, so that vias and other traces are not accidentally placed incorrectly.

TCLK Design and Layout Considerations

One of the most commonly encountered problems in Gigabit Ethernet applications is underestimating the importance of TCLK jitter. The PLL based clock synthesizers, which are developed for driving high-speed microprocessor applications, are not generally desirable for high performance communication systems such as Gigabit Ethernet. Low jitter oscillators are recommended over PLL based synthesizers. The TCLK input provides the reference clock for the internal PLL, which is multiplied ten times to generate the baud rate clock. Therefore, it is very important that the TCLK be as jitter-free as possible in order to minimize the jitter introduced into PLL and its baud rate clock. The most difficult issue with regards to the TCLK is that the signal goes to multiple inputs when there are multiple SERDES devices (all require an extremely clean clock with fast edges and low jitter) present on a single board. The recommended scheme is to provide the clock from the low jitter 125MHz oscillator to a low skew clock buffer and then provide separate traces to each load from the low skew clock buffer. The power to the clock buffer should be isolated from the 3.3V plane with the use of a ferrite bead, and adequate decoupling should be provided for the buffer to filter the power supply noise. The clocks can be parallely terminated with AC termination to get the faster edges as the clock buffers are designed to drive 50ohm terminations. 22ohm series terminations can be used to minimize reflections and reduce EMI.

Frequency Stability of Crystal Oscillators

Frequency stability of crystal oscillators that provide fundamental circuit timing is very critical in Gigabit Ethernet technology. Several types of frequency stability are important:

- Long term frequency stability, which is determined by aging of the crystal and other circuit components.
- Medium term frequency stability, which is determined by environmental influences such as temperature, vibration and pressure.
- Short term stability, where the frequency fluctuates around its nominal value over a short period.

Most of the oscillator vendors specify the long-term stability but don't specify the short-term stability that is inter-related with the phase noise and jitter. A low phase clocking source can provide cost and accuracy benefits for an entire system.

Power Supply and Bypass Capacitors Layout Considerations

Good layout and bypass techniques to filter the power supply to IC have a significant impact upon signal quality. The power supply noise is of major concern as it will couple into the PLL circuits of transceiver, thereby increasing jitter generation in the transmitter and reducing jitter tolerance in the receiver. The board design must have a power plane for GND and VDD with at least 0.5 oz. Copper. 0.1uF and 0.001uF bypass

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capacitors should be used and placed as close as possible to the appropriate power supply pins of IDT77V7101 as shown in the Figure 6. IDT77V7101 doesn't have any analog VDD pins listed in the Data Sheet, so the power plane for this device should be isolated from the board's 3.3V plane with ferrite bead to filter out the noise and provide clean power to the chip. Ground plane must remain intact rather than attempting to steer current paths through cut planes. There is only one PLL loop filter capacitor of 0.001uF required between pins 16 and 17 of the device. Keeping the lines short will prevent the PLL loop filter capacitors from picking up noise from surrounding components. Vias used to connect the power planes to VDD and GND pins of the chips should be at least 25mils and the thickness of the trace connecting the capacitor and pin of the device should be equal to the width of the pin or at least 12mils.

The value of 115ohms is used for terminating the 100ohm differential transmission lines in the figures. The layout shown in Figure 7 is recommended for more noisy environments when there are several digital signals switching simultaneously. Pins 18 and 50 should be filtered with ferrite bead, and the rest of the chip should also be isolated with the help of a ferrite bead from the 3.3V power plane.

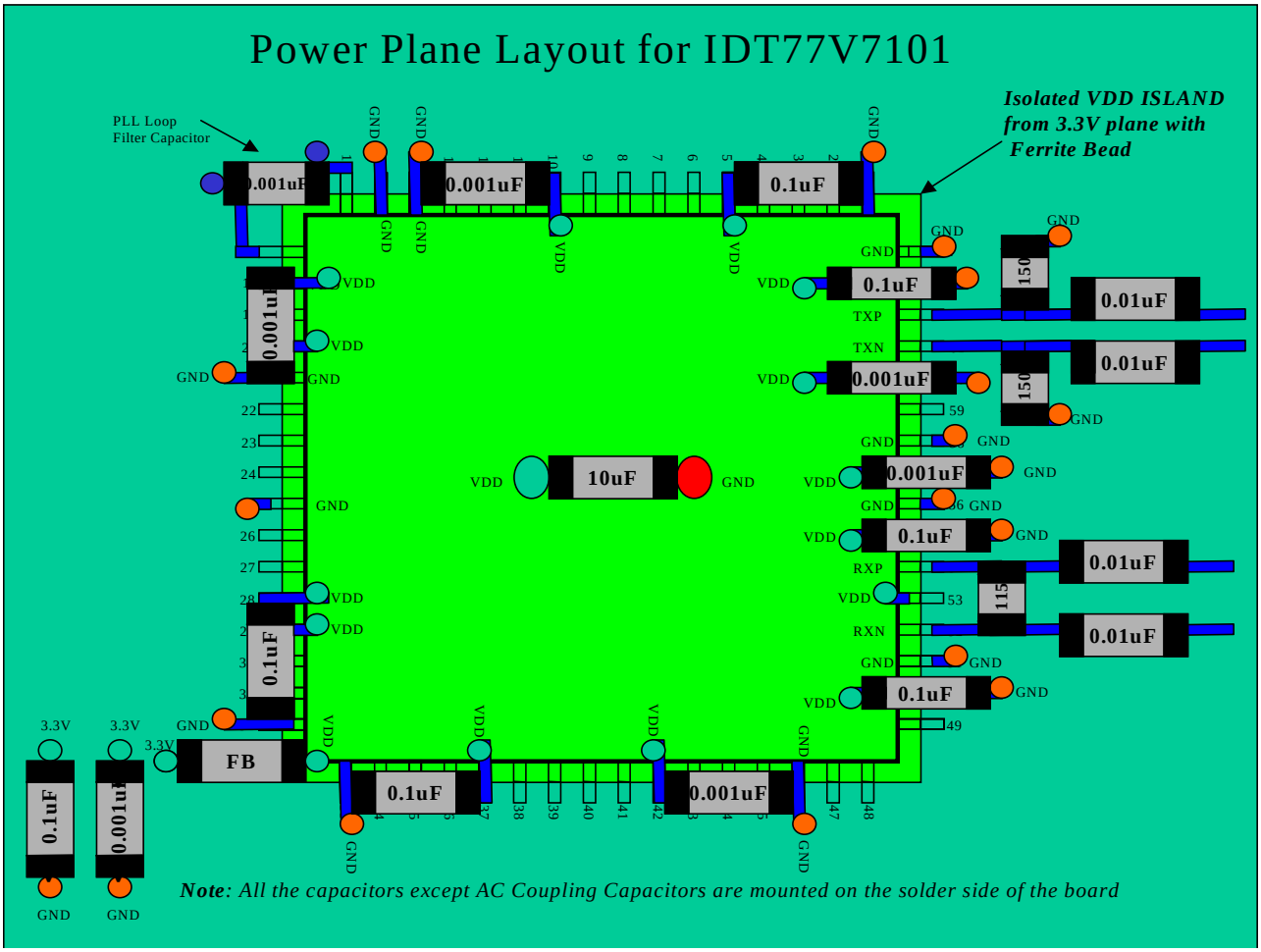
Power Plane Layout for IDT77V7101
PLL Loop Filter Capacitor
Isolated VDD ISLAND from 3.3V plane with Ferrite Bead
0.001uF
0.1uF
10uF
FB
150
115
0.01uF
TXP
TXN
RXP
RXN
3.3V
VDD
GND
Note: All the capacitors except AC Coupling Capacitors are mounted on the solder side of the board

Figure 6

Power Plane Layout for IDT77V7101

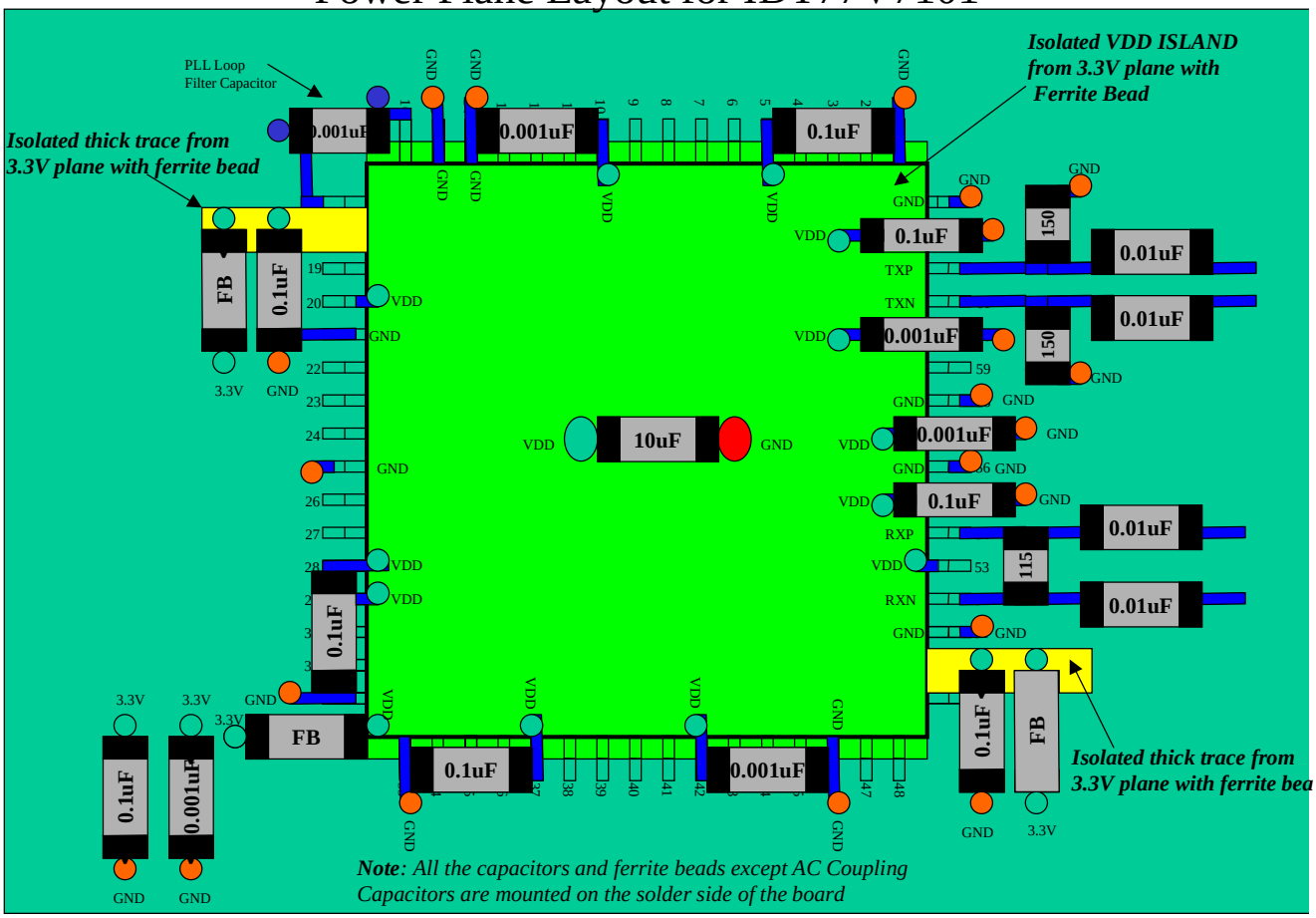

Figure 7

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Parallel Data Bus Design and Layout Considerations

The problem with data buses is that there is a lot of signals in a small area. The primary consideration here is to keep the traces roughly the same length, so that the trace length differences do not reduce the setup/hold times of the chips. The layout designer should be careful by closely grouping vias on these buses, as these groups of vias often create large holes in the ground plane. The recommended layout for placing the vias on the receive and transmit data buses is shown in Figure 8.

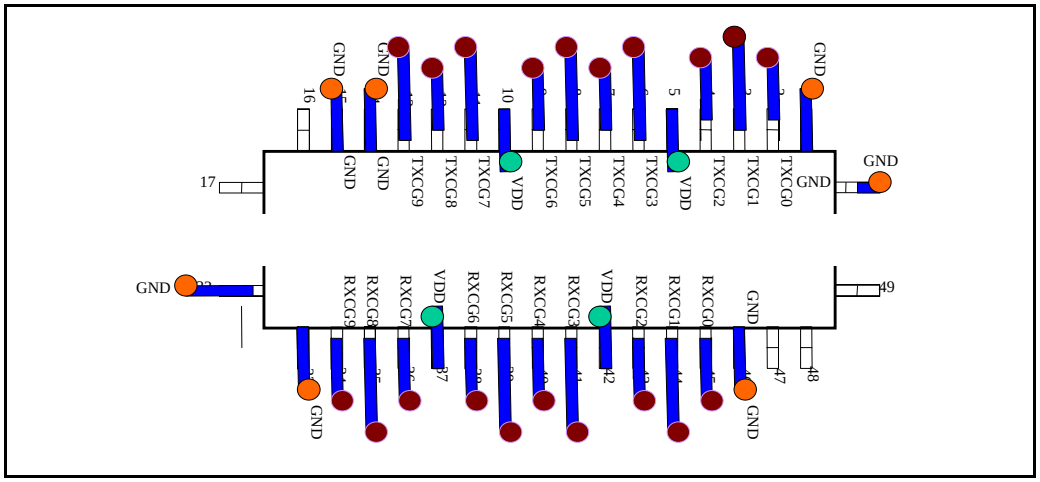

Figure 8

IDT77V7101 drivers on the receive parallel side do not drive 50ohm transmission lines. Therefore, designers should keep the receive parallel bus as short as possible, 1-2 inches, and the impedance of the traces should be around 70-75ohms, which can be achieved with thin traces. The parallel buses should also be designed for controlled impedance of 70 - 75 ohms, since it doesn't add any cost to the fabrication process because the fabrication house will charge the same amount of money for testing four traces as for a hundred traces for the controlled impedance boards. The design engineer should work very closely with the fabrication house to get the board material thickness, so that he can use these parameters to decide on the thickness and width of traces to get the desired impedance on the board.

In the event the chip doesn't give sufficient setup time margin for the MAC as well as any ASIC interface on the receive parallel interface, the recovered clocks should be delayed accordingly to meet the setup and hold times for the ASIC or MAC.

References

[1] IDT77V7101 Gigabit Ethernet Transceiver Chip Data Sheet

[2] Terminating Differential Signals on PCBs by Steve Kaufer and Kellee Crisafulli, Printed Circuit Design

[3] High-Speed Digital Design, A Handbook of Black Magic by Howard W. Johnson and Martin Graham
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