PROGRAMMING TURBOCLOCK™ QS5991, QS5992, QS5993, QS5V991, AND QS5V993

APPLICATION NOTE AN-226

INTRODUCTION

As new technology demands high-performance design, the distribution of high-speed clock has become a difficult task for the system designers. TurboClock™ provides the design engineers with the opportunities to overcome the many challenging issues of clock skew, and clock multiplication and division. The family offers 5V and 3.3V products in 32-pin PLCC and 28-pin QSOP packages:

- QS5991 (5V, TTL outputs in PLCC)
- QS5992 (5V, CMOS outputs in PLCC)
- QS5993 (5V, TTL outputs in QSOP)
- QS5V991 (3.3V, LVTTL outputs in PLCC)
- QS5V993 (3.3V, LVTTL outputs in QSOP)

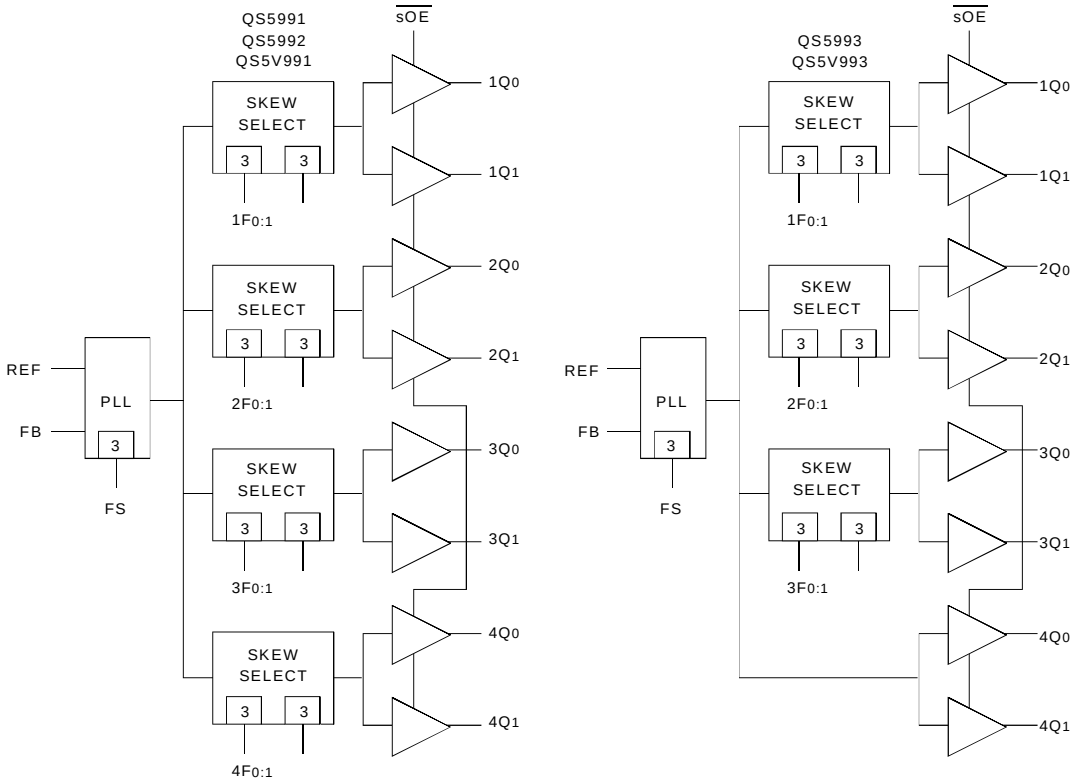
Both QS5991 and QS5992 are pin-compatible to Cypress CY7B991 and CY7B992, respectively. Figure 1 shows the TurboClock block diagrams for different product variants.

PROGRAMMING THE OUTPUT SKEW

The outputs of TurboClock™ are organized in four banks of 2 outputs each (nQ_1, nQ_0). Each output pair is programmed with the corresponding Function/Skew Select (nF_1, nF_0) inputs. The inputs can be tied High, Low, or left unconnected to Mid level (an internal resistor network will bias the signal level to 0.5V_{CC}). These 3-level inputs allow a total of nine different output selections. In the datasheet, the Skew Selection Table for Output Pairs (reproduced in the Control Summary Table) shows the list of outputs from each pair when any zero skew output is used as feedback. Note that output pair #1 and #2 share the same output characteristics, and skew adjustment for pair #4 is not available for QS5993 and QS5V993.

The first step in programming is to determine the VCO frequency (F_{NOM}) based on the REF input frequency, and the designed output frequencies. The output pair 1Q and 2Q will always be equal to VCO frequency. When an undivided output is used as feedback, the VCO operates at the same

FIGURE 1: TURBOCLOCK BLOCK DIAGRAMS



frequency as REF (or FB). If a divide-by-2 or divide-by-4 output is used as feedback, the VCO will operate at two or four times the REF frequency since the PLL will always try to align the frequency and phase of FB with REF. (When the divide-by-2 or divide-by-4 output is used as feedback, the FB is running at one-half or one-fourth the frequency of other outputs. Therefore, the other outputs are actually two or four times the REF frequency.)

The second step is to decide the setting for FS and $nF_{1:0}$ control inputs based on the VCO frequency and desired output skew. The desired output skew will be a multiple of the Time Unit (t_U) calculated from the PLL Programmable Skew Range and Resolution Table.

The flexibility of TurboClock is further enhanced by using a skewed output as feedback. For instance, if feedback is 3Q and $3F_{1:0}$ = ML (–2t_U), the 2Q output will have zero skew when $2F_{1:0}$ = LH (–2t_U) since the actual output skew at 2Q is calculated from the programmed 2Q output skew (–2t_U) minus the feedback skew (–2t_U). If $2F_{1:0}$ = LL, then the actual output skew at 2Q is –2t_U [–4t_U– (–2t_U)]. The Output Configuration tables show all the possible output configurations (skew adjustment, frequency multiplication/division) with different feedbacks. Tables 1 through 3 hold true for 1Q output configurations if FB is 2Q. The first column in the tables set the skew of the feedback. Each output pair has nine possible output combinations for a given FB(listed immediately on the right-hand side of the FB skew) by setting different levels to Function Select pairs ($nF_{1:0}$).

CONTROL SUMMARY TABLE FOR FEEDBACK SIGNALS

nF1:0	Skew (Pair #1, #2)	Skew (Pair #3)	Skew (Pair #4) (1)
LL	–4t_U	Divide by 2	Divide by 2
LM	–3t_U	–6t_U	–6t_U
LH	–2t_U	–4t_U	–4t_U
ML	–1t_U	–2t_U	–2t_U
MM	Zero Skew	Zero Skew	Zero Skew
MH	1t_U	2t_U	2t_U
HL	2t_U	4t_U	4t_U
HM	3t_U	6t_U	6t_U
HH	4t_U	Divide by 4	Inverted

NOTE:
1. Skew (pair #4) is not applicable for QS5993 and QS5V993.

PLL PROGRAMMABLE SKEW RANGE AND RESOLUTION TABLE

		FS = LOW	FS = MID	FS = HIGH
Time Unit (t_U)		1/(44 x F_{NOM})	1/(26 x F_{NOM})	1/(16 x F_{NOM})
VCO Frequency (F_{NOM})	QS5991, QS5992, and QS5993	25 to 35MHz	35 to 60MHz	60 to 100 MHz
	QS5V991 and QS5V993	25 to 35MHz	35 to 60MHz	60 to 85 MHz

OBTAINING MAXIMUM VCO FREQUENCY OPERATION FOR QS5991, QS5992, AND QS5993

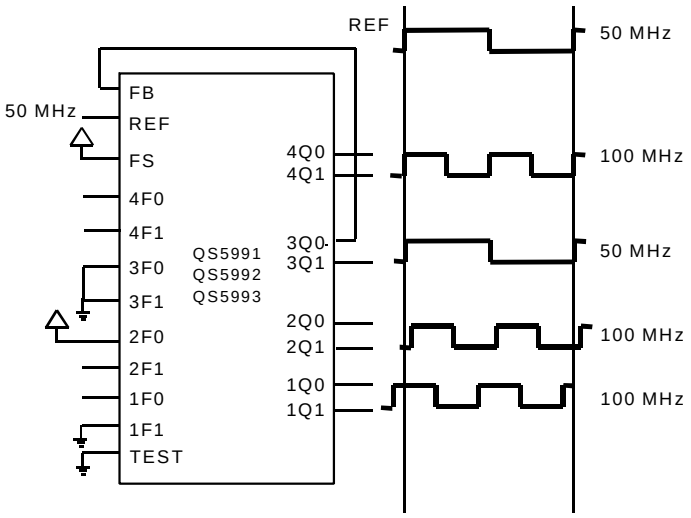


Figure 2. Wiring Diagram and Frequency Multiply by two with 3F[1:0] = LL.

Figure 2 demonstrates the QS5991,QS5992, and QS5993 configured for getting max output at 100 MHz. The 3Q0 output is programmed to divide by two and is fed back to FB. This causes the PLL to increase its frequency until 3Q0 and 3Q1 outputs are locked at 50 MHz while 1Qx, 2Qx and 3Qx outputs run at 100 MHz. The 1Qx, 2Qx and 4Qx outputs are skewed by programming their select inputs accordingly (Refer to Table 4 for more details.) Note that FS pin is connected to High for fastest frequency output range.

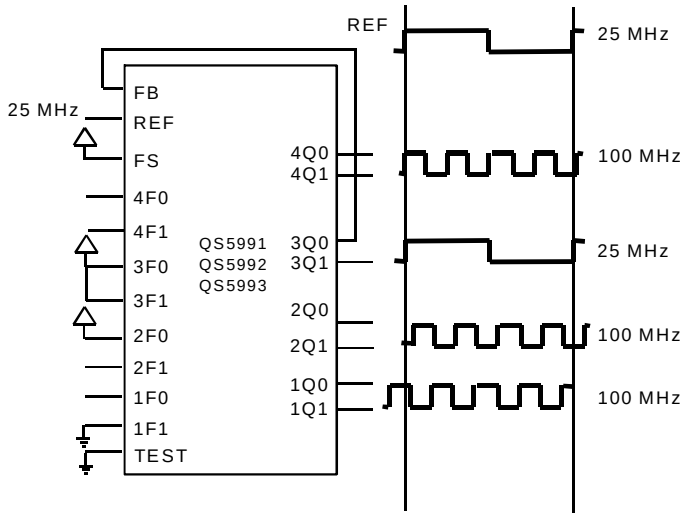


Figure 3. Wiring Diagram and Frequency Multiply by four with 3F[1:0] = HH.

Figure 3 shows the QS5991, QS5992 and QS5993 configured for getting max output at 100 MHz. The 3Q0 output is programmed to divide by four and is fed back to FB. This causes the PLL to increase its frequency until 3Q0 and 3Q1 outputs are locked at 25 MHz while 1Qx, 2Qx and 4Qx outputs run at 100 MHz. The 1Qx, 2Qx and 3Qx outputs are skewed by programming their select inputs accordingly (Refer to Table 5 for more details.) Note that FS pin is connected to High for fastest frequency output range.

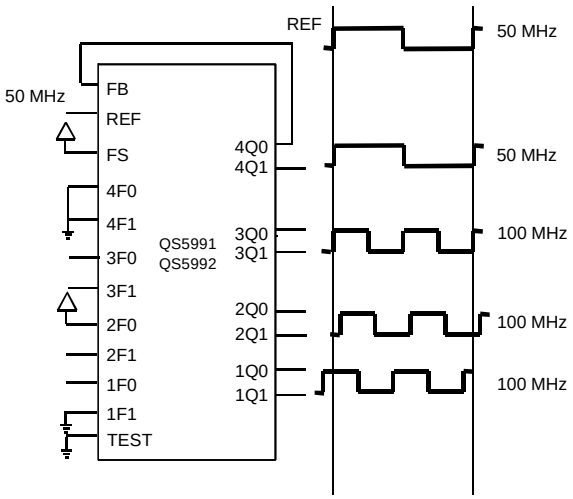


Figure 4. Wiring Diagram and Frequency Multiply by two with 4F[1:0] = LL.

Figure 4 illustrates the QS5991 and QS5992 configured for getting max output at 100 MHz. The 4Q0 output is programmed to divide by two and is fed back to FB. This causes the PLL to increase its frequency until 4Q0 and 4Q1 outputs are locked at 50 MHz while 1Qx, 2Qx and 3Qx outputs run at 100 MHz. The 1Qx, 2Qx and 3Qx outputs are skewed by programming their select inputs accordingly (Refer to Table 6 for more details.) Note that FS pin is connected to High for fastest frequency output range.

OBTAINING MAXIMUM VCO FREQUENCY OPERATION FOR QS5V991 AND QS5V993

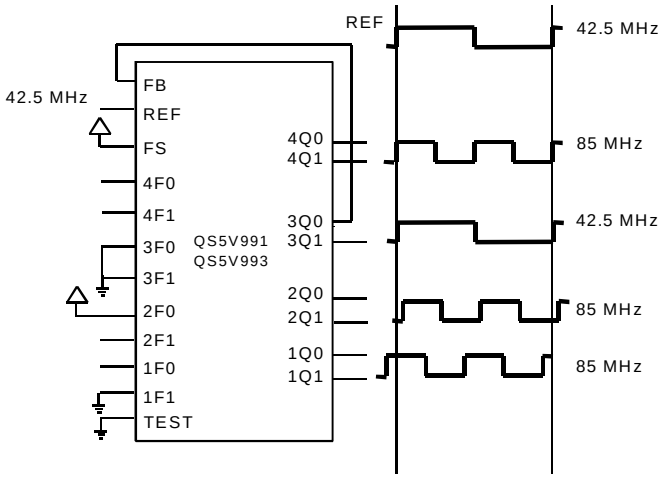


Figure 5. Wiring Diagram and Frequency Multiply by two with 3F[1:0] = LL.

Figure 5 demonstrates the QS5V991 and QS5V993 configured for getting max output at 85 MHz. The 3Q0 output is programmed to divide by two and is fed back to FB. This causes the PLL to increase its frequency until 3Q0 and 3Q1 outputs are locked at 42.5 MHz while 1Qx, 2Qx and 3Qx outputs run at 85MHz. The 1Qx, 2Qx and 4Qx outputs are skewed by programming their select inputs accordingly (Refer to Table 4 for more details.) Note that FS pin is connected to High for fastest frequency output range.

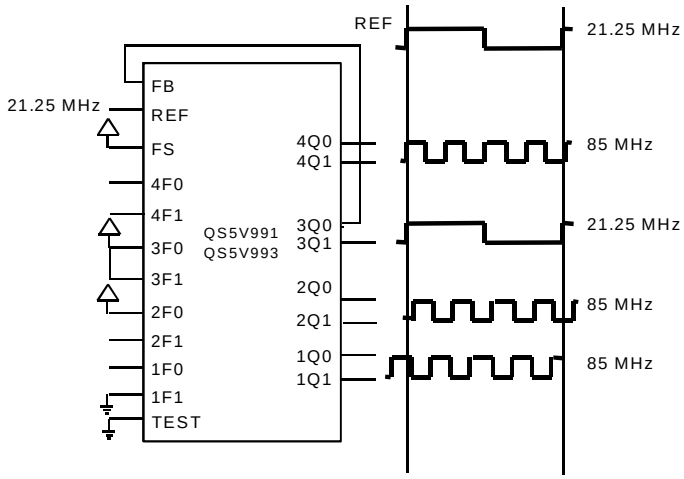


Figure 6. Wiring Diagram and Frequency Multiply by four with 3F[1:0] = HH.

Figure 6 shows the QS5V991 and QS5V993 configured for getting max output at 85 MHz. The 3Q0 output is programmed to divide by four and is fed back to FB. This causes the PLL to increase its frequency until 3Q0 and 3Q1 outputs are locked at 21.25 MHz while 1Qx, 2Qx and 4Qx outputs run at 85 MHz. The 1Qx, 2Qx and 3Qx outputs are skewed by programming their select inputs accordingly (Refer to Table 5 for more details.) Note that FS pin is connected to High for fastest frequency output range.

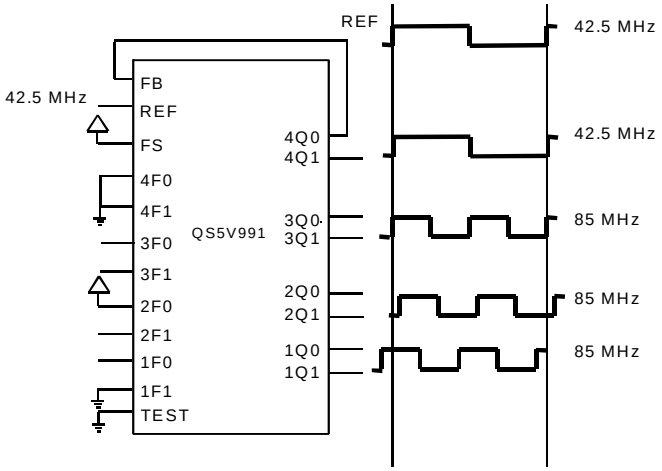


Figure 7. Wiring Diagram and Frequency Multiply by two with 4F[1:0] = LL.

Figure 7 illustrates the QS5V991 configured for getting max output at 85 MHz. The 4Q0 output is programmed to divide by two and is fed back to FB. This causes the PLL to increase its frequency until 4Q0 and 4Q1 outputs are locked at 42.5 MHz while 1Qx, 2Qx and 3Qx outputs run at 85 MHz. The 1Qx, 2Qx and 3Qx outputs are skewed by programming their select inputs accordingly (Refer to Table 8 for more details.) Note that FS pin is connected to High for fastest frequency output range.

OBTAINING MINIMUM VCO FREQUENCY OPERATION FOR QS5991, QS5992, QS5993, QS5V991, AND QS5V993

The VCO can operate at 25MHz minimum frequency with less than a 25MHz REF input with divided-by-two mode. If the divided-by-two is used as a feedback, the REF input can be as low as 12.5 MHZ and the VCO will operate at twice the REF frequency (25MHz). The VCO will operate at 25MHz with 25MHz REF input if there is no divider in the feedback loop. However, if the divided-by-four is used as a feedback, the input frequency is limited by the minimum REF input at 10MHz and the VCO will operate at four times the frequency (40MHz).

OUTPUT CONFIGURATION TABLES

TABLE 1. FB = 1Q. 2Q OUTPUT CONFIGURATIONS WITH DIFFERENT 2F(1:0)

FB	Output at 2F(1:0)								
1F(1:0)	LL	LM	LH	ML	MM	MH	HL	HM	HH
LL	0tU	1tU	2tU	3tU	4tU	5tU	6tU	7tU	8tU
LM	–1tU	0tU	1tU	2tU	3tU	4tU	5tU	6tU	7tU
LH	–2tU	–1tU	0tU	1tU	2tU	3tU	4tU	5tU	6tU
ML	–3tU	–2tU	–1tU	0tU	1tU	2tU	3tU	4tU	5tU
MM	–4tU	–3tU	–2tU	–1tU	0tU	1tU	2tU	3tU	4tU
MH	–5tU	–4tU	–3tU	–2tU	–1tU	0tU	1tU	2tU	3tU
HL	–6tU	–5tU	–4tU	–3tU	–2tU	–1tU	0tU	1tU	2tU
HM	–7tU	–6tU	–5tU	–4tU	–3tU	–2tU	–1tU	0tU	1tU
HH	–8tU	–7tU	–6tU	–5tU	–4tU	–3tU	–2tU	–1tU	0tU

TABLE 2. FB = 1Q. 3Q OUTPUT CONFIGURATIONS WITH DIFFERENT 3F(1:0)

FB	Output at 3F(1:0)								
1F(1:0)	LL	LM	LH	ML	MM	MH	HL	HM	HH
LL	f/2+4tU	–2tU	0tU	2tU	4tU	6tU	8tU	10tU	f/4+4tU
LM	f/2+3tU	–3tU	–1tU	1tU	3tU	5tU	7tU	9tU	f/4+3tU
LH	f/2+2tU	–4tU	–2tU	0tU	2tU	4tU	6tU	8tU	f/4+2tU
ML	f/2+1tU	–5tU	–3tU	–1tU	1tU	3tU	5tU	7tU	f/4+1tU
MM	f/2+0tU	–6tU	–4tU	–2tU	0tU	2tU	4tU	6tU	f/4+0tU
MH	f/2–1tU	–7tU	–5tU	–3tU	–1tU	1tU	3tU	5tU	f/4–1tU
HL	f/2–2tU	–8tU	–6tU	–4tU	–2tU	0tU	2tU	4tU	f/4–2tU
HM	f/2–3tU	–9tU	–7tU	–5tU	–3tU	–1tU	1tU	3tU	f/4–3tU
HH	f/2–4tU	–10tU	–8tU	–6tU	–4tU	–2tU	0tU	2tU	f/4–4tU

TABLE 3. FB = 1Q. 4Q OUTPUT CONFIGURATIONS WITH DIFFERENT 4F(1:0)

FB	Output at 4F(1:0)								
1F(1:0)	LL	LM	LH	ML	MM	MH	HL	HM	HH
LL	f/2+4tU	–2tU	0tU	2tU	4tU	6tU	8tU	10tU	–f+4tU
LM	f/2+3tU	–3tU	–1tU	1tU	3tU	5tU	7tU	9tU	–f+3tU
LH	f/2+2tU	–4tU	–2tU	0tU	2tU	4tU	6tU	8tU	–f+2tU
ML	f/2+1tU	–5tU	–3tU	–1tU	1tU	3tU	5tU	7tU	–f+1tU
MM	f/2+0tU	–6tU	–4tU	–2tU	0tU	2tU	4tU	6tU	–f+0tU
MH	f/2–1tU	–7tU	–5tU	–3tU	–1tU	1tU	3tU	5tU	–f–1tU
HL	f/2–2tU	–8tU	–6tU	–4tU	–2tU	0tU	2tU	4tU	–f–2tU
HM	f/2–3tU	–9tU	–7tU	–5tU	–3tU	–1tU	1tU	3tU	–f–3tU
HH	f/2–4tU	–10tU	–8tU	–6tU	–4tU	–2tU	0tU	2tU	–f–4tU

TABLE 4. FB = 3Q. 1Q/2Q OUTPUT CONFIGURATIONS WITH DIFFERENT 1F(1:0)/2F(1:0)

FB	Output at 1F(1:0)/2F(1:0)								
3F(1:0)	LL	LM	LH	ML	MM	MH	HL	HM	HH
LL	2*f–4tU	2*f–3tU	2*f–2tU	2*f–1tU	2*f+0tU	2*f+1tU	2*f+2tU	2*f+3tU	2*f+4tU
LM	2tU	3tU	4tU	5tU	6tU	7tU	8tU	9tU	10tU
LH	0tU	1tU	2tU	3tU	4tU	5tU	6tU	7tU	8tU
ML	–2tU	–1tU	0tU	1tU	2tU	3tU	4tU	5tU	6tU
MM	–4tU	–3tU	–2tU	–1tU	0tU	1tU	2tU	3tU	4tU
MH	–6tU	–5tU	–4tU	–3tU	–2tU	–1tU	0tU	1tU	2tU
HL	–8tU	–7tU	–6tU	–5tU	–4tU	–3tU	–2tU	–1tU	0tU
HM	–10tU	–9tU	–8tU	–7tU	–6tU	–5tU	–4tU	–3tU	–2tU
HH	4*f–4tU	4*f–3tU	4*f–2tU	4*f–1tU	4*f+0tU	4*f+1tU	4*f+2tU	4*f+3tU	4*f+4tU

TABLE 5. FB = 3Q. 4Q OUTPUT CONFIGURATIONS WITH DIFFERENT 4F(1:0)

FB	Output at 4F(1:0)								
3F(1:0)	LL	LM	LH	ML	MM	MH	HL	HM	HH
LL	0tU	2*f–6tU	2*f–4tU	2*f–2tU	2*f+0tU	2*f+2tU	2*f+4tU	2*f+6tU	–2*f
LM	f/2+6tU	0tU	2tU	4tU	6tU	8tU	10tU	12tU	–f+6tU
LH	f/2+4tU	–2tU	0tU	2tU	4tU	6tU	8tU	10tU	–f+4tU
ML	f/2+2tU	–4tU	–2tU	0tU	2tU	4tU	6tU	8tU	–f+2tU
MM	f/2+0tU	–6tU	–4tU	–2tU	0tU	2tU	4tU	6tU	–f+0tU
MH	f/2–2tU	–8tU	–6tU	–4tU	–2tU	0tU	2tU	4tU	–f–2tU
HL	f/2–4tU	–10tU	–8tU	–6tU	–4tU	–2tU	0tU	2tU	–f–4tU
HM	f/2–6tU	–12tU	–10tU	–8tU	–6tU	–4tU	–2tU	0tU	–f–6tU
HH	2*f	4*f–6tU	4*f–4tU	4*f–2tU	4*f+0tU	4*f+2tU	4*f+4tU	4*f+6tU	–4*f

TABLE 6. FB = 4Q. 1Q/2Q OUTPUT CONFIGURATIONS WITH DIFFERENT 1F(1:0)/2F(1:0)(1)

FB	Output at 1F(1:0)/2F(1:0)								
4F(1:0)	LL	LM	LH	ML	MM	MH	HL	HM	HH
LL	–2*f–4tU	2*f–3tU	2*f–2tU	2*f–1tU	2*f+0tU	2*f+1tU	2*f+2tU	2*f+3tU	2*f+4tU
LM	2tU	3tU	4tU	5tU	6tU	7tU	8tU	9tU	10tU
LH	0tU	1tU	2tU	3tU	4tU	5tU	6tU	7tU	8tU
ML	–2tU	–1tU	0tU	1tU	2tU	3tU	4tU	5tU	6tU
MM	–4tU	–3tU	–2tU	–1tU	0tU	1tU	2tU	3tU	4tU
MH	–6tU	–5tU	–4tU	–3tU	–2tU	–1tU	0tU	1tU	2tU
HL	–8tU	–7tU	–6tU	–5tU	–4tU	–3tU	–2tU	–1tU	0tU
HM	–10tU	–9tU	–8tU	–7tU	–6tU	–5tU	–4tU	–3tU	–2tU
HH	–f–4tU	–f–3tU	–f–2tU	–f–1tU	–f+0tU	–f+1tU	–f+2tU	–f+3tU	–f+4tU

NOTE:
1. Table 6 is not applicable for QS5993 and QS5V993.

TABLE 7. FB = 4Q. 3Q OUTPUT CONFIGURATIONS WITH DIFFERENT 3F(1:0) (1)

FB	Output at 3F(1:0)								
4F(1:0)	LL	LM	LH	ML	MM	MH	HL	HM	HH
LL	0tU	2*f–6tU	2*f–4tU	2*f–2tU	2*f+0tU	2*f+2tU	2*f+4tU	2*f+6tU	f/2+0tU
LM	f/2+6tU	0tU	2tU	4tU	6tU	8tU	10tU	12tU	f/4+6tU
LH	f/2+4tU	–2tU	0tU	2tU	4tU	6tU	8tU	10tU	f/4+4tU
ML	f/2+2tU	–4tU	–2tU	0tU	2tU	4tU	6tU	8tU	f/4+2tU
MM	f/2+0tU	–6tU	–4tU	–2tU	0tU	2tU	4tU	6tU	f/4+0tU
MH	f/2–2tU	–8tU	–6tU	–4tU	–2tU	0tU	2tU	4tU	f/4–2tU
HL	f/2–4tU	–10tU	–8tU	–6tU	–4tU	–2tU	0tU	2tU	f/4–4tU
HM	f/2–6tU	–12tU	–10tU	–8tU	–6tU	–4tU	–2tU	0tU	f/4–6tU
HH	–f/2	–f–6tU	–f–4tU	–f–2tU	–f+0tU	–f+2tU	–f+4tU	–f+6tU	–f/4

NOTE:
1. Table 7 is not applicable for QS5993 and QS5V993.

CONCLUSION

With its flexible, programmable skew capability, TurboClock is ideally suited for a variety of applications. IDT offers several tools to assist the designers with designs incorporating TurboClock. One of these tools is TurboKit, a powerful software tool that provides the designers with all possible solutions for a given set of inputs at the press of a key. The designers can then select the solution that best meets their requirements. In addition, IBIS models are available at no cost for system simulation purposes.

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