AP-625

APPLICATION NOTE

28F008S5/S3 Compatibility with 28F008SA/SA-L

December 1998

Order Number: 292180-004

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 CG-041493

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REVISION HISTORY

Number	Description
-001	Original Version
-002	Minor changes throughout document Revised 28F008SA-L device ID from A1 to A2 Removed 28F008SC-L reference Changed byte write reference to program
-003	Change 28F008SC reference to 28F008S5/S3
-004	Removed references to “Byte-Wide FlashFile™ memory and 28F008SC

1.0 INTRODUCTION

The 28F008S5/S3 are the first SmartVoltage technology devices to be added to Intel® x8 FlashFile™ memory family. Since its architecture evolved from the 28F008SA/SA-L, it maintains compatibility, enabling a smooth migration from the 28F008SA/SA-L to 28F008S5/S3.

The 28F008S5/S3 FlashFile memories provide new enhancements that help reduce system cost and improve system code/data security and performance, such as:

- Enhanced Suspend Operations
- Flexible Block Locking Scheme
- SmartVoltage Technology

This application note is divided into three major sections: software compatibility, hardware compatibility and specification differences. These sections will highlight enhancements and differences between the 28F008S5/S3 and 28F008SA/SA-L.

2.0 SOFTWARE COMPATIBILITY

The 28F008S5/S3 are software-compatible with the 28F008SA/SA-L. Just as the Pentium® processor can execute software developed specifically for the Intel486™ microprocessor, software written for the 28F008SA/SA-L will work with the 28F008S5/S3, assuming it supports the 28F008S5/S3 device ID. In addition, the 28F008S5/S3 enhances the 28F008SA/SA-L command set, by supplying a superset of software commands. These new and enhanced commands enable a superior level of system data security, flexibility and performance.

2.1 Command Superset

The superset of commands provides both enhancements and new feature support to the 28F008SA/SA-L command set architecture. The enhancements expand upon the suspend capability and improve suspend latency delays. New additions enable a flexible block locking scheme.

Use of these commands listed in Table 1 is optional. Depending upon application requirements, the 28F008SA/SA-L command set may provide sufficient flexibility and support.

Table 1. Enhanced and New Commands Added to the 28F008S5/S3 Command-Set Architecture

Command	Enhanced	New
Intelligent Identifier	✔	
Block Erase Suspend	✔	
Program Suspend		✔
Set Block Lock-Bit		✔
Set Master Lock-Bit		✔
Clear Block Lock-Bits		✔

2.1.1 ENHANCED INTELLIGENT IDENTIFIER OPERATION

The 28F008S5/S3 extend the capability of the Intelligent Identifier command (90H) by providing access to more internal device information. Therefore, the command is renamed Read Identifier Codes command (90H). It provides access to the manufacture and device codes like the 28F008SA/SA-L. The command also enables access to individual block lock configuration codes for each block and master lock configuration code information as shown in Figure 1. The lock configuration information is pertinent to applications that choose to implement the 28F008S5/S3 block locking feature.

Because of the enhanced and new commands, the 28F008S5/S3 and 28F008SA/SA-L do not share the same device ID. This difference allows for software component identification. System software can read the device ID and select the appropriate algorithms for the given component.

Table 2. Device IDs for the 8-Mbit FlashFile™ Memory Family

Device	Device Code (Hex)
28F008SA & 28F008SA-L	A2
28F008S5 & 28F008S3	A6

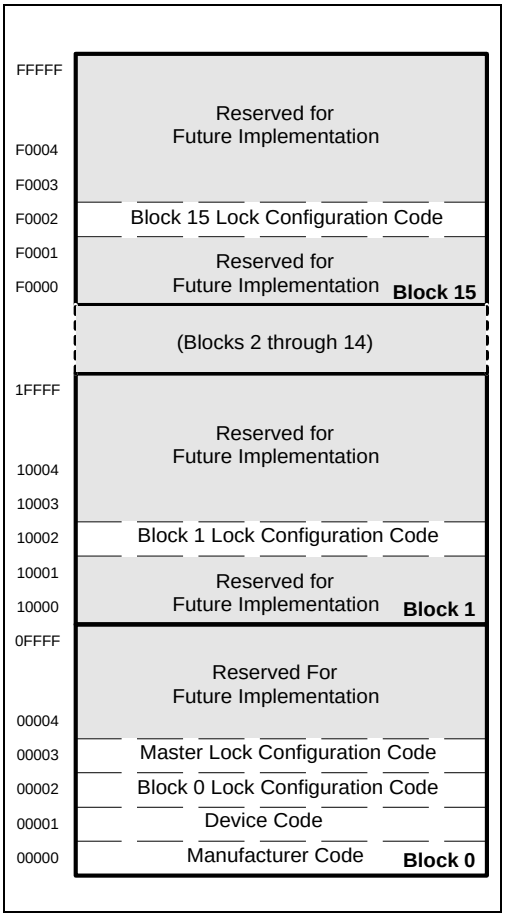

Figure 1. 28F008S5/S3 Device Identifier Code Memory Map

2.1.2 ENHANCED SUSPEND OPERATIONS

The 28F008SA/SA-L support erase suspend to read. The 28F008S5/S3 embellish the suspend capability by supporting a variety of options and improving the suspend latency delay. The 28F008S5/S3 support these suspend operations:

- Program Suspend to Read
- Erase Suspend to Read and Program

The Program Suspend command allows program interruption to read data in other bytes of memory. Status register bit SR.2 informs the system of the program suspend status.

The Erase Suspend command allows block erase interruption to read or program data in another block of memory. The program operation can be suspended using the Program Suspend command during an erase suspend state, as well.

2.1.3 NEW BLOCK LOCKING CAPABILITY

Enhancing the 28F008SA/SA-L code/data protection mechanisms, the 28F008S5/S3 incorporate an additional security feature: individual block locking. Its usage is optional and versatile, enabling many different levels of protection.

Individual block locking uses a combination of bits to lock and unlock blocks:

- Sixteen block lock-bits that gate block erase and program operations.
- A master lock-bit that gates modification of block lock-bits.

A block lock-bit is assigned to each of the sixteen 64-Kbyte blocks. These bits are configured by using the Set and Clear Block Lock-Bit commands. The Clear Block Lock-Bits command unlocks all sixteen blocks by simultaneously clearing all the block lock-bits. When a block lock-bit is set, it disables all block erase and program operations to that block. However, high voltage (V_{HH}) on RP# overrides the block lock-bits, permitting erase and program operations.

The master lock-bit is set using a combination of software and hardware. Using the Set Master Lock-Bit command sequence in conjunction with RP# = V_{HH} sets the master lock-bit. Once set, the master lock-bit cannot be cleared (only temporarily overridden when RP# = V_{HH}). If the Set Master Lock-Bit command sequence is attempted with RP# = V_{IH}, the operation fails.

When the master lock-bit is not set, individual block lock-bits can be set and cleared using the Set and Clear Block Lock-Bit command sequences. After the master lock-bit is set, subsequent setting and clearing of block lock-bits require both a software command sequence and V_{HH} on the RP# pin as shown in Table 3. If a Set or Clear Block Lock-Bit command is attempted with the master lock-bit set and RP# = V_{IH}, the operation will fail.

With a good understanding of the 28F008S5/S3 block locking scheme, the proper implementation can be selected for your design. In many cases, the block locking option may not be required. The 28F008SA/SA-L protection mechanisms, dedicated V_{PP}, V_{LKO}, and two command sequence, provide sufficient protection. On the other hand, applications that value this new feature may elect to lock individual blocks in a programmer or in-system. Using a PROM programmer, critical system boot code that will not require modification can be permanently locked. This assumes that the system can't apply V_{HH} to RP# to unlock blocks. If in-system block locking and unlocking is required, the system must control high voltage on the RP# pin—only when the master lock-bit is locked.

Table 3. 28F008S5/S3 Optional Block Locking Protection Combinations

Operation	Master Lock-Bit	Block Lock-Bit	RP#	Effect
Block Erase or Program	X	0	V_{IH} or V_{HH}	Block is Unlocked. Block Erase and Program Enabled
		1	V_{IH}	Block is Locked. Program and Erase Disabled
			V_{HH}	Block Lock-Bit Override. Block Erase and Program Enabled
Set Block Lock-Bit	0	X	V_{IH} or V_{HH}	Set Block Lock-Bit Enabled
	1	X	V_{IH}	Master Lock-Bit is Set, Set Block Lock-Bit Disabled
			V_{HH}	Master Lock-Bit Override, Set Block Lock-Bit Enabled
Set Master Lock-Bit	X	X	V_{IH}	Set Master Lock-Bit Disabled
			V_{HH}	Set Master Lock-Bit Enabled
Clear Block Lock-Bits	0	X	V_{IH} or V_{HH}	Clear Block Lock-Bit Enabled
	1	X	V_{IH}	Master Lock-Bit is Set, Clear Block Lock-Bits Disabled
			V_{HH}	Master Lock-Bit Override, Clear Block Lock-Bit Enabled

Table 4. 28F008S5/S3 Status Register Definition, Highlighting New Additions: SR.2 and SR.1

WSMS	ESS	ECLBS	PSLBS	VPPS	**PSS**	**DPS**	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

SR.6 = ERASE SUSPEND STATUS
1 = Block Erase Suspended
0 = Block Erase in Progress/Completed

SR.5 = ERASE AND CLEAR LOCK-BITS STATUS
1 = Error in Block Erasure or Clear Lock-Bits
0 = Successful Block Erase or Clear Lock-Bits

SR.4 = PROGRAM AND SET LOCK-BIT STATUS
1 = Error in Program or Set Block/Master Lock-Bit
0 = Successful Program or Set Block/Master Lock-Bit

SR.3 = V_{PP} STATUS
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

SR.2 = PROGRAM SUSPEND STATUS
1 = Program Suspended
0 = Program in Progress/Completed

SR.1 = DEVICE PROTECT STATUS
1 = Block Lock-Bit, Master Lock-Bit and/or RP# Lock Detected, Operation Abort
0 = Unlock

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS

NOTES:

Check RY/BY# or SR.7 to determine block erase, program, or lock-bit configuration completion. SR.6-0 are invalid while SR.7 = "0."

If both SR.5 and SR.4 are "1"s after a block erase or lock-bit configuration attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase, Program, Set Block/Master Lock-Bit, or Clear Block Lock-Bits command sequences. SR.3 is not guaranteed to reports accurate feedback only when $V_{PP} = V_{PPH1/2/3}$.

SR.1 does not provide a continuous indication of master and block lock-bit values. The WSM interrogates the master lock-bit, block lock-bit, and RP# only after Block Erase, Program, or Lock-Bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, master lock-bit is set, and/or RP# is not V_{HH}. Reading the block lock and master lock configuration codes after writing the Read Identifier Codes command indicates master and block lock-bit status.

SR.2 and SR.1 are RESERVED bits on the 28F008SA

2.2 Status Register

The 28F008S5/S3 and 28F008SA/SA-L share a compatible status register definition. The 28F008S5/S3, however, expand the status register definition to enable support for its new features. It furnishes additional system feedback by introducing two new status register bits for program suspend and device data protection notification. These bits, SR.2 and SR.1, were previously reserved for future use in the 28F008SA/SA-L status register definition. Code written for the 28F008SA/SA-L should mask these two bits when polling the status register.

3.0 HARDWARE COMPATIBILITY

Like the 28F008SA/SA-L, the 28F008S5/S3 are available in 40-lead standard TSOP and 44-lead PSOP packages and is pinout-compatible, which paves the way for a smooth migration to the 28F008S5/S3. The following three sections address hardware upgrade concerns.

- Package Offerings
- SmartVoltage Technology
- RP# Control

3.1 Package Offerings

The 28F008S5/S3 does not implement the reverse-pinout 40-lead TSOP configuration. It will be available in the standard 40-TSOP and 44-lead PSOP packages. The small form factor of the standard TSOP package coupled with advance PCB layout tools enable very compact layouts. Using standard packages, a high-density flash array as compact as the compact layout is achievable.

3.2 Taking Advantage of SmartVoltage Technology

The 28F008S5/S3 provide system designers with several V_{CC} and V_{PP} options to meet various system performance and power expectations.

Table 5. V_{CC} and V_{PP} Operational Combinations Offered by SmartVoltage Technology

Product	V_{CC} Voltage	V_{PP} Voltage
28F008S3	2.7 V	—
	3.3 V	3.3 V and 12 V(1)
28F008S5	5.0 V	5.0 V and 12 V

NOTE:

1. 12 V (11.4 V-12.6 V) can only be applied to V_{PP} for a maximum of 80 hours over the lifetime of the device. Therefore, V_{PP} should not be permanently tied to 12 V.

As the V_{PP} voltage decreases, flash memory's block erase and program performance decreases. The 28F008S5/S3 therefore, retain the 12 V V_{PP} option for applications that require high block erase and program performance. For the 28F008S3, 12 V can only be applied to V_{PP} for a maximum of 80 hours. Therefore, V_{PP} should not be permanently tied to 12 V. The 12 V V_{PP} option provides fast program and erase performance to maximize factory throughput. Automatic-Test-Equipment (ATE) and PROM programmers can take advantage of the 12 V V_{PP} capability to reduce flash memory programming time which will lower manufacturing costs.

New designs may elect to utilize a V_{PP} voltage equivalent to V_{CC}. Designs that plan to use the 28F008S5/S3 in the future can implement a flexible V_{PP} option, as shown in Figure 2. This implementation provides connection to 12 V V_{PP} for the 28F008SA/SA-L today and lower voltages for the 28F008S5/S3 in the future. The low voltage V_{PP} connection is a requirement for the 28F008S3. A lower V_{PP} voltage allows the 12 V converter and associated circuitry that is sometimes needed to generate a high programming voltage to be eliminated to lower system cost and component count.

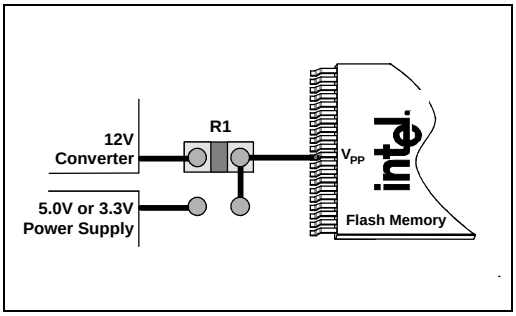

Figure 2. Flexible V_{PP} Voltage Design

3.3 Optional High Voltage Control on RP#

If high voltage control is necessary to permit in-system block locking and unlocking, the system must have a way to elevate the RP# voltage to V_{HH}. High voltage on RP# allows block locking and unlocking when the master lock-bit is unlocked. Figure 3 shows a two MOSFET configuration that switches voltage between 0 V, +5 V, and +12 V when inputs Reset# and Unlock# are driven to CMOS levels.

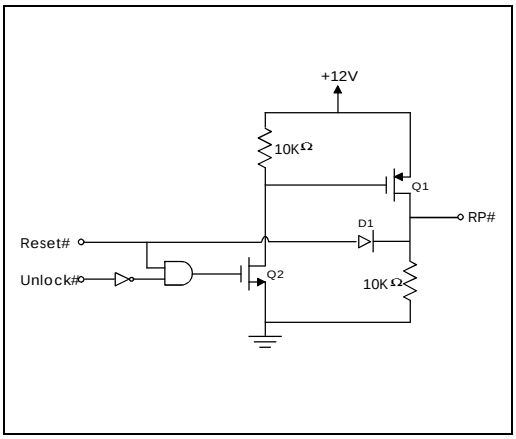

Figure 3. Optional High Voltage Control on RP#

4.0 SPECIFICATION DIFFERENCES

The 28F008S5/S3 are compatible with the 28F008SA/SA-L. Some specification differences exist between the two products due to different circuit designs and process technology.

Address Transition Detection (ATD)

New circuitry called Address Transition Detection (ATD) is built into the 28F008S5/S3. This circuitry enables an Automatic Power Saving (APS) feature and improves access time. APS substantially reduces the active current when the device is in a static mode of operation (addresses not switching).

ATD circuitry detects address transitions on the device's inputs and automatically generates an internal signal that starts a read access. ATD has been integrated into many flash memory components but is new to the 8-Mbit FlashFile memories. Key items to verify in your system design include:

- Glitches on CE# & Address Lines
- Input Signal Rise/Fall Time
- Floating Address Lines

When the device is selected (CE# = "0"), all addresses should be driven to a valid state. Also, it is imperative that all input signal transition times be <10 ns to prevent higher power consumption or inconsistent device operation. This specification is similar to that stated in all other flash memory datasheet test configuration conditions.

4.1 DC Characteristics

Tables 6 and 7 compare the 28F008S5/S3 DC specifications to the 28F008SA/SA-L. Notice that V_{PPLK} is lower. Designs that switch V_{PP} off during normal operations to prevent unwanted data alteration should make sure that the V_{PP} voltage transitions to GND.

SmartVoltage technology provides the 28F008S5/S3 with additional V_{CC} and V_{PP} options that the 28F008SA does not offer. Refer to the 28F008S5/S3 datasheets for further information about valid voltages.

Table 6. DC Specification Differences between the 28F008SA and 28F008S5 at 5 V V_{CC}

Sym	Parameter	28F008SA		28F008S5		Unit	Test Condition
		Typ	Max	Typ	Max		
I_{CCD}	V_{CC} Deep Power-Down Current		1.2		10	µA	RP# = GND ± 0.2 V I_{OUT} (RY/BY#) = 0 mA
V_{PPLK}	V_{PP} during Normal Operations	0	6.5	0	1.5	V	

Table 7. DC Specification Differences between the 28F008SA-L and 28F008S3 at 3.3 V V_{CC}

Sym	Parameter	28F008SA-L		28F008S3		Unit	Test Condition
		Typ	Max	Typ	Max		
I_{CCD}	V_{CC} Deep Power-Down Current		1.2		10	µA	RP# = GND ± 0.2 V I_{OUT} (RY/BY#) = 0 mA
V_{PPLK}	V_{PP} during Normal Operations	0	6.5	0	1.5	V	

4.2 AC Characteristics

The 28F008S5/S3 significantly improve t_{GHQZ} at 3.3 V and 5 V V_{CC}. This improvement eases high-speed designs and improves processor compatibility. In addition, 3.3 V V_{CC} read performance over the 28F008SA-L is significantly improved. Table 8 compares the read performance between the 28F008S5 and 28F008SA. Tables 9 and 10 compare the 28F008S3's read and write performance to the 28F008SA-L.

The 28F008S5/S3 optional block locking capability may require high voltage control of RP# to lock and unlock blocks. If so, the applied V_{HH} voltage must be present t_{PHHWH} before initiating a set or clear lock-bit command and held valid throughout the operation.

Table 8. AC Read Specification Differences between the 28F008SA and 28F008S5 at 5 V V_{CC}

Versions		28F008SA-85/90		28F008S5-85/90		28F008S5-120		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{GHQZ}	OE# High to Output in High Z		30		10		15	ns

Table 9. AC Read Specification Differences between the 28F008SA-L and 28F008S3 at 3.3 V V_{CC}

Versions		28F008SA-L200		28F008S3-120		28F008S3-150		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{AVAV}	Read Cycle Time	200		120		150		ns
t_{AVQV}	Address to Output Delay		200		120		150	ns
t_{ELQV}	CE# to Output Delay		200		120		150	ns
t_{PHQV}	RP# High to Output Delay		500		600		600	ns
t_{GLQV}	OE# to Output Delay		85		50		55	ns
t_{GHQZ}	OE# High to Output in High Z		30		20		25	ns

Table 10. AC Write Specification Differences between the 28F008SA-L and 28F008S3 at 3.3 V V_{CC}

Versions		28F008SA-L200		28F008S3-120		28F008S3-150		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{AVAV}	Write Cycle Time	200		120		150		ns
t_{ELWL}	CE# Setup to WE# Going Low	20		10		10		ns
t_{WLWH}	WE# Pulse Width	60		50		50		ns
t_{AVWH}	Address Setup to WE#/CE# Going High	60		50		50		ns
t_{DVWH}	Data Setup to WE#/CE# Going High	60		50		50		ns

5.0 CONCLUSION

This application note outlined differences and design issues to consider when upgrading from the 28F008SA/SA-L to 28F008S5/S3. Consult reference documentation for a more complete understanding of compatibility and device capabilities. Please contact your local Intel or distribution sales office for more information on Intel® flash memory products.

APPENDIX A
ADDITIONAL INFORMATION(1,2)

Order Number	Document/Tool
290597	*5 Volt FlashFile™ Memory; 28F004S5, 28F008S5, 28F016S5* datasheet
290598	*3 Volt FlashFile™ Memory; 28F004S3, 28F008S3, 28F016S3* datasheet
290429	*5 Volt FlashFile™ Memory; 28F008SA* datasheet
Note 3	*AP-359 28F008SA Hardware Interfacing*
Note 3	*28F008SA-L* datasheet
Note 3	*AP-364 28F008SA Automation and Algorithms*
Contact Intel/Distribution Sales Office	TimingDesigner* Files
Contact Intel/Distribution Sales Office	Schematic Symbols
Contact Intel/Distribution Sales Office	Functional Models
Contact Intel/Distribution Sales Office	iBIS Models

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. These documents can be located at the Intel World Wide Web support site, http://www.intel.com/support/flash/memory