FAST CMOS OCTAL TRANSPARENT LATCH

IDT54/74FCT2373T/AT/CT

FEATURES:

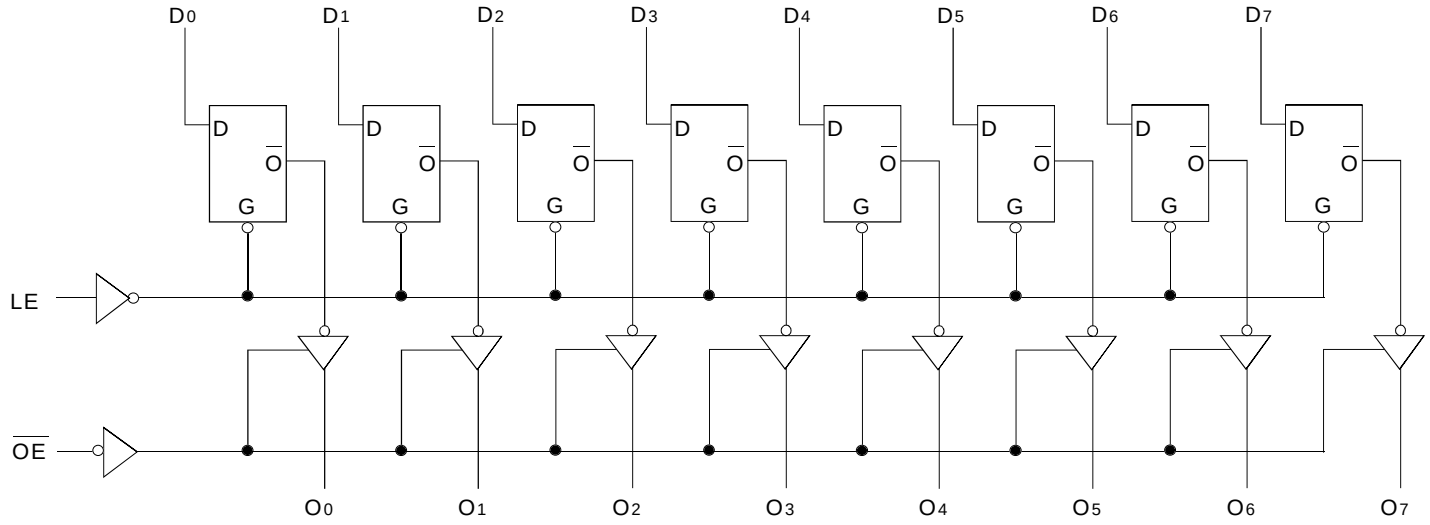
- Low input and output leakage ≤1µA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- Meets or exceeds JEDEC standard 18 specifications
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Std., A and C speed grades
- Resistor output (-15mA I_{OH}, 12mA I_{OL} Ind.)
  (-12mA I_{OH}, 12mA I_{OL} Mil.)
- Reduced system switching noise
- Available in the following packages:
  - Industrial: SOIC, QSOP, TSSOP
  - Military: CERDIP, LCC, CERPACK

DESCRIPTION:

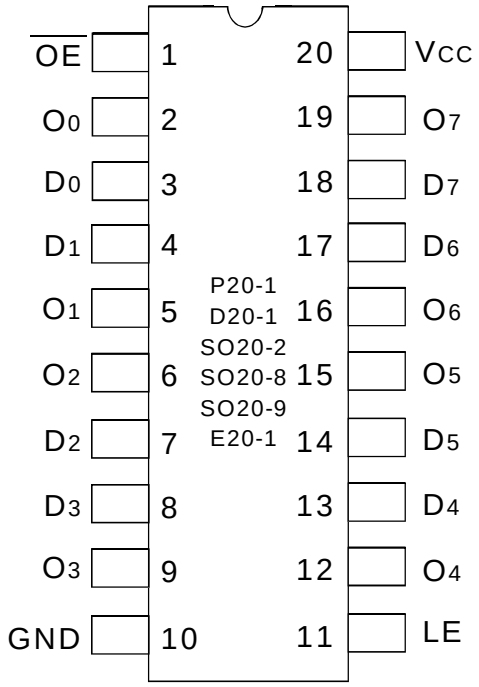
The FCT2373T is an octal transparent latch built using an advanced dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is high. When LE is low, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is low. When $\overline{OE}$ is high, the bus output is in the high-impedance state.

The FCT2373T has balanced drive outputs with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. The FCT2373T parts are plug-in replacements for FCT373T parts.

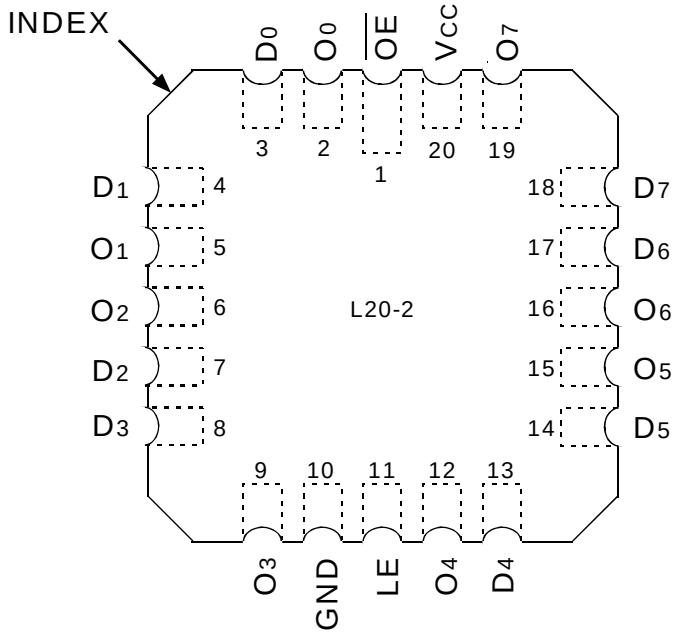
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP/ SOIC/ QSOP/ TSSOP/ CERPACK
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
D_N	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
O_N	3-State Outputs

FUNCTION TABLE (1)

Inputs			Outputs
D_N	LE	$\overline{OE}$	O_N
L	H	L	L
H	H	L	H
X	X	H	Z

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]		V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State output pins) [4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	µA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Input LOW Current	V_{CC} = 0V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V [3]		16	48		µA
I_{ODH}	Input HIGH Current	V_{CC} = 0V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V [3]		–16	–48		µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL I_{OH} = –15mA IND	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA	—	0.3	0.5	V

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for thie parameter is ±5µA at T_A = -55°C.
5. This parameter is guaraneteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	2.2	mA
		50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	V_{IN} = 3.4 V_{IN} = GND	—	0.9	3.2	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND		1.2	3.4[5]	
		50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	V_{IN} = 3.4 V_{IN} = GND	—	3.2	11.4[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - INDUSTRIAL (1)

Symbol	Parameter	Condition(1)	FCT2373T		FCT2373AT		FCT2373CT		Unit
			Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pF R_L = 500Ω	1.5	8	1.5	5.2	1.5	4.2	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_N		2	13	2	8.5	2	5.5	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12	1.5	6.5	1.5	5.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.5	1.5	5.5	1.5	5	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to LE		2	—	2	—	2	—	ns
t_H	Hold Time HIGH or LOW, D_N to LE		1.5	—	1.5	—	1.5	—	ns
t_W	LE Pulse Width HIGH(3)		6	—	5	—	5	—	ns

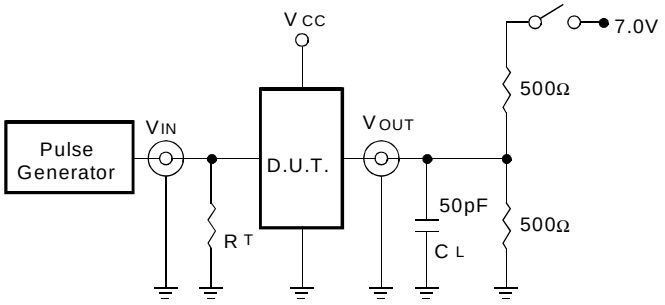
SWITCHING CHARACTERISTICS OVER OPERATING RANGE - MILITARY (1)

Symbol	Parameter	Condition(1)	FCT2373T		FCT2373AT		FCT2373CT		Unit
			Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pF R_L = 500Ω	1.5	8.5	1.5	5.6	1.5	5.1	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_N		2	15	2	9.8	2	8	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	13.5	1.5	7.5	1.5	6.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	10	1.5	6.5	1.5	5.9	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to LE		2	—	2	—	2	—	ns
t_H	Hold Time HIGH or LOW, D_N to LE		1.5	—	1.5	—	1.5	—	ns
t_W	LE Pulse Width HIGH(3)		6	—	6	—	6	—	ns

NOTES:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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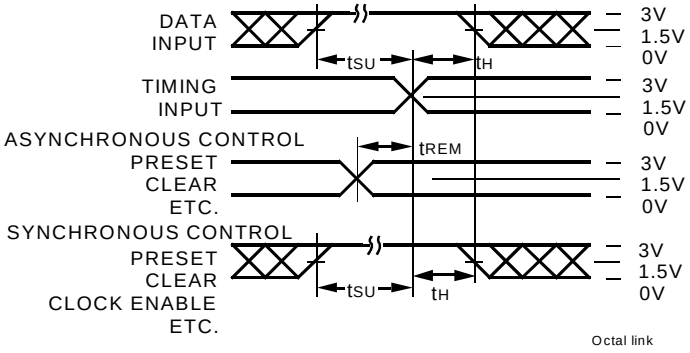
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD, AND RELEASE TIMES



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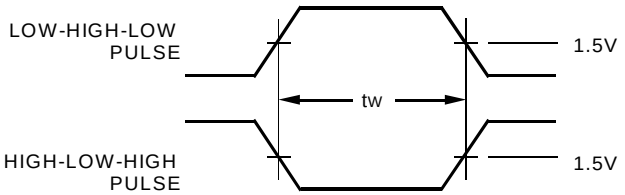
PULSE WIDTH



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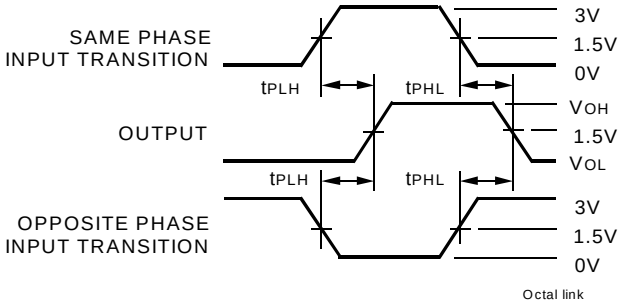
PROPAGATION DELAY



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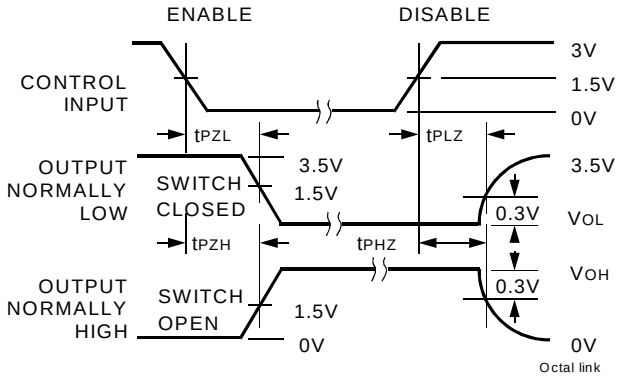
ENABLE AND DISABLE TIMES



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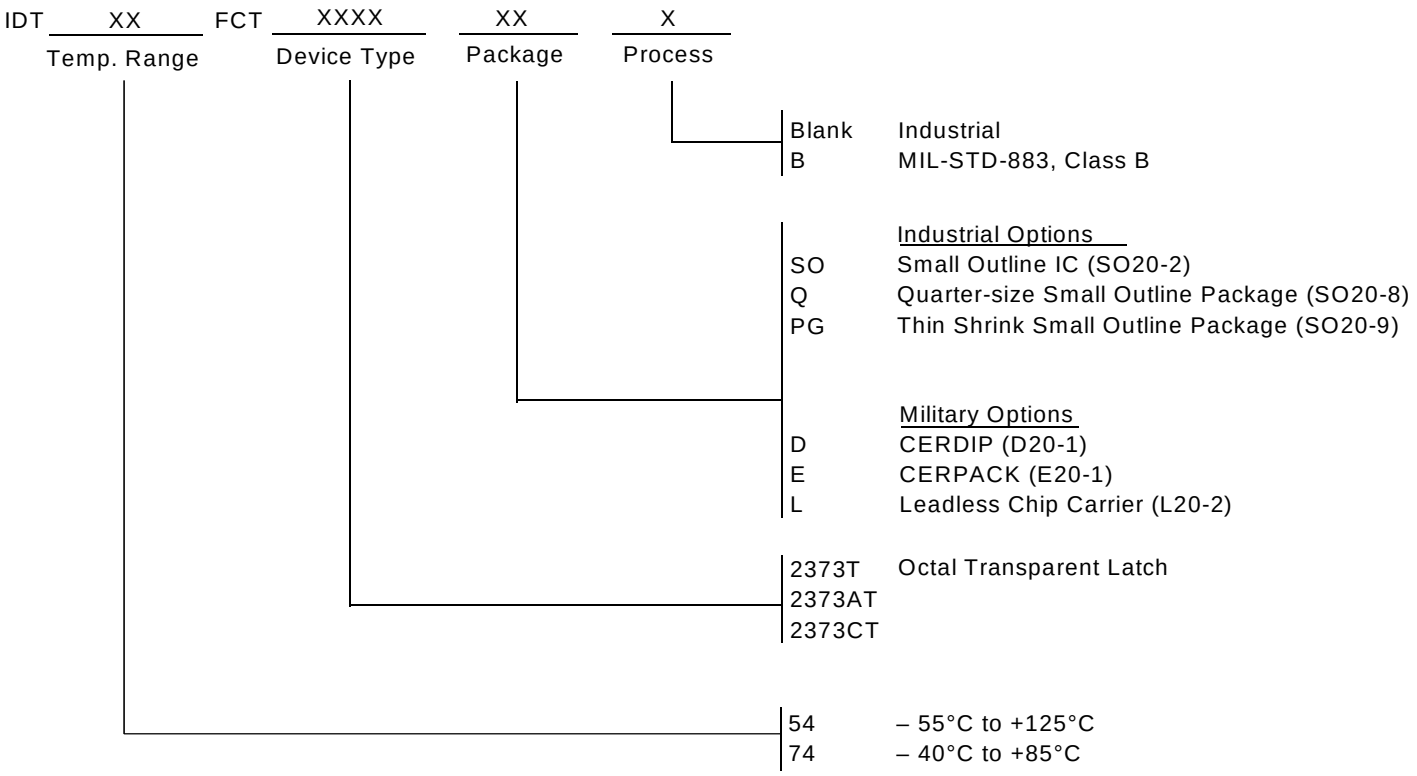
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



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