

TENTATIVE

TOSHIBA MULTI CHIP DISCRETE DEVICE

**HN7G01FU**

POWER MANAGEMENT SWITCH APPLICATION

DRIVER CIRCUIT APPLICATION

INTERFACE CIRCUIT APPLICATION

Q1 (Transistor) : 2SA1955 Equivalent

Q2 (MOS-FET) : 2SK1830 Equivalent

Q1 (Transistor) MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Collector-Base Voltage	V <sub>CB0</sub>	-15	V
Collector-Emitter Voltage	V <sub>CEO</sub>	-12	V
Emitter-Base Voltage	V <sub>EB0</sub>	-5	V
Collector Current	I <sub>C</sub>	-400	mA
Base Current	I <sub>B</sub>	-50	mA

Q2 (MOS-FET) MAXIMUM RATINGS (Ta = 25°C)

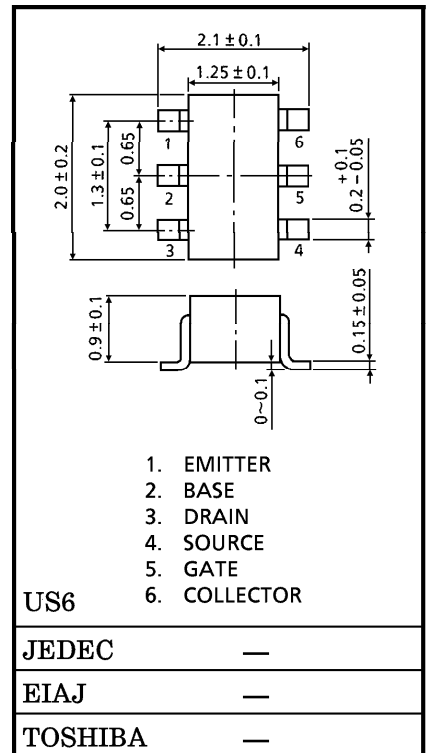
CHARACTERISTIC	SYMBOL	RATING	UNIT
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	10	V
Drain Current	I <sub>D</sub>	50	mA

Q1, Q2 COMMON RATINGS (Ta = 25°C)

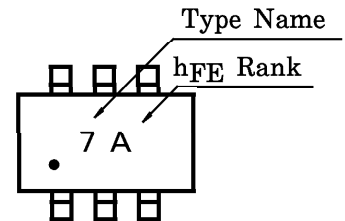
CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Dissipation	P <sub>C</sub> (*)	200	mW
Junction Temperature	T <sub>j</sub>	125	°C
Storage Temperature Range	T <sub>stg</sub>	-55~125	°C

(\*) Total Rating

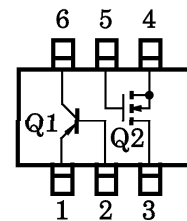
Unit in mm



MARKING



PIN ASSIGNMENT (TOP VIEW)



Q1 (Transistor) ELECTRICAL CHARACTERISTICS (Ta = 25°C)

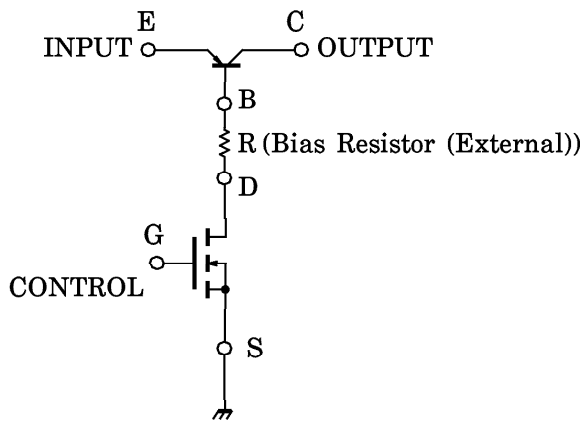
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut-off Current	$I_{CBO}$	$V_{CB} = -15\text{ V}, I_E = 0$	—	—	-0.1	$\mu\text{A}$
Emitter Cut-off Current	$I_{EBO}$	$V_{EB} = -5\text{ V}, I_C = 0$	—	—	-0.1	mA
DC Current Gain	$h_{FE} (*)$	$V_{CE} = -2\text{ V}, I_C = -10\text{ mA}$	300	—	1000	
Collector-Emitter Saturation Voltage	$V_{CE(sat)} (1)$	$I_C = -10\text{ mA}, I_B = -0.5\text{ mA}$	—	-15	-30	mV
	$V_{CE(sat)} (2)$	$I_C = -200\text{ mA}, I_B = -10\text{ mA}$	—	-110	-250	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = -200\text{ mA}, I_B = -10\text{ mA}$	—	-0.87	-1.2	V

(\*)  $h_{FE}$  Classification    A : 300~600, B : 500~1000

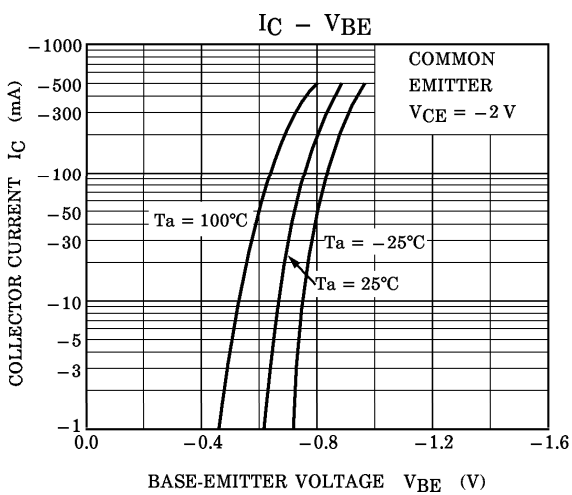
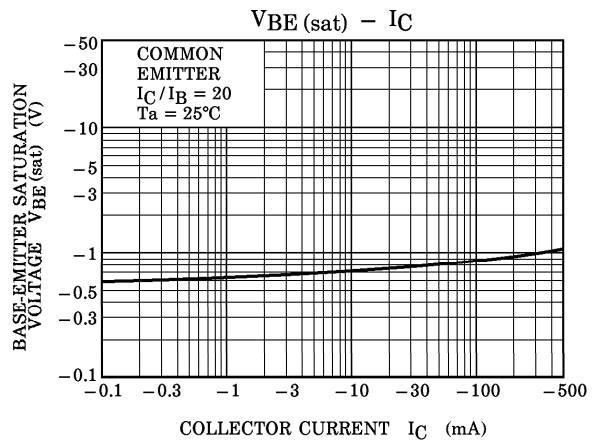
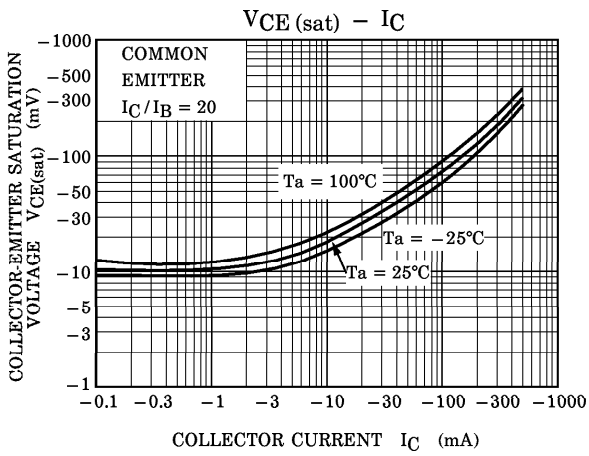
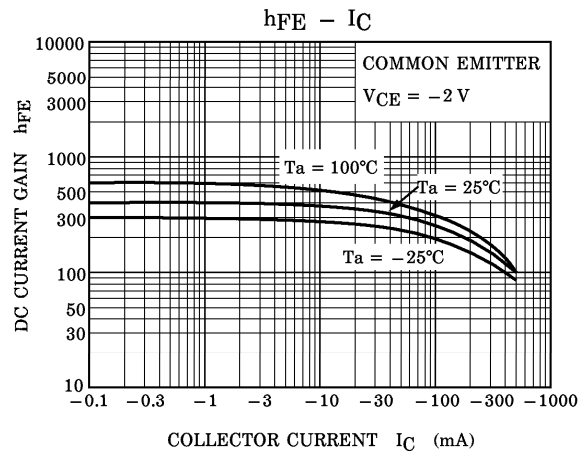
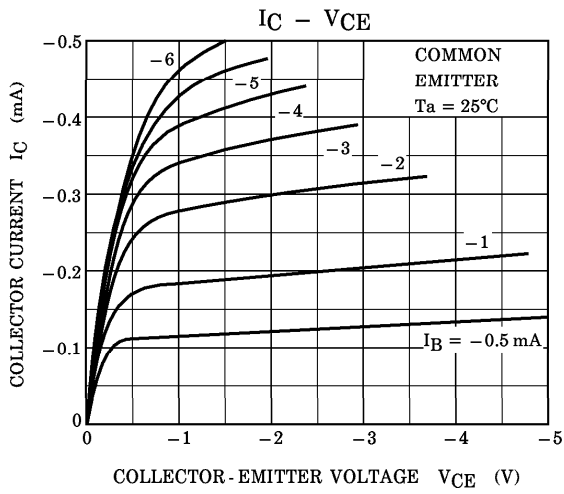
Q2 (MOS-FET) ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current	$I_{GSS}$	$V_{GS} = 10\text{ V}, V_{DS} = 0$	—	—	1	$\mu\text{A}$
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 100\ \mu\text{A}, V_{GS} = 0$	20	—	—	V
Drain Current	$I_{DSS}$	$V_{DS} = 20\text{ V}, V_{GS} = 0$	—	—	1	$\mu\text{A}$
Gate Threshold Voltage	$V_{th}$	$V_{DS} = 3\text{ V}, I_D = 0.1\text{ mA}$	0.5	—	1.5	V
Forward Transfer Admittance	$ Y_{fs} $	$V_{DS} = 3\text{ V}, I_D = 10\text{ mA}$	20	—	—	mS
Drain-Source ON Resistance	$R_{DS(ON)}$	$I_D = 10\text{ mA}, V_{GS} = 2.5\text{ V}$	—	20	40	$\Omega$

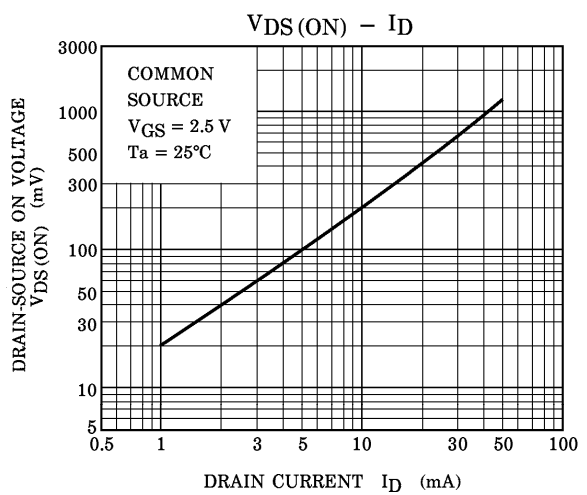
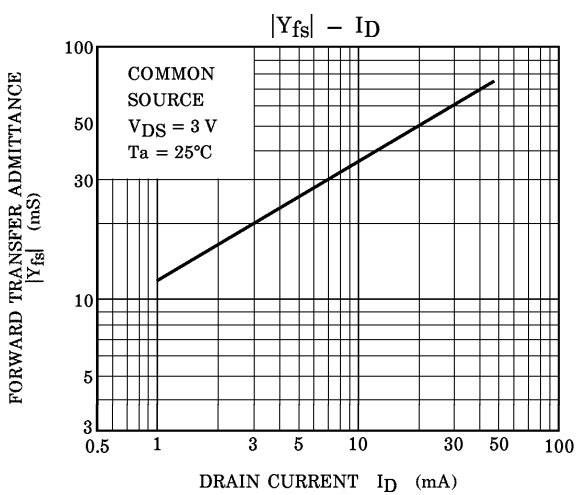
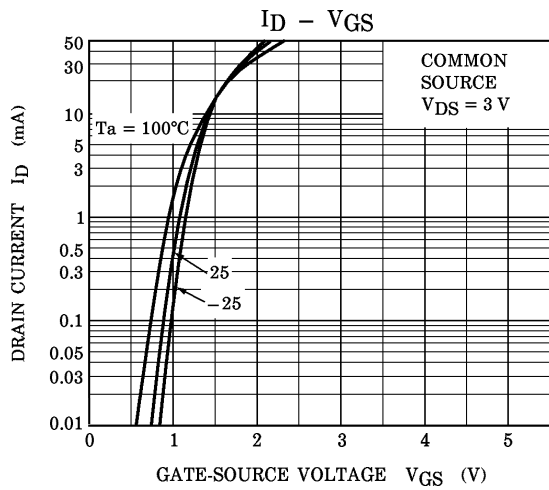
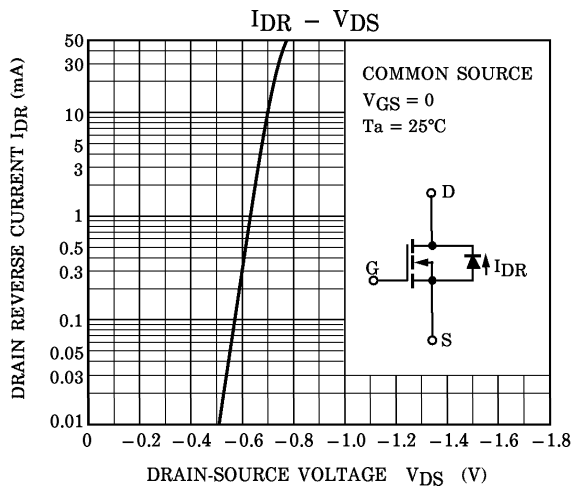
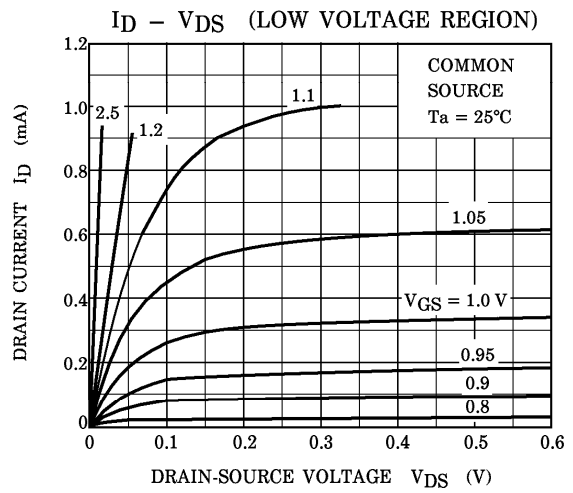
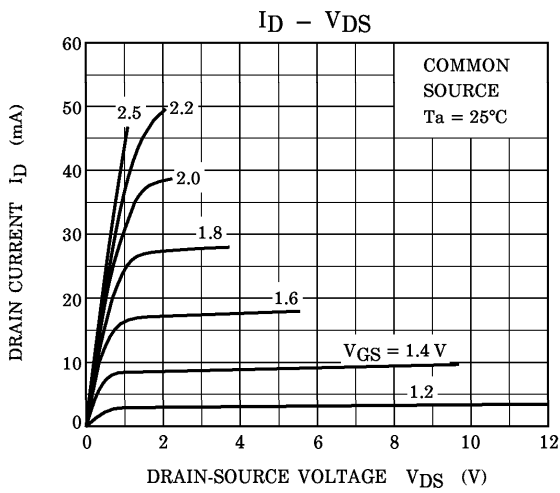
APPLICATION EXAMPLE (Power Management Switch)



○ Transistor



○ MOS-FET



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