

# MC10134

## Dual Multiplexer With Latch

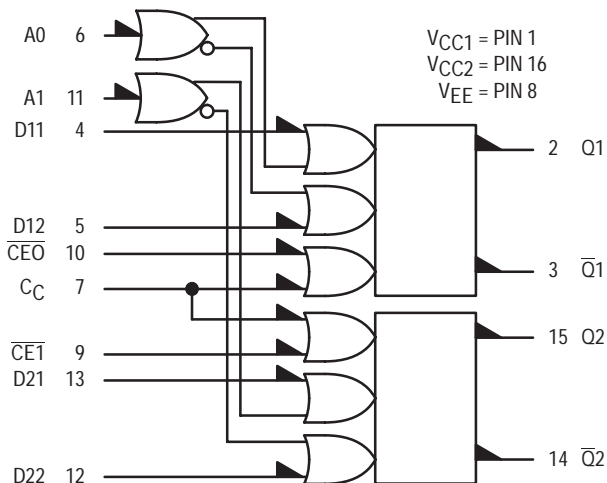
The MC10134 is a dual multiplexer with clocked D type latches. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ( $\overline{CE}$ ) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock ( $C_C$ ).

The data select inputs determine which data input is enabled. A high (H) level on the A0 input enables data input D12 and a low (L) level on the A0 input enables data input D11. A high (H) level on the A1 input enables data input D22 and a low (L) level on the A1 input enables data input D21.

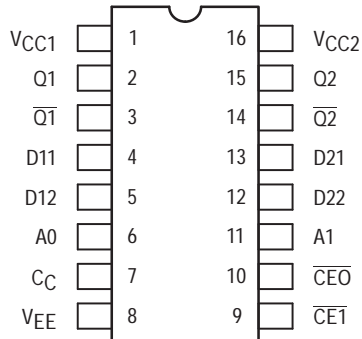
Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

- $P_D = 225$  mW typ/pkg (No Load)
- $t_{pd} = 3.0$  ns typ
- $t_r, t_f = 2.5$  ns typ (20%–80%)

### LOGIC DIAGRAM



### DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.

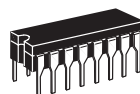
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



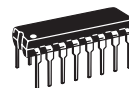
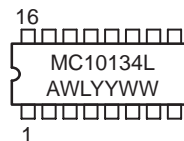
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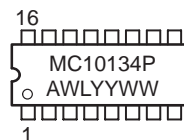
### MARKING DIAGRAMS



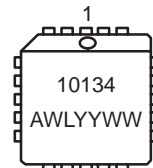
CDIP-16  
L SUFFIX  
CASE 620



PDIP-16  
P SUFFIX  
CASE 648



PLCC-20  
FN SUFFIX  
CASE 775



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### TRUTH TABLE

C	A0	D11	D12	$Q_{n+1}$
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	$Q_n$

$$C = \overline{CE} + C_C$$

### ORDERING INFORMATION

Device	Package	Shipping
MC10134L	CDIP-16	25 Units / Rail
MC10134P	PDIP-16	25 Units / Rail
MC10134FN	PLCC-20	46 Units / Rail

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## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I <sub>E</sub>	8		60			55		60	mAdc
Input Current	I <sub>inH</sub>	4		460			290		290	μAdc
		5		460			290		290	
		6		425			265		265	
		7		460			290		290	
		10		425			265		265	
	I <sub>inL</sub>	4*	0.5		0.5			0.3		μAdc
Output Voltage      Logic 1	V <sub>OH</sub>	2	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	Vdc
		2	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	
Output Voltage      Logic 0	V <sub>OL</sub>	2	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	Vdc
		2	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	
Threshold Voltage      Logic 1	V <sub>OHA</sub>	2	−1.080		−0.980			−0.910		Vdc
		2	−1.080		−0.980			−0.910		
Threshold Voltage      Logic 0	V <sub>OLA</sub>	2		−1.655			−1.630		−1.595	Vdc
		2		−1.655			−1.630		−1.595	
Switching Times (50Ω Load)										
Propagation Delay	Data	t <sub>4+2+</sub>	2	1.0	3.5	1.0	3.3	1.0	3.6	ns
	Clock	t <sub>10−2+</sub>	2	1.0	6.0	1.0	5.7	1.0	6.3	
	Select	t <sub>6+2+</sub>	2	1.0	4.8	1.0	4.6	1.0	5.0	
Setup Time	Data	t <sub>setup</sub>	2	2.5		2.5		2.5		
	Select	t <sub>setup</sub>	2	3.5		3.5		3.5		
Hold Time	Data	t <sub>hold</sub>	2	1.5		1.5		1.5		
	Select	t <sub>hold</sub>	2	1.0		1.0		1.0		
Rise Time      (20 to 80%)		t <sub>2+</sub>	2	1.5	3.7	1.5	3.5	1.5	3.8	
Fall Time      (20 to 80%)		t <sub>2−</sub>	2	1.5	3.7	1.5	3.5	1.5	3.8	

\* All other inputs tested in the same manner.

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## ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					(V <sub>CC</sub> ) Gnd
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>	
			–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
			+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
			+85°C	–0.700	–1.825	–1.035	–1.440	–5.2
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V <sub>CC</sub> ) Gnd
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>	
Power Supply Drain Current	I <sub>E</sub>	8					8	1, 16
Input Current	I <sub>inH</sub>	4	4				8	1, 16
		5	5				8	1, 16
		6	6				8	1, 16
		7	7					
		10	10					
	I <sub>inL</sub>	4*		4			8	1, 16
Output Voltage	Logic 1	2	4	6,7,10			8	1, 16
		2	5,6	7,10			8	1, 16
Output Voltage	Logic 0	2		4,6,7,10			8	1, 16
		2	6	5,7,10			8	1, 16
Threshold Voltage	Logic 1	2		6,7,10	4		8	1, 16
		2	6	7,10	5		8	1, 16
Threshold Voltage	Logic 0	2		6,7,10		4	8	1, 16
		2	6	7,10		5	8	1, 16
Switching Times (50Ω Load)			+1.11 V	+0.31 V	Pulse In	Pulse Out	–3.2 V	+2.0 V
Propagation Delay	Data	t <sub>4+2+</sub>	2	6,7,10	4	2	8	1, 16
	Clock	t <sub>10–2+</sub>	2	4	7	10	8	1, 16
	Select	t <sub>6+2+</sub>	2	5	7,10	6	8	1, 16
Setup Time	Data	t <sub>setup</sub>	2	6,7	4,10	2	8	1, 16
	Select	t <sub>setup</sub>	2	5	7,11	6,10	8	1, 16
Hold Time	Data	t <sub>hold</sub>	2	6,7	4,10	2	8	1, 16
	Select	t <sub>hold</sub>	2	5	7,11	6,10	8	1, 16
Rise Time (20 to 80%)		t <sub>2+</sub>	2	6,7,10	4	2	8	1, 16
Fall Time (20 to 80%)		t <sub>2–</sub>	2	6,7,10	4	2	8	1, 16

\* All other inputs tested in the same manner.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

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## PACKAGE DIMENSIONS

PLCC-20  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 775-02  
ISSUE C



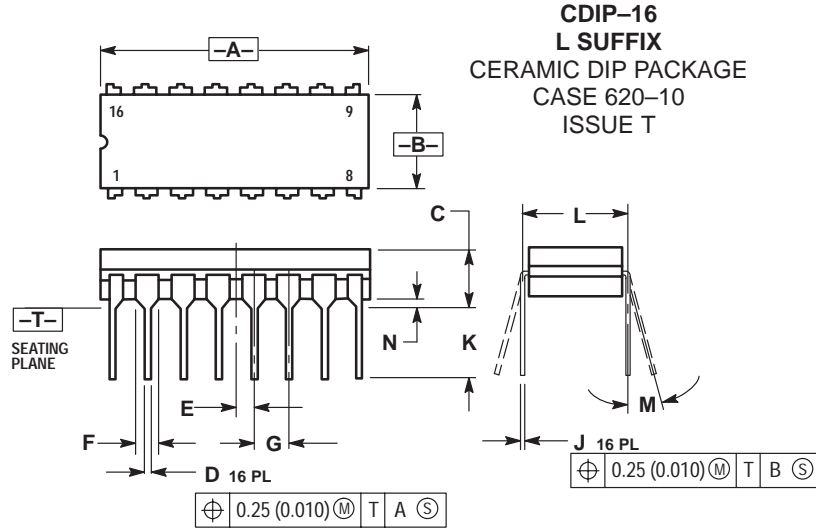
### NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

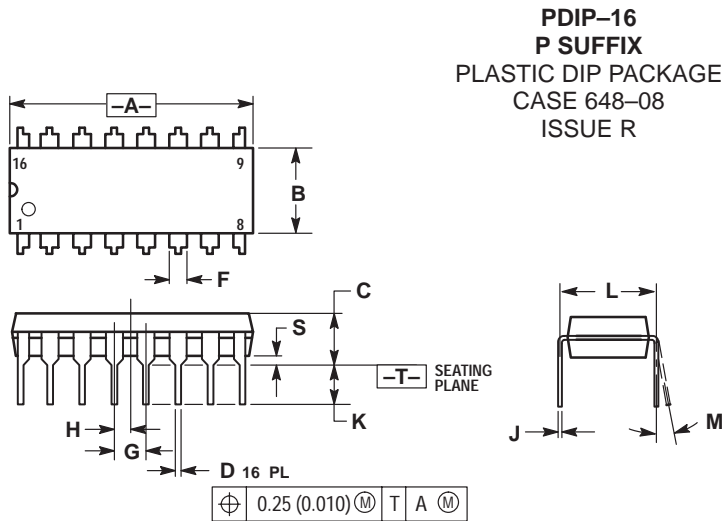
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## PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

## **Notes**

## **Notes**

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