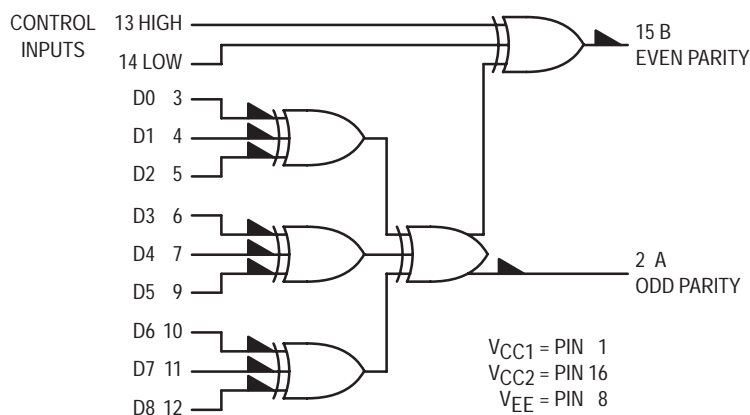# MC10170

9+2-Bit Parity Generator/ Checker

The MC10170 is a 11–bit parity circuit, which is segmented into 9 data bits and 2 control bits.

Output A generates odd parity on 9 bits; that is, Output A goes high for an odd number of high logic levels on the bit inputs in only 2 gate delays.

The Control Inputs can be used to expand parity to larger numbers of bits with minimal delay or can be used to generate even parity. To expand parity to larger words, the MC10170 can be used with the MC10160 or other MC10170's. The MC10170 can generate both even and odd parity.

- P_D = 300 mW typ/pkg (No Load)
- t_{pd} = 2.5 ns typ (Control Inputs to B Output)
    4.0 ns typ (Data Inputs to A Output)
    6.0 ns typ (Data Inputs to B Output)
- t_r, t_f = 2.0 ns typ (20%–80%)

MARKING DIAGRAMS

CDIP–16
L SUFFIX
CASE 620

```
MC10170L
AWLYYWW
```
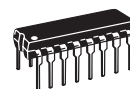
PDIP–16
P SUFFIX
CASE 648

```
MC10170P
AWLYYWW
```
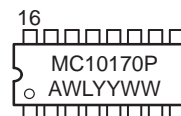
PLCC–20
FN SUFFIX
CASE 775

```
10170
AWLYYWW
```
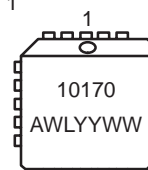
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

LOGIC DIAGRAM

CONTROL INPUTS

13 HIGH
14 LOW

15 B EVEN PARITY

D0 3
D1 4
D2 5

D3 6
D4 7
D5 9

2 A ODD PARITY

D6 10
D7 11
D8 12

V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

INPUTS	OUTPUTS	
Sum of D Inputs at High Level	Odd Parity Output A	Even Parity Output B
Even	Low	High
Odd	High	Low

DIP PIN ASSIGNMENT

V_{CC1}	1	16	V_{CC2}
A	2	15	B
D0	3	14	LOW
D1	4	13	HIGH
D2	5	12	D8
D3	6	11	D7
D4	7	10	D6
V_{EE}	8	9	D5
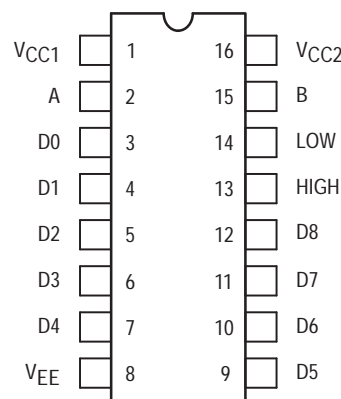
Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

ORDERING INFORMATION

Device	Package	Shipping
MC10170L	CDIP–16	25 Units / Rail
MC10170P	PDIP–16	25 Units / Rail
MC10170FN	PLCC–20	46 Units / Rail

March, 2000 – Rev. 7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		78		57	71		78	mAdc
Input Current	I_{inH}	3 5		350 350			200 220		220 220	µAdc
	I_{inL}	3	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 15	−1.060 −1.060	−0.890 −0.890	−0.960 −0.960		−0.810 −0.810	−0.890 −0.890	−0.700 −0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 15	−1.890 −1.890	−1.675 −1.675	−1.850 −1.850		−1.650 −1.650	−1.825 −1.825	−1.615 −1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 15	−1.080 −1.080		−0.980 −0.980			−0.910 −0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 15		−1.655 −1.655			−1.630 −1.630		−1.595 −1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{13+15+} t_{14-15-} t_{3+2-} t_{3-15+}	15 15 2 15	1.5 1.5 2.0 4.0	4.2 4.2 6.6 9.5	1.5 1.5 2.0 4.0	2.5 2.5 4.0 6.0	4.0 4.0 6.0 8.8	1.5 1.5 2.0 4.0	4.4 4.4 6.6 9.5	
Rise Time (20 to 80%)	t_{2+}	2	1.5	4.3	1.5	2.0	3.9	1.5	4.3	
Fall Time (20 to 80%)	t_{2-}	2	1.5	4.3	1.5	2.0	3.9	1.5	4.3	

MC10170

ELECTRICAL CHARACTERISTICS (continued)

				TEST VOLTAGE VALUES (Volts)					
		@ Test Temperature		V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
		−30°C		−0.890	−1.890	−1.205	−1.500	−5.2	
		+25°C		−0.810	−1.850	−1.105	−1.475	−5.2	
		+85°C		−0.700	−1.825	−1.035	−1.440	−5.2	
		Pin Under Test	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**						
Characteristic	**Symbol**		V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	**(V_{CC}) Gnd**
Power Supply Drain Current	I_E	8						1, 16
Input Current	I_{inH}	3 5	3 5				8 8	1, 16 1, 16
	I_{inL}	3		3			8	1, 16
Output Voltage Logic 1	V_{OH}	2 15	3, 4, 5 14				8 8	1, 16 1, 16
Output Voltage Logic 0	V_{OL}	2 15	4, 5 13, 14				8 8	1, 16 1, 16
Threshold Voltage Logic 1	V_{OHA}	2 15			5 13		8 8	1, 16 1, 16
Threshold Voltage Logic 0	V_{OLA}	2 15				5 13	8 8	1, 16 1, 16
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**	**−3.2 V**	**+2.0**
Propagation Delay	t_{13+15+} $t_{14−15−}$ $t_{3+2−}$ $t_{3−15+}$	15 15 2 15			13 14 3 3	15 15 2 15	8 8 8 8	1, 16 1, 16 1, 16 1, 16
Rise Time (20 to 80%)	t_{2+}	2			3	2	8	1, 16
Fall Time (20 to 80%)	$t_{2−}$	2			3	2	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

PACKAGE DIMENSIONS

PLCC–20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE C

VIEW D–D

VIEW S

NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	----	0.51	----
K	0.025	----	0.64	----
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	----	0.020	----	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	----	1.02	----

MC10170

PACKAGE DIMENSIONS
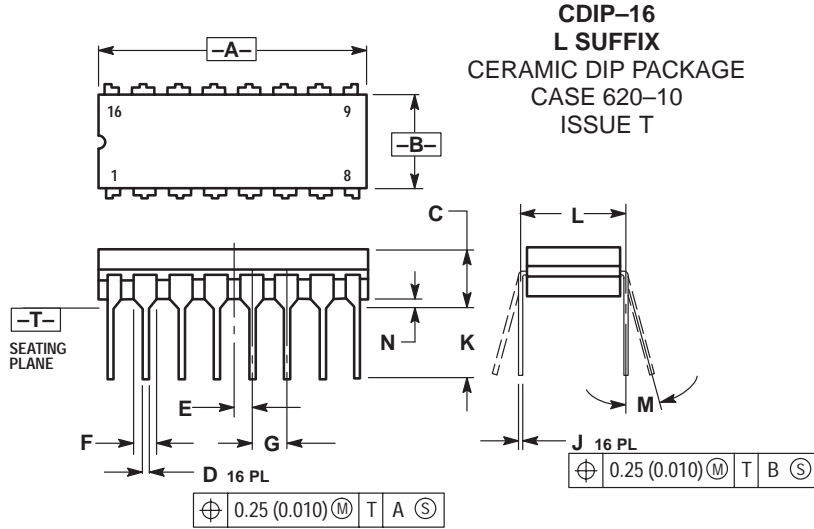
CDIP–16
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE T

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	----	0.200	----	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01
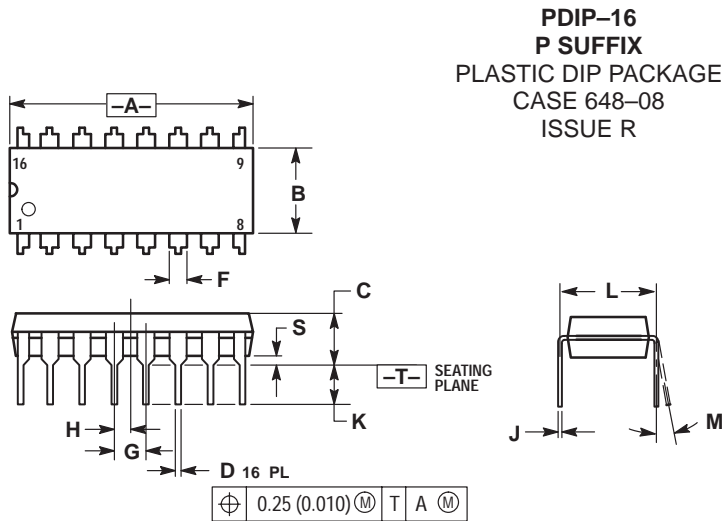
PDIP–16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

<u>Notes</u>

<u>Notes</u>

PUBLICATION ORDERING INFORMATION