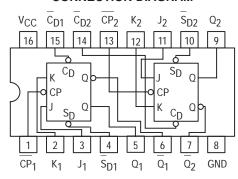


DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

The MC74F112 contains two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on SD or CD prevents clocking and forces Q or Q HIGH_respectively. Simultaneous LOW signals on SD and CD force both Q and Q HIGH.

CONNECTION DIAGRAM



FUNCTION TABLE (Each Half)

Inputs	Output				
@ t _n	@ t _n + 1				
J K	Q				
L L	Q _n				
L H	L				
H L	Н				
н н	Q _n				

Asynchronous Inputs:

LOW Input to SD sets Q to HIGH level

LOW Input to $\overline{\mathsf{C}}_D$ sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on $\overline{\mathsf{C}}_D$ and $\overline{\mathsf{S}}_D$ makes both Q and $\overline{\mathsf{Q}}$ HIGH

H = HIGH Voltage Level

L = LOW Voltage Level

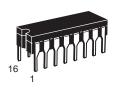
t_n = Bit time before clock pulse

 $t_n + 1$ = Bit time after clock pulse

MC74F112

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

FAST™ SCHOTTKY TTL



J SUFFIX CERAMIC CASE 620-09



N SUFFIX PLASTIC CASE 648-08

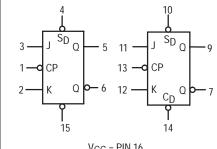


D SUFFIX SOIC CASE 751B-03

ORDERING INFORMATION

MC74FXXXJ Ceramic MC74FXXXN Plastic MC74FXXXD SOIC

LOGIC SYMBOL

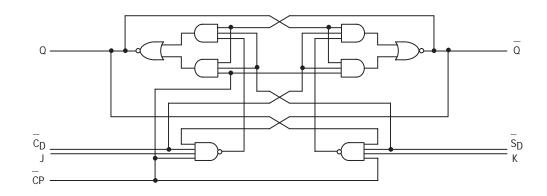


V_{CC} = PIN 16 GND = PIN 8

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LOGIC DIAGRAM (one half shown)



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Тур	Max	Unit
VCC	Supply Voltage	74	4.5	5.0	5.5	V
TA	Operating Ambient Temperature Range	74	0	25	70	°C
ЮН	Output Current — High	74			-1.0	mA
loL	Output Current — Low	74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

			Limits							
Symbol	Parameter		Min Typ		Max	Unit	Test Conditions			
VIH	Input HIGH Voltage					V	Guaranteed Input HIGH Voltage			
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage			
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN		
		74	2.5	3.4		V	$I_{OH} = -1.0 \text{ mA}$	V _{CC} = 4.50 V		
Vон	Output HIGH Voltage	74	2.7	3.4		V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V		
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA V _{CC} = MIN			
liH	Input LOW Current (J and K Inputs)				20	μΑ	$V_{CC} = MAX, V_{IN} = 2.7 V$			
					100	μΑ	V _{CC} = MAX, V _{IN} = 7.0 V			
					-0.6	mA				
I _{IL}					-2.4	mA	V _{CC} = MAX, V _{IN} = 0.5 V			
	(C _D and S _D Inputs)				-3.0	mA	1			
los	Output Short Circuit Current (No	-60		-150	mA	V _{CC} = MAX, V _{OUT} =	: 0 V			
ICC	Power Supply Current		12	19	mA	V _{CC} = MAX, V _{CP} = 0) V			

NOTES:

- 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

MC74F112

AC CHARACTERISTICS

		74F T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		74F T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
Symbol	Parameter	Min	Max	Min	Max	Unit
f _{max}	Maximum Clock Frequency	110				MHz
^t PLH	Propagation Delay	2.0	6.5	2.0	7.5	
^t PHL	\overline{CP}_{n} to Q_{n} or \overline{Q}_{n}	2.0	6.5	2.0	7.5	ns
^t PLH	Propagation Delay	2.0	6.5	2.0	7.5	
^t PHL	C _{Dn} or S _{Dn} to Q _n or Q _n	2.0	6.5	2.0	7.5	ns

AC OPERATING REQUIREMENTS

			74F T _A = +25°C			74F T _A = 0°C to +70°C			Ł
									Į
			V _{CC} = +5.0 V			V _{CC} = 5.0 V ± 10%			1
	Symbol	Parameter	Min	Тур	Max	Min	Max	Unit	4
	t _S (H)	Setup Time, HIGH or LOW	4.0			4.0			1
	$t_S(L)$	J_n or K_n to \overline{CP}_n	3.0			3.0		20	Ι
	t _h (H)	Hold Time, HIGH or LOW	0			0		ns	
	t _h (L)	J_n or K_n to \overline{CP}_n	0			0			
	t _W (H)	CP _n Pulse Width, HIGH	4.5			4.5		ns	I
ı	t_W (L)	or LOW	4.5			4.5		115	
	t_W (L)	C _{Dn} or S _{Dn} Pulse Width, LOW	4.5			4.5		ns	1
	t _{rec}	Recovery Time CDn or SDn to CP	4.0			5.0		ns	

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