

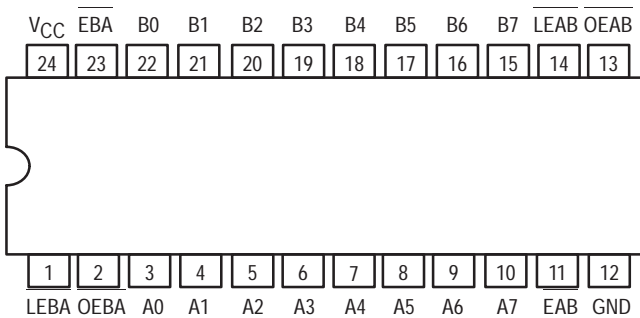


OCTAL REGISTERED TRANSCEIVER, NON-INVERTING, 3-STATE

The MC74F543 Octal Registered Transceivers contain two sets of data flowing in either direction. Separate Latch Enable (LEAB, LEBA) and Enable (OEAB, OEBA) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The MC74F543 has a noninverting data path. The A outputs are guaranteed to sink 20 mA while the B outputs are rated for 64 mA.

- Combines 74F245 and 74F373 Type Functions in One Chip
- 8-Bit Octal Transceiver
- Non-Inverting
- Back-to-Back Registers for Storage
- Separate Controls for Data Flow in Each Direction
- Glitchless Outputs During 3-State Power Up or Power Down Operation
- High Impedance Outputs in Power Off State
- A Outputs Sink 24 mA and Source 3.0 mA
- B Outputs Sink 64 mA and Source 15 mA
- See F544 for Inverting Version
- ESD Protection > 4000 Volts

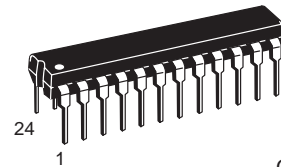
PIN ASSIGNMENT



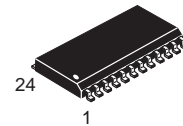
MC74F543

**OCTAL REGISTERED
TRANSCEIVER,
NON-INVERTING, 3-STATE**

FAST™ SCHOTTKY TTL



**N SUFFIX
PLASTIC
CASE 724-03**



**DW SUFFIX
SOIC
CASE 751E-03**

ORDERING INFORMATION

MC74FXXXN Plastic
MC74FXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.5	V
T _A	Operating Ambient Temperature Range	74	0	70	°C
I _{OH}	Output Current — High	74		-3.0/-15	mA
I _{OL}	Output Current — Low	74		24/64	mA

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FUNCTION TABLE

Inputs				Outputs	Status
OEXX	EXX	LEXX	Data		
H	X	X	X	Z	Outputs disabled
L	H	L	l	Z	Outputs disabled
L	H	L	h	Z	Data latched
L	L	H	l	L	Data latched
L	L	H	h	H	Data latched
L	L	L	L	L	Transparent
L	L	L	H	H	Transparent

H = HIGH voltage level; h = HIGH state must be present one set-up time before the LOW-to-HIGH transition of LEXX or EXX (XX = AB or BA); L = LOW Voltage Level; l = LOW state must be present one set-up time before the LOW-to-HIGH transition of LEXX or EXX (XX = AB or BA); X = Don't care; Z = HIGH impedance state.

FUNCTIONAL DESCRIPTION

The MC74F543 contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable (EAB) Input must be LOW in order to enter data from A0–A7 or take data from B0–B7, as indicated in the Function Table. With EAB LOW, a LOW signal on the A-to-B Latch Enable (LEAB) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH

transition of the LEAB signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With EAB and OEAB both LOW, the 3-State B output buffers are active and reflects the data present at the output of the A latches. Control of data flow from B to A is similar, but using the EBA, LEBA, and OEBA inputs.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions		
			Min	Typ	Max				
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage		
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage		
V _{IK}	Input Clamp Diode Voltage			-0.73	-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA		
V _{OH}	Output HIGH Voltage	A0–A7	74	2.4		V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V	
		B0–B7	74	2.7	3.4	V	I _{OH} = -15 mA	V _{CC} = 4.75 V	
V _{OL}	Output LOW Voltage	A0–A7	74		0.35	0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
		B0–B7	74		0.4	0.55	V	I _{OL} = 64 mA	
I _{IH}	Input HIGH Current		I/O Pins			1.0	mA	V _{CC} = MAX, V _{IN} = 5.5 V	
			Control Pins			100	20	μA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current		EAB, EBA			-1.2	mA	V _{CC} = MAX, V _{IN} = 0.5 V	
			Other Inputs			-0.6			
I _{OZH}	Off-State Output Current, High-Level Voltage Applied					70	μA	V _{CC} = MAX	V _{OUT} = 2.7 V
						1.0	mA		V _{OUT} = 5.5 V
I _{OZL}	Off-State Output Current, Low-Level Voltage Applied					-600	μA	V _{CC} = MAX, V _{OUT} = 0.5 V	
I _{OS}	Output Short Circuit Current (Note 2)		A _n Outputs	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V	
			B _n Outputs	-100		-225			
I _{CC}	Total Supply Current		I _{CC} H		70	100	mA	V _{CC} = MAX	
			I _{CC} L		95	125			
			I _{CC} Z		95	125			

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	70	100		70		MHz
t _{PLH} t _{PHL}	Propagation Delay Transparent Mode A _n to B _n or B _n to A _n	3.0 3.0	5.5 5.0	7.5 6.5	3.0 3.0	8.5 7.5	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to A _n	4.5 4.5	8.5 8.5	11 11	4.5 4.5	12.5 12.5	ns
t _{PLH} t _{PHL}	Propagation Delay LEAB to B _n	4.5 4.5	8.5 8.5	11 11	4.5 4.5	12.5 12.5	ns
t _{PZH} t _{PZL}	Output Enable Time to OEBA or OEAB to A _n or B _n EBA or EAB to A _n or B _n	3.0 4.0	7.0 7.5	9.0 10.5	3.0 4.0	10 12	ns
t _{PHZ} t _{PLZ}	Output Disable Time to OEBA or OEAB to A _n or B _n EBA or EAB to A _n or B _n	2.5 2.0	6.0 5.5	8.0 7.5	2.5 2.0	9.0 8.5	ns

AC OPERATING REQUIREMENTS

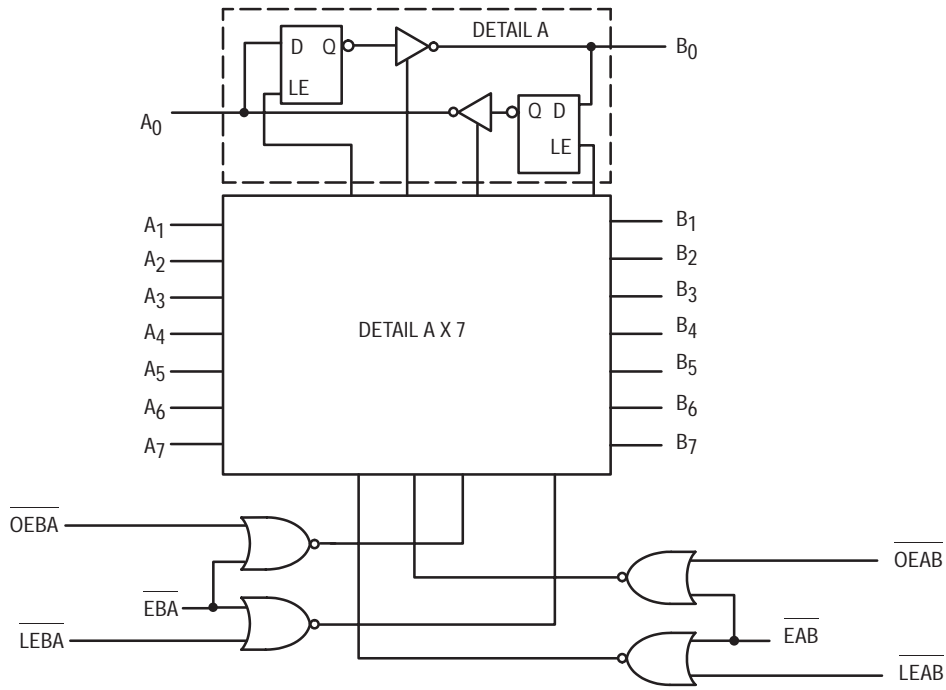
Symbol	Parameter	74F			74F			Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t _{s(H)} t _{s(L)}	Setup Time, <u>HIGH</u> or <u>LOW</u> A _n or B _n to LEBA or LEAB	3.0 3.0			3.5 3.5			ns
t _{h(H)} t _{h(L)}	Hold Time, <u>HIGH</u> or <u>LOW</u> A _n to B _n to LEBA or LEAB	3.0 3.0			3.5 3.5			ns
t _{w(L)}	Latch Enable, B to A Pulse Width, LOW	8.0			9.0			ns

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LOGIC DIAGRAM




NOTE:

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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