MC74VHC1GT86

2-Input Exclusive OR Gate / CMOS Logic Level Shifter
with LSTTL–Compatible Inputs

The MC74VHC1GT86 is an advanced high speed CMOS 2–input Exclusive OR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL–type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic–level translator from 3.0 V CMOS logic to 5.0V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high–voltage power supply.

The MC74VHC1GT86 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT86 to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when V_{CC} = 0 V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: t_{PD} = 4.8 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8 V; V_{IH} = 2.0 V
- CMOS–Compatible Outputs: V_{OH} > 0.8 V_{CC}; V_{OL} < 0.1 V_{CC} @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 83; Equivalent Gates = 16

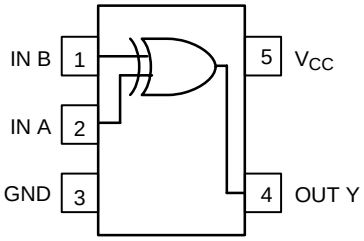

Figure 1. Pinout (Top View)

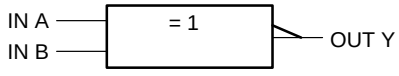

Figure 2. Logic Symbol

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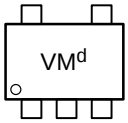
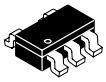
MARKING DIAGRAMS

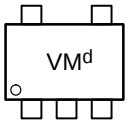
SC–88A / SOT–353/SC–70
DF SUFFIX
CASE 419A



Pin 1
d = Date Code

TSOP–5/SOT–23/SC–59
DT SUFFIX
CASE 483





Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT Y
5	V_{CC}

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS (Note 1.)

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage		–0.5 to +7.0	V
V_{IN}	DC Input Voltage		–0.5 to +7.0	V
V_{OUT}	DC Output Voltage	V_{CC} = 0 High or Low State	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current		–20	mA
I_{OK}	Output Diode Current	V_{OUT} < GND; V_{OUT} > V_{CC}	+20	mA
I_{OUT}	DC Output Current, per Pin		+25	mA
I_{CC}	DC Supply Current, V_{CC} and GND		+50	mA
P_D	Power dissipation in still air	SC–88A, TSOP–5	200	mW
θ_{JA}	Thermal resistance	SC–88A, TSOP–5	333	°C/W
T_L	Lead temperature, 1 mm from case for 10 s		260	°C
T_J	Junction temperature under bias		+150	°C
T_{stg}	Storage temperature		–65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 3.) Machine Model (Note 4.) Charged Device Model (Note 5.)	> 2000 > 200 N/A	V
$I_{Latch–Up}$	Latch–Up Performance	Above V_{CC} and Below GND at 125°C (Note 6.)	±500	mA

1. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
2. Derating – SC–88A Package: –3 mW/°C from 65° to 125°C
   – TSOP5 Package: –3 mW/°C from 65° to 125°C
3. Tested to EIA/JESD22–A114–A
4. Tested to EIA/JESD22–A115–A
5. Tested to JESD22–C101–A
6. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		3.0	5.5	V
V_{IN}	DC Input Voltage		0.0	5.5	V
V_{OUT}	DC Output Voltage	V_{CC} = 0 High or Low State	0.0 0.0	5.5 V_{CC}	V
T_A	Operating Temperature Range		–55	+125	°C
t_r , t_f	Input Rise and Fall Time	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

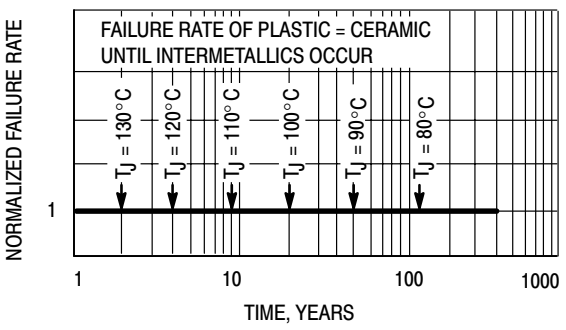


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$-55 \le T_A \le 125°C$ Min	$-55 \le T_A \le 125°C$ Max	Unit
V_{IH}	Minimum High–Level Input Voltage		3.0 4.5 5.5	1.4 2.0 2.0			1.4 2.0 2.0		1.4 2.0 2.0		V
V_{IL}	Maximum Low–Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50$ μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4$ mA $I_{OH} = -8$ mA	 3.0 4.5	 2.58 3.94			 2.48 3.80		 2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50$ μA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4$ mA $I_{OL} = 8$ mA	 3.0 4.5			 0.36 0.36		 0.44 0.44		 0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5$ V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Input: $V_{IN} = 3.4$ V	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	$V_{OUT} = 5.5$ V	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input $t_r = t_f$ = 3.0 ns

Symbol	Parameter	Test Conditions	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$-55 \le T_A \le 125°C$ Min	$-55 \le T_A \le 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input A or B to Y	$V_{CC} = 3.3 \pm 0.3$ V C_L = 15 pF C_L = 50 pF		5.0 6.2	11.0 14.5		13.0 16.5		15.5 19.5	ns
		$V_{CC} = 5.0 \pm 0.5$ V C_L = 15 pF C_L = 50 pF		3.1 4.2	6.8 8.8		8.0 10.0		10.0 12.0	
C_{IN}	Maximum Input Capacitance			5.5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 7.)	11	pF

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

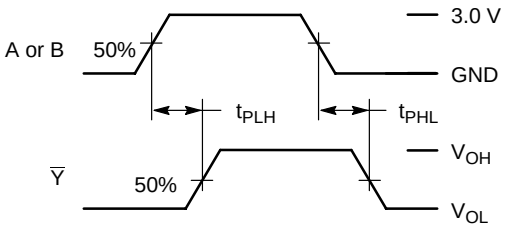
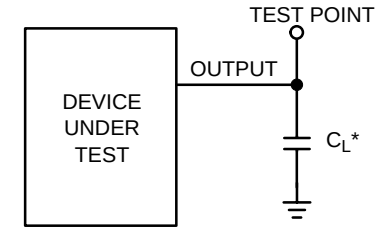


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance

Figure 5. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type (Name/SOT#/ Common Name)	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1GT86DFT1	MC	74	VHC1G	T86	DF	T1	SC–88A / SOT–353 / SC–70	178 mm (7”) 3000 Unit
MC74VHC1GT86DFT2	MC	74	VHC1G	T86	DF	T2	SC–88A / SOT–353 / SC–70	178 mm (7”) 3000 Unit
MC74VHC1GT86DFT4	MC	74	VHC1G	T86	DF	T4	SC–88A / SOT–353 / SC–70	330 mm (13”) 10,000 Unit
MC74VHC1GT86DTT1	MC	74	VHC1G	T86	DT	T1	TSOPS / SOT–23 / SC–59	178 mm (7”) 3000 Unit
MC74VHC1GT86DTT3	MC	74	VHC1G	T86	DT	T3	TSOPS / SOT–23 / SC–59	330 mm (13”) 10,000 Unit

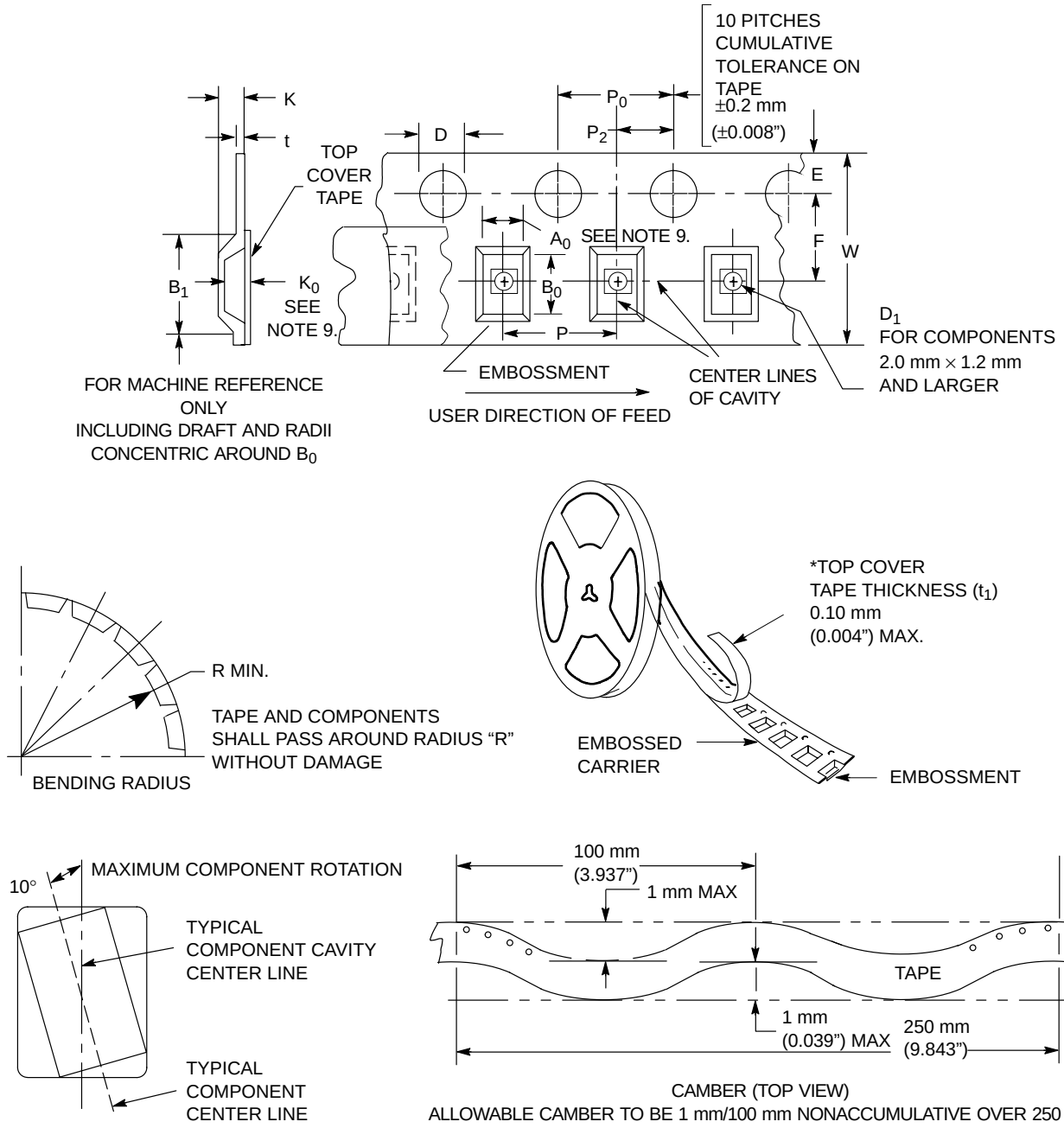


Figure 6. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 8. and 9.)

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R	T	W
8 mm	4.35 mm (0.171”)	1.5 +0.1/ –0.0 mm (0.059 +0.004/ –0.0”)	1.0 mm Min (0.039”)	1.75 ±0.1 mm (0.069 ±0.004”)	3.5 ±0.5 mm (1.38 ±0.002”)	2.4 mm (0.094”)	4.0 ±0.10 mm (0.157 ±0.004”)	4.0 ±0.1 mm (0.156 ±0.004”)	2.0 ±0.1 mm (0.079 ±0.002”)	25 mm (0.98”)	0.3 ±0.05 mm (0.01 +0.0038/ –0.0002”)	8.0 ±0.3 mm (0.315 ±0.012”)

8. Metric Dimensions Govern–English are in parentheses for reference only.
9. A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

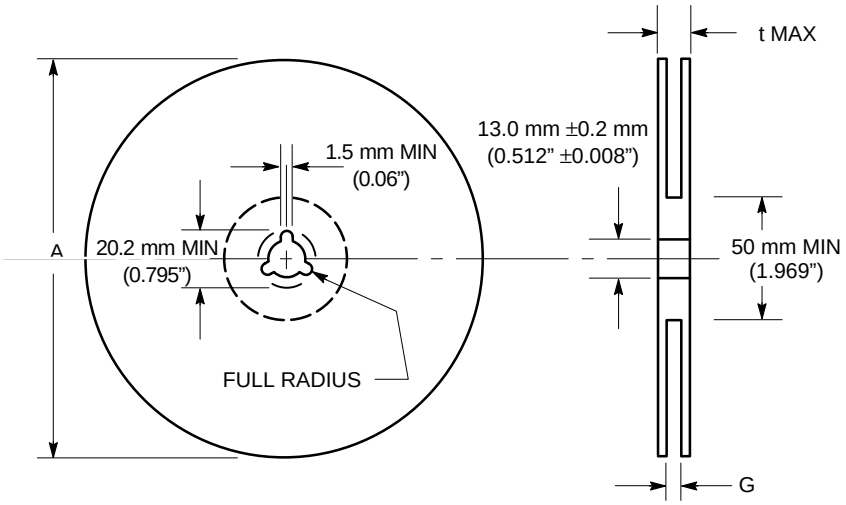


Figure 7. Reel Dimensions

REEL DIMENSIONS

Tape Size	T&R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7”)	8.4 mm, +1.5 mm, –0.0 (0.33” + 0.059”, –0.00)	14.4 mm (0.56”)
8 mm	T3, T4	330 mm (13”)	8.4 mm, +1.5 mm, –0.0 (0.33” + 0.059”, –0.00)	14.4 mm (0.56”)

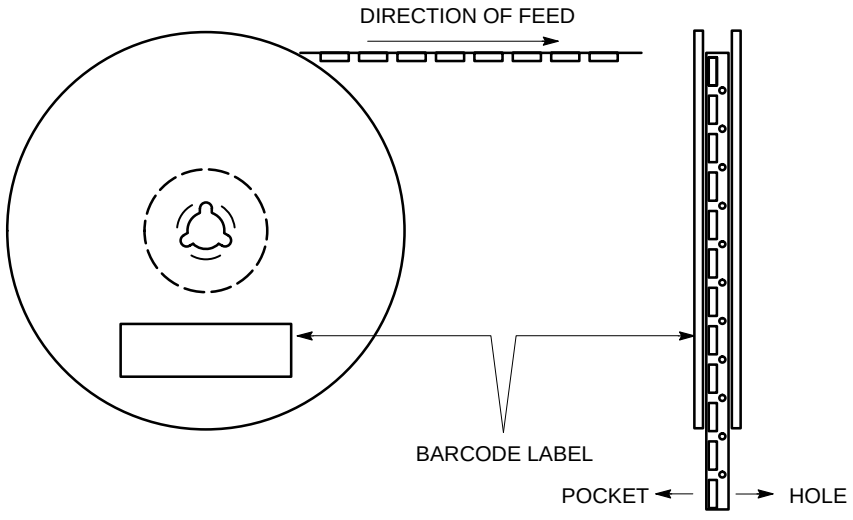


Figure 8. Reel Winding Direction

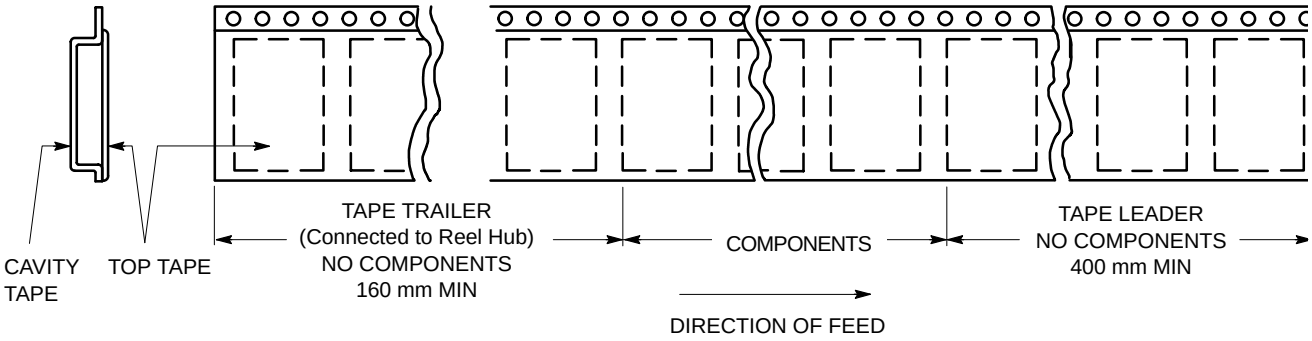


Figure 9. Tape Ends for Finished Goods

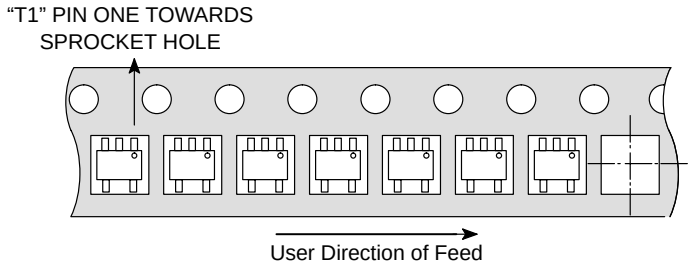


Figure 10. DFT1 (SC88A) Reel Configuration/Orientation

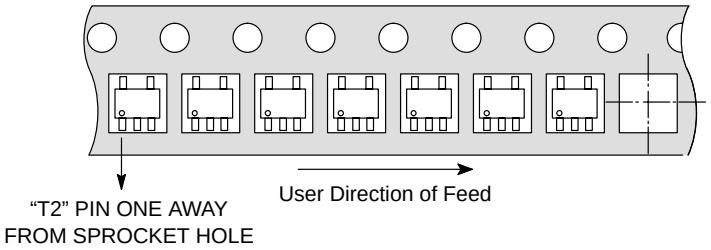


Figure 11. DFT2 and DFT4 (SC88A) Reel Configuration/Orientation

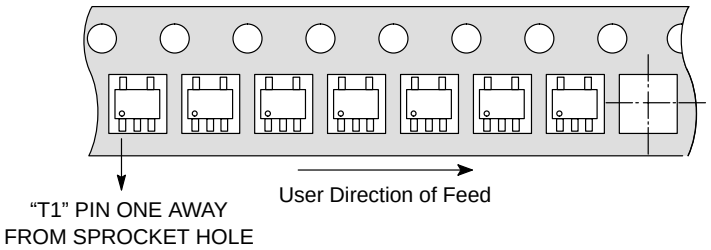
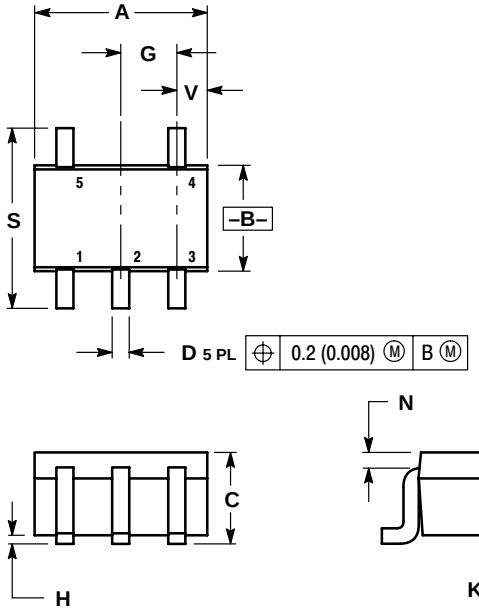


Figure 12. DTT1 and DTT3 (TSOP5) Reel Configuration/Orientation

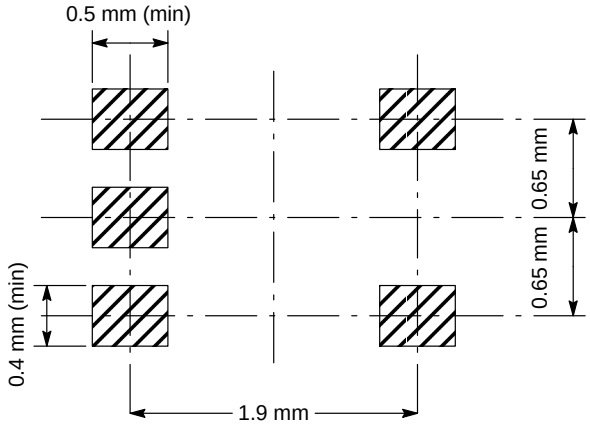
PACKAGE DIMENSIONS

SC–88A/SOT–353/SC–70
DF SUFFIX
5–LEAD PACKAGE
CASE 419A–01
ISSUE E



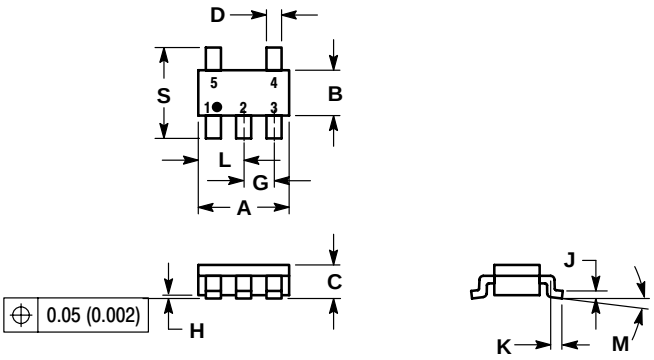
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40



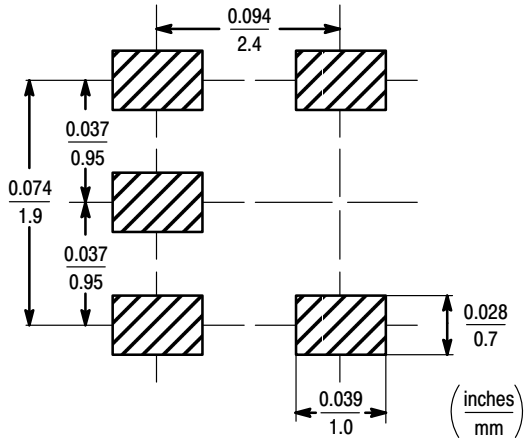
PACKAGE DIMENSIONS

TSOP–5/SOT–23/SC–59
DT SUFFIX
5–LEAD PACKAGE
CASE 483–01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.00	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181



Notes

Notes

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