

Product Preview

TMOS E-FET™

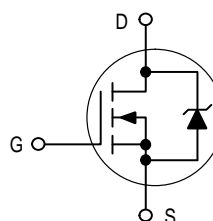
High Energy Power FET

N-Channel Enhancement-Mode Silicon Gate

D2PAK-SL Straight-Leaded Through Hole Mount Package

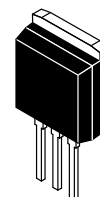
The D2PAK-SL package features a low profile design which allows it to be used in applications that require low profile components with higher power and lower $R_{DS(on)}$ capabilities. This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced TMOS E-FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Package Designed for Low Profile Through Hole Mount
- Robust High Voltage Termination
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation



MTB3N60E1

TMOS POWER FET
3.0 AMPERES
600 VOLTS
 $R_{DS(on)} = 2.2 \text{ OHMS}$



CASE 418C-01, Style 2
D2PAK-SL

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	600	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	600	Vdc
Gate-Source Voltage — Continuous — Non-repetitive	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	3.0 14	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75 0.6	Watts W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS ($T_J < 150^\circ\text{C}$)

Single Pulse Drain-to-Source Avalanche Energy — $T_J = 25^\circ\text{C}$ — $T_J = 100^\circ\text{C}$	$W_{DSR(1)}$	290 46	mJ
Repetitive Pulse Drain-to-Source Avalanche Energy	$W_{DSR(2)}$	7.5	

(1) $V_{DD} = 50 \text{ V}$, $I_D = 3.0 \text{ A}$

(2) Pulse Width and frequency is limited by $T_J(\text{max})$ and thermal response

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MTB3N60E1**THERMAL CHARACTERISTICS**

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 250\ \mu\text{Adc}$)	$V_{(BR)DSS}$	600	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 600\ \text{V}$, $V_{GS} = 0$) ($V_{DS} = 480\ \text{V}$, $V_{GS} = 0$, $T_J = 125^\circ\text{C}$)	I_{DSS}	— —	— —	0.25 1.0	mAdc
Gate-Body Leakage Current — Forward ($V_{GSF} = 20\ \text{Vdc}$, $V_{DS} = 0$)	I_{GSSF}	—	—	100	nAdc
Gate-Body Leakage Current — Reverse ($V_{GSR} = 20\ \text{Vdc}$, $V_{DS} = 0$)	I_{GSSR}	—	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{Adc}$) ($T_J = 125^\circ\text{C}$)	$V_{GS(th)}$	2.0 1.5	— —	4.0 3.5	Vdc
Static Drain-to-Source On-Resistance ($V_{GS} = 10\ \text{Vdc}$, $I_D = 1.5\ \text{A}$)	$R_{DS(on)}$	—	2.1	2.2	Ohms
Drain-to-Source On-Voltage ($V_{GS} = 10\ \text{Vdc}$) ($I_D = 3.0\ \text{A}$) ($I_D = 1.5\ \text{A}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— —	— —	9.0 7.5	Vdc
Forward Transconductance ($V_{DS} = 15\ \text{Vdc}$, $I_D = 1.5\ \text{A}$)	g_{FS}	1.5	—	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 25\ \text{V}$, $V_{GS} = 0$, $f = 1.0\ \text{MHz})$	C_{iss}	—	770	—	pF
Output Capacitance		C_{oss}	—	105	—	
Transfer Capacitance		C_{rss}	—	19	—	

SWITCHING CHARACTERISTICS*

Turn-On Delay Time	$(V_{DD} = 300\ \text{V}$, $I_D \approx 3.0\ \text{A}$, $R_L = 100\ \Omega$, $R_G = 12\ \Omega$, $V_{GS(on)} = 10\ \text{V})$	$t_{d(on)}$	—	23	—	ns
Rise Time		t_r	—	34	—	
Turn-Off Delay Time		$t_{d(off)}$	—	58	—	
Fall Time		t_f	—	35	—	
Total Gate Charge	$(V_{DS} = 420\ \text{V}$, $I_D = 3.0\ \text{A}$, $V_{GS} = 10\ \text{V})$	Q_g	—	28	31	nC
Gate-Source Charge		Q_{gs}	—	5.0	—	
Gate-Drain Charge		Q_{gd}	—	17	—	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	$(I_S = 3.0\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s})$	V_{SD}	—	—	1.4	Vdc
Forward Turn-On Time		t_{on}	—	**	—	ns
Reverse Recovery Time		t_{rr}	—	400	—	

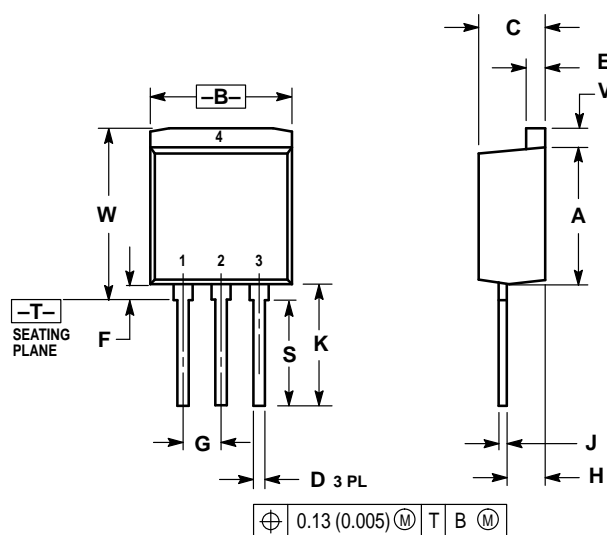
INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_d	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L_s	—	7.5	—	

* Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2.0\%$.

** Limited by circuit inductance.

PACKAGE DIMENSIONS




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.039 REF		1.00 REF	
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.280	0.360	7.11	9.14
S	0.276 REF		7.00 REF	
V	0.045	0.055	1.14	1.40
W	0.423	0.462	10.75	11.75

STYLE 2:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

CASE 418C-01
 ISSUE O

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