Power MOSFET 20 Amps, 30 Volts N-Channel DPAK

This logic level vertical power MOSFET is a general purpose part that provides the "best of design" available today in a low cost power package. Avalanche energy issues make this part an ideal design in. The drain-to-source diode has a ideal fast but soft recovery.

Features

- Ultra-Low RDS(on), single base, advanced technology
- SPICE parameters available
- Diode is characterized for use in bridge circuits
- IDSS and VDS(on) specified at elevated temperatures
- High Avalanche Energy Specified
- ESD JEDAC rated HBM Class 1, MM Class A, CDM Class 0

Typical Applications

- Power Supplies
- Inductive Loads
- PWM Motor Controls
- Replaces MTD20N03L in many applications

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	30	Vdc
Drain-to-Gate Voltage (R _{GS} = 1.0 M Ω)	VDGR	30	Vdc
Gate–to–Source Voltage – Continuous – Non–Repetitive (t _p ≤10 ms)	V _{GS} V _{GS}	±20 ±24	Vdc
Drain Current - Continuous @ $T_A = 25^{\circ}C$ - Continuous @ $T_A = 100^{\circ}C$ - Single Pulse $(t_p \le 10 \ \mu s)$	ID IDM	20 16 60	Adc Apk
Total Power Dissipation @ T _A = 25°C Derate above 25°C Total Power Dissipation @ T _C = 25°C (Note 1.)	P _D	74 0.6 1.75	Watts W/°C W
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T _J = 25°C (V _{DD} = 30 Vdc, V _{GS} = 5 Vdc, L = 1.0 mH, I _{L(pk)} = 24 A, V _{DS} = 34 Vdc)	E _{AS}	288	mJ
Thermal Resistance - Junction-to-Case - Junction-to-Ambient - Junction-to-Ambient (Note 1.)	R _Ө ЈС R _Ө ЈА R _Ө ЈА	1.67 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	°C

^{1.} When surface mounted to an FR4 board using the minimum recommended pad size and repetitive rating; pulse width limited by maximum junction temperature.

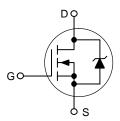


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http://onsemi.com

20 AMPERES 30 VOLTS RDS(on) = 27 m Ω

N-Channel



MARKING DIAGRAM

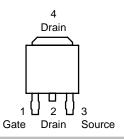


CASE 369A DPAK STYLE 2



20N3L = Device Code = Year WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
NTD20N03L27	DPAK	75 Units/Rail
NTD20N03L27-1	DPAK	75 Units/Rail
NTD20N03L27T4	DPAK	2500 Tape & Reel

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Drain-to-Source Breakdown Voltage (VGS = 0 Vdc, ID = 250 μAdc) Temperature Coefficient (Positive) Zero Gate Voltage Drain Current (VDS = 30 Vdc, VGS = 0 Vdc) (VDS = 30 Vdc, VGS = 0 Vdc, TJ = Gate-Body Leakage Current (VGS = ON CHARACTERISTICS (Note 2.) Gate Threshold Voltage (Note 2.) (VDS = VGS, ID = 250 μAdc) Threshold Temperature Coefficient (Note 2.) Static Drain-to-Source On-Resistant (VGS = 4.0 Vdc, ID = 10 Adc) (VGS = 5.0 Vdc, ID = 10 Adc)	=150°C) ±20 Vdc, V _{DS} = 0 Vdc) Negative) ce (Note 2.)	V(BR)DSS IDSS IGSS VGS(th) RDS(on)	30 - - - - - 1.0	- 43 - - - - 1.6 5.0	- - 10 100 ±100	Vdc mV/°C μAdc nAdc	
(V _G S = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive) Zero Gate Voltage Drain Current (V _D S = 30 Vdc, V _G S = 0 Vdc) (V _D S = 30 Vdc, V _G S = 0 Vdc, T _J = Gate-Body Leakage Current (V _G S = ON CHARACTERISTICS (Note 2.) Gate Threshold Voltage (Note 2.) (V _D S = V _G S, I _D = 250 μAdc) Threshold Temperature Coefficient (Note 2.) Static Drain-to-Source On-Resistant (V _G S = 4.0 Vdc, I _D = 10 Adc)	=150°C) ±20 Vdc, V _{DS} = 0 Vdc) Negative) ce (Note 2.)	IDSS IGSS VGS(th)	- - - -	1.6	10 100 ±100	mV/°C μAdc nAdc	
(V _D S = 30 Vdc, V _G S = 0 Vdc) (V _D S = 30 Vdc, V _G S = 0 Vdc, T _J = Gate-Body Leakage Current (V _G S = ON CHARACTERISTICS (Note 2.) Gate Threshold Voltage (Note 2.) (V _D S = V _G S, I _D = 250 μAdc) Threshold Temperature Coefficient (Note 2.) Static Drain-to-Source On-Resistant (V _G S = 4.0 Vdc, I _D = 10 Adc)	±20 Vdc, V _{DS} = 0 Vdc) Negative) ce (Note 2.)	IGSS VGS(th)	1.0	1.6	100 ±100	nAdc Vdc	
ON CHARACTERISTICS (Note 2.) Gate Threshold Voltage (Note 2.) (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Note 2.) Static Drain-to-Source On-Resistant (V _{GS} = 4.0 Vdc, I _D = 10 Adc)	Negative) ce (Note 2.) ce (Note 2.)	VGS(th)	1.0	1.6	2.0	Vdc	
(V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (N Static Drain-to-Source On-Resistant (V _{GS} = 4.0 Vdc, I _D = 10 Adc)	ce (Note 2.)						
(V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (N Static Drain-to-Source On-Resistant (V _{GS} = 4.0 Vdc, I _D = 10 Adc)	ce (Note 2.)						
$(V_{GS} = 4.0 \text{ Vdc}, I_{D} = 10 \text{ Adc})$	ce (Note 2.)	R _D S(on)	-				
	,		_	28 23	31 27	mΩ	
Static Drain-to-Source On-Resistant (V _{GS} = 5.0 Vdc, I _D = 20 Adc) (V _{GS} = 5.0 Vdc, I _D = 10 Adc, T _J =	V _{DS(on)}	_ _	0.48 0.40	0.54 -	Vdc		
Forward Transconductance (Note 2.)	9FS	_	21	-	mhos		
DYNAMIC CHARACTERISTICS							
Input Capacitance		C _{iss}	_	1005	1260	pF	
Output Capacitance	$(V_{DS} = 25 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}, f = 1.0 \text{ MHz})$	C _{oss}	_	271	420		
Transfer Capacitance	,	C _{rss}	_	87	112		
SWITCHING CHARACTERISTICS (No	ote 3.)						
Turn-On Delay Time		^t d(on)	_	17	25	ns	
Rise Time	$(V_{DD} = 20 \text{ Vdc}, I_{D} = 20 \text{ Adc}, V_{GS} = 5.0 \text{ Vdc},$	t _r	_	137	160		
Turn-Off Delay Time	$R_{G} = 9.1 \Omega$) (Note 2.)	td(off)	_	38	45		
Fall Time		t _f	_	31	40		
Gate Charge	(V _{DS} = 48 Vdc, I _D = 15 Adc, V _{GS} = 10 Vdc) (Note 2.)	QT	_	13.8	18.9	nC	
		Q ₁	_	2.8	-		
		Q ₂	_	6.6	-		
SOURCE-DRAIN DIODE CHARACTE	RISTICS		•	•	•	•	
	S = 20 Adc, V _{GS} = 0 Vdc) (Note 2.) = 20 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	_ _	1.0 0.9	1.15 –	Vdc	
Reverse Recovery Time		t _{rr}	_	23	-	ns	
	(I _S =15 Adc, V _{GS} = 0 Vdc, dl _S /dt = 100 A/μs) (Note 2.)	ta	-	13	_		
		t _b	_	10	_		
Reverse Recovery Stored Charge	<u> </u>	Q _{RR}	-	0.017	-	μC	

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperature.

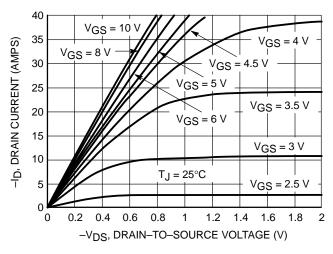


Figure 1. On-Region Characteristics

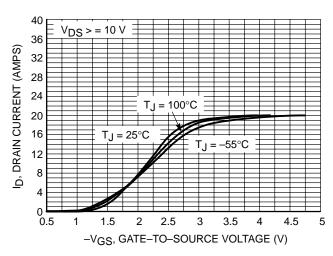


Figure 2. Transfer Characteristics

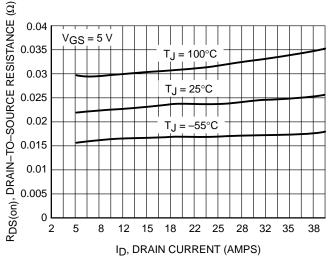


Figure 3. On-Resistance vs. Drain Current and **Temperature**

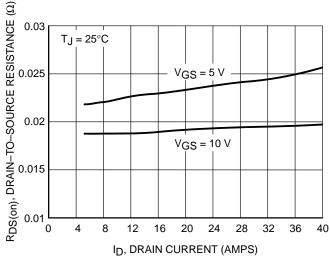


Figure 4. On-Resistance vs. Drain Current and **Gate Voltage**

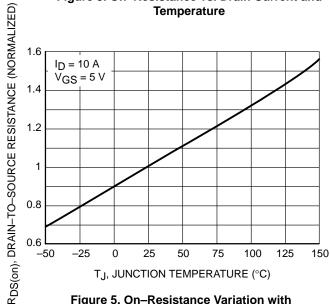


Figure 5. On-Resistance Variation with **Temperature**

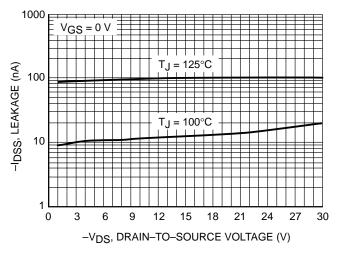


Figure 6. Drain-to-Source Leakage Current vs. Voltage

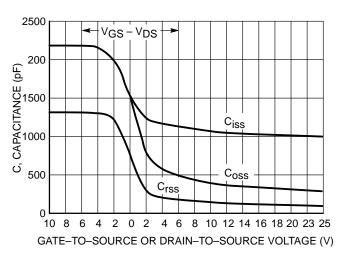


Figure 7. Capacitance Variation

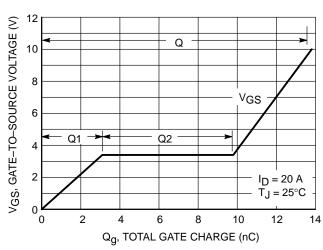


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

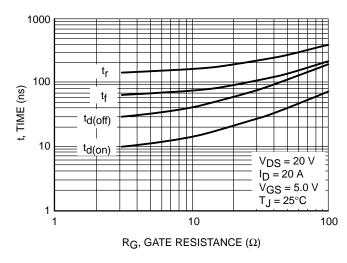


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

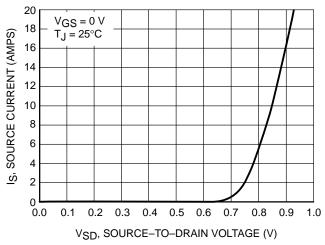


Figure 10. Diode Forward Voltage vs. Current

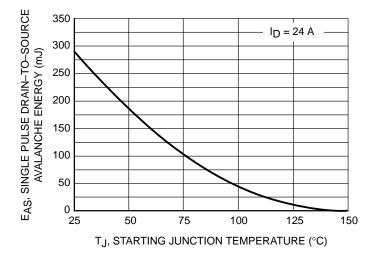
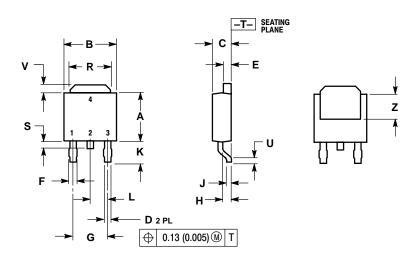


Figure 11. Maximum Avalanche Energy vs. Starting Junction Temperature

PACKAGE DIMENSIONS

DPAK CASE 369A-13 **ISSUE AA**



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.250	5.97	6.35
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
Е	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
Н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020		0.51	
٧	0.030	0.050	0.77	1.27
Z	0.138		3.51	

- STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN





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