



# SPI/I<sup>2</sup>C<sup>R</sup> Compatible, 10-Bit Digital Temperature Sensor and Quad Voltage Output 12/10/8-Bit DAC

## Preliminary Technical Data

## ADT7316/7317/7318

### FEATURES

ADT7316 - Four 12-Bit DACs  
 ADT7317 - Four 10-Bit DACs  
 ADT7318 - Four 8-Bit DACs  
 Buffered Voltage Output  
 Guaranteed Monotonic By Design Over All Codes  
 10-Bit Temperature to Digital Converter  
 Temperature range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
 Temperature Sensor Accuracy of  $\pm 2^{\circ}\text{C}$   
 Supply Range :  $+ 2.7\text{ V}$  to  $+ 5.5\text{ V}$

DAC Output Range:  $0 - V_{\text{REF}}$   
 Power-Down Current  $1\mu\text{A}$   
 Internal  $2.25\text{ V}_{\text{REF}}$  Option  
 Double-Buffered Input Logic  
 Buffered / Unbuffered Reference Input Option  
 Power-on Reset to Zero Volts  
 Simultaneous Update of Outputs (LDAC Function)  
 On-Chip Rail-to-Rail Output Buffer Amplifier

I<sup>2</sup>C, SPI<sup>TM</sup>, QSPI<sup>TM</sup>, MICROWIRE<sup>TM</sup> and DSP-Compatible 5-wire Serial Interface  
 16-Lead TSSOP Package

### APPLICATIONS

Portable Battery Powered Instruments  
 Personal Computers  
 Telecommunications Systems  
 Electronic Test Equipment  
 Domestic Appliances  
 Process Control

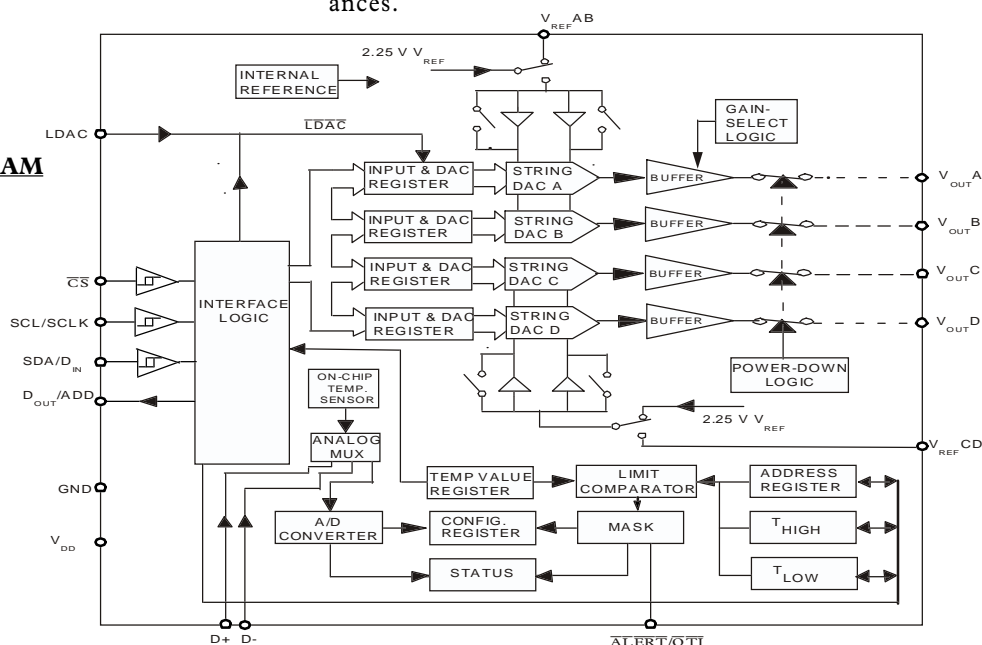
### GENERAL DESCRIPTION

The ADT7316/7317/7318 combines a 10-Bit Temperature-to-Digital Converter and a quad 12/10/8-Bit DAC respectively, in a 16-Lead QSOP package. This includes a bandgap temperature sensor and a 10-bit ADC to monitor and digitize the temperature reading to a resolution of  $0.25^{\circ}\text{C}$ . The ADT7316/17/18 operates from a single  $+2.7\text{ V}$  to  $+ 5.5\text{ V}$  supply. The output voltage of the DAC ranges from  $0\text{ V}$  to  $V_{\text{DD}}$ , with an output voltage settling time of typ  $7\text{ msec}$ . The ADT7316/17/18 provides two serial interface options, a four-wire serial interface which is compatible with SPI<sup>TM</sup>, QSPI<sup>TM</sup>, MICROWIRE<sup>TM</sup> and DSP interface standards; and a two-wire I<sup>2</sup>C interface. It features a standby mode that is controlled via the serial interface.

The reference for the four DACs is derived either internally or from two reference pins (one per DAC pair). The outputs of all DACs may be updated simultaneously using the software LDAC function or external LDAC pin. The ADT7316/7317/7318 incorporates a power-on-reset circuit, which ensures that the DAC output powers-up to zero volts and it remains there until a valid write takes place.

The ADT7316/7317/7318's wide supply voltage range, low supply current and SPI/I<sup>2</sup>C-compatible interface, make it ideal for a variety of applications, including personal computers, office equipment and domestic appliances.

### FUNCTIONAL BLOCK DIAGRAM



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## ADT7316/ADT7317/ADT7318-SPECIFICATIONS

## Preliminary Technical Data

(V<sub>DD</sub>=2.7 V to 5.5 V, GND=0 V, REF<sub>IN</sub>=2.25 V, unless otherwise noted)

Parameter <sup>1</sup>	Min	Typ	Max	Units	Conditions/Comments
<b>DC PERFORMANCE<sup>3,4</sup></b>					
<b>DAC</b>					
<b>ADT7318</b>					
Resolution		8		Bits	
Relative Accuracy		±0.15	±1	LSB	
Differential Nonlinearity		±0.02	±0.25	LSB	Guaranteed Monotonic by design over all codes
<b>ADT7317</b>					
Resolution		10		Bits	
Relative Accuracy		±0.5	±4	LSB	
Differential Nonlinearity		±0.05	±0.5	LSB	Guaranteed Monotonic by design over all codes
<b>ADT7316</b>					
Resolution		12		Bits	
Relative Accuracy		±2	±16	LSB	
Differential Nonlinearity		±0.02	±1	LSB	Guaranteed Monotonic by design over all codes
<b>INTERNAL TEMPERATURE SENSOR</b>					
Accuracy			±2	°C	T <sub>A</sub> = 0°C to +85°C
			±3	°C	T <sub>A</sub> = -40°C to +125°C
Resolution			10	Bits	
<b>EXTERNAL TEMPERATURE SENSOR</b>					
Accuracy			±2	°C	T <sub>A</sub> = 0°C to +85°C
			±3	°C	T <sub>A</sub> = -40°C to +125°C
Resolution			10	Bits	
Update Rate, t <sub>R</sub>		400		μs	
Temperature Conversion Time		25		μs	
Offset Error		±0.4	±3	% of FSR	
Gain Error		±0.15	±1	% of FSR	
Lower Deadband		20	60	mV	Lower Deadband exists only if Offset Error is Negative
Upper Deadband		tbd	tbd	mV	Upper Deadband exists if V <sub>REF</sub> = V <sub>DD</sub>
Offset Error Drift <sup>5</sup>		-12		ppm of FSR/°C	
Gain Error Drift <sup>5</sup>		-5		ppm of FSR/°C	
DC Power Supply Rejection Ratio <sup>5</sup>		-60		dB	ΔV <sub>DD</sub> = ±10%
DC Crosstalk <sup>5</sup>		200		μV	
<b>DAC REFERENCE INPUT<sup>5</sup></b>					
V <sub>REF</sub> Input Range	1		V <sub>DD</sub>	V	Buffered Reference Mode
V <sub>REF</sub> Input Range	0.25		V <sub>DD</sub>	V	Unbuffered Reference Mode
V <sub>REF</sub> Input Impedance	37	45		kΩ	Normal Operation
		>10		MΩ	Buffered reference mode and Power-Down Mode
Reference Feedthrough		-90		dB	Frequency=10KHz
Channel-to-Channel Isolation		-80		dB	Frequency=10KHz
<b>OUTPUT CHARACTERISTICS<sup>5</sup></b>					
Minimum Output Voltage <sup>6</sup>		0.001		V	This is a measure of the minimum and maximum drive V capability of the output amplifier
Maximum Output Voltage <sup>6</sup>		V <sub>DD</sub> -0.001			
DC Output Impedance		0.5		Ω	
Short Circuit Current		25		mA	V <sub>DD</sub> = +5V
		16		mA	V <sub>DD</sub> = +3V
Power Up Time		2.5		μs	Coming out of Power Down Mode. V <sub>DD</sub> = +5 V
		5		μs	Coming out of Power Down Mode. V <sub>DD</sub> = +3 V
<b>DIGITAL INPUTS<sup>5</sup></b>					
Input Current			±1	μA	V <sub>IN</sub> = 0V to V <sub>DD</sub>
V <sub>IL</sub> , Input Low Voltage			0.8	V	V <sub>DD</sub> = +5V±10%
			0.6	V	V <sub>DD</sub> = +3V±10%
V <sub>IH</sub> , Input High Voltage	2			V	
Pin Capacitance		2	10	pF	All Digital Inputs
<b>DIGITAL OUTPUT</b>					
Output High Voltage, V <sub>OH</sub>	2.4			V	I <sub>SOURCE</sub> = I <sub>SINK</sub> = 200 μA
Output Low Voltage, V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 3 mA
Output High Current, I <sub>OH</sub>			1	mA	V <sub>OH</sub> = 5 V
Output Capacitance, C <sub>OUT</sub>			50	pF	
ALERT Output Saturation Voltage			0.8	V	I <sub>OUT</sub> = 4 mA

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Parameter <sup>1</sup>	Min	Typ	Max	Units	Conditions/Comments
<b>I<sup>2</sup>C TIMING CHARACTERISTICS<sup>7,8</sup></b>					
Serial Clock Period, $t_1$	2.5			$\mu$ s	Fast-Mode I <sup>2</sup> C. See Figure 1
Data In Setup Time to SCL High, $t_2$					
Data Out Stable after SCL Low, $t_3$	0			ns	See Figure 1
SDA Low Setup Time to SCL Low (Start Condition), $t_4$	50			ns	See Figure 1
SDA High Hold Time after SCL High (Stop Condition), $t_5$	50			ns	See Figure 1
SDA and SCL Fall Time, $t_6$			90	ns	See Figure 1
<b>SPI TIMING CHARACTERISTICS<sup>9,10</sup></b>					
$\overline{CS}$ to SCLK Setup Time, $t_1$	0			ns	See Figure 2
SCLK High Pulsewidth, $t_2$	50			ns	See Figure 2
SCLK Low Pulse, $t_3$	50			ns	See Figure 2
Data Access Time after SCLK Falling edge, $t_4$ <sup>11</sup>			35	ns	See Figure 2
Data Setup Time Prior to SCLK Rising Edge, $t_5$	20			ns	See Figure 2
Data Hold Time after SCLK Rising Edge, $t_6$	0			ns	See Figure 2
$\overline{CS}$ to SCLK Hold Time, $t_7$	0			ns	See Figure 2
$\overline{CS}$ to DOUT High Impedance			40	ns	See Figure 2
<b>POWER REQUIREMENTS</b>					
$V_{DD}$	2.7		5.5	V	
$I_{DD}$ (Normal Mode) <sup>9</sup>	0.85		1.3	mA	$V_{IH} = V_{DD}$ and $V_{IL} = GND$
$I_{DD}$ (Power Down Mode)	1		3	$\mu$ A	$V_{DD} = +4.5V$ to $+5.5V$ , $V_{IH}=V_{DD}$ and $V_{IL}=GND$
	0.5		1	$\mu$ A	$V_{DD} = +2.7V$ to $+3.6V$ , $V_{IH}=V_{DD}$ and $V_{IL}=GND$
Power Dissipation	tbd	tbd	tbd	$\mu$ W	$V_{DD} = +2.7$ V. Using Normal Mode
	tbd	tbd	tbd	$\mu$ W	$V_{DD} = +2.7$ V. Using Shutdown Mode

Notes:

<sup>1</sup> See Terminology

<sup>2</sup> Temperature ranges are as follows: B Version: -40°C to +125°C.

<sup>3</sup> DC specifications tested with the outputs unloaded.

<sup>4</sup> Linearity is tested using a reduced code range:: ADT7316 (code 115 to 4095); ADT7317 (code 28 to 1023); ADT7318 (code 8 to 255)

<sup>5</sup> Guaranteed by Design and Characterization, not production tested

<sup>6</sup> In order for the amplifier output to reach its minimum voltage, Offset Error must be negative. In order for the amplifier output to reach its maximum voltage,  $V_{REF}=V_{DD}$  and "Offset plus Gain" Error must be positive.

<sup>7</sup> The SDA & SCL timing is measured with the input filters turned on so as to meet the Fast-Mode I<sup>2</sup>C specification. Switching off the input filters improves the transfer rate but has a negative affect on the EMC behaviour of the part.

<sup>8</sup> Guaranteed by design. Not tested in production.

<sup>9</sup> Guaranteed by design and characterization, not production tested.

<sup>10</sup> All input signals are specified with  $t_r = t_f = 5$  ns (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of 1.6 V.

<sup>11</sup> Measured with the load circuit of Figure 3.

<sup>12</sup>  $I_{DD}$  spec. is valid for all DAC codes. Interface inactive. All DACs active. Load currents excluded.

Specifications subject to change without notice.

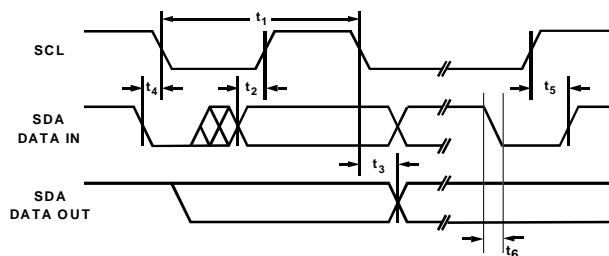


Figure 1. Diagram for I<sup>2</sup>C Bus Timing

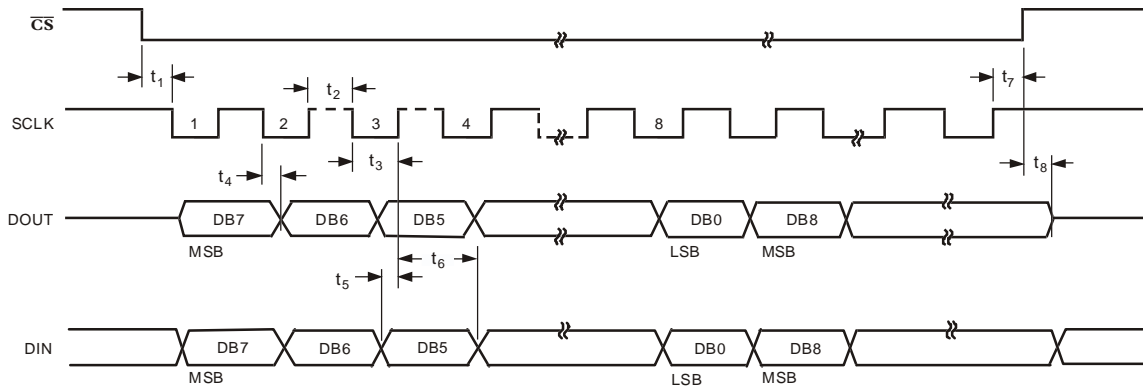


Figure 2. Diagram for SPI Bus Timing

## DAC AC CHARACTERISTICS<sup>1</sup>

( $V_{DD} = +2.7V$  to  $+5.5V$ ;  $R_L = 2k\Omega$  to GND;  $C_L = 200pF$  to GND; All specifications  $T_{MIN}$  to  $T_{MAX}$  unless otherwise noted.)

Parameter <sup>2</sup>	Min	Typ @ 25°C	Max	Units	Conditions/Comments
Output Voltage Settling Time					$V_{REF} = V_{DD} = +5V$
ADT7318		6	8	$\mu s$	1/4 Scale to 3/4 Scale change (40 Hex to C0 Hex)
ADT7317		7	9	$\mu s$	1/4 Scale to 3/4 Scale change (100 Hex to 300 Hex)
ADT7316		8	10	$\mu s$	1/4 Scale to 3/4 Scale change (400 Hex to C00 Hex)
Slew Rate		0.7		V/ $\mu s$	
Major-Code Change Glitch Energy		12		nV-s	1 LSB change around major carry.
Digital Feedthrough		1		nV-s	
Digital Crosstalk		1		nV-s	
Analog Crosstalk		0.5		nV-s	
DAC-to-DAC Crosstalk		3		nV-s	
Multiplying Bandwidth		200		kHz	$V_{REF} = 2V \pm 0.1V_{pp}$
Total Harmonic Distortion		-70		dB	$V_{REF} = 2.5V \pm 0.1V_{pp}$ , Frequency=10kHz.

### NOTES

<sup>1</sup>Guaranteed by Design and Characterization, not production tested

<sup>2</sup>See Terminology

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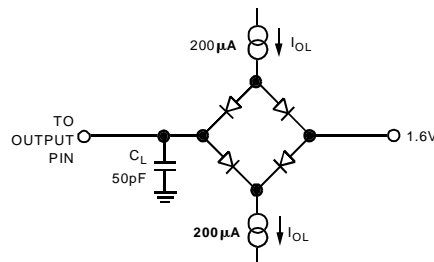


Figure 3. Load Circuit for Access Time and Bus Relinquish Time

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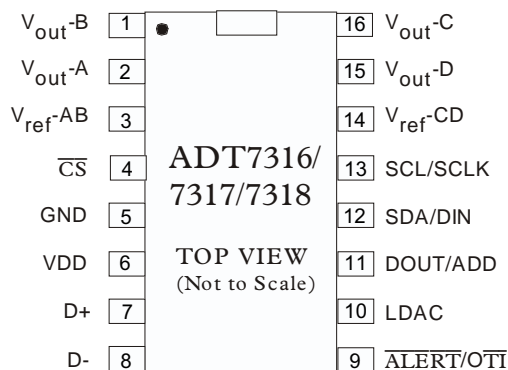
# ADT7316/7317/7318

## ABSOLUTE MAXIMUM RATINGS\*

V <sub>DD</sub> to GND	-0.3 V to +7 V
Analog Input Voltage to GND	-0.3 V to V <sub>DD</sub> + 0.3 V
Digital Input Voltage to GND	-0.3 V to V <sub>DD</sub> + 0.3 V
Digital Output Voltage to GND	-0.3 V to V <sub>DD</sub> + 0.3 V
Reference input voltage to GND	-0.3 V to V <sub>DD</sub> + 0.3V
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
16-Lead TSSOP Package	
Power Dissipation	(T <sub>j</sub> max - T <sub>A</sub> ) / θ <sub>JA</sub>
θ <sub>JA</sub> Thermal Impedance	150 °C/W (QSOP)
Reflow Soldering	
Peak Temperature	+220 +/- 0°C
Time of Peak Temperature	10 sec to 40 sec

\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PIN CONFIGURATION QSOP



## ORDERING GUIDE

Model	Temperature Range	DAC Resolution	Package Description	Package Options
ADT7318ARU	-40°C to +125°C	8-Bits	16-Lead QSOP	RQ-16
ADT7317ARU	-40°C to +125°C	10-Bits	16-Lead QSOP	RQ-16
ADT7316ARU	-40°C to +125°C	12-Bits	16-Lead QSOP	RQ-16

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADT7316/7317/7318 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## ADT7318 PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	V <sub>OUTB</sub>	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
2	V <sub>OUTA</sub>	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
3	V <sub>REFAB</sub>	Reference Input Pin for DACs A and B. It may be configured as a buffered or unbuffered input to each or both of the DACs A and B. It has an input range from 0.25 V to V <sub>DD</sub> in unbuffered mode and from 1 V to V <sub>DD</sub> in buffered mode.
4	$\overline{CS}$	SPI Active low control Input. This is the frame synchronization signal for the input data. When CS goes low, it enables the input register and data is transferred in on the rising edges of the following serial clocks and transferred out on the falling edges.
5	GND	Ground Reference Point for All Circuitry on the part. Analog and Digital Ground.
6	V <sub>DD</sub>	Positive Supply Voltage, +2.65 V to +5.25 V. The supply should be decoupled to ground.
7	D+	Positive connection to external temperature sensor
8	D-	Negative connection to external temperature sensor
9	$\overline{ALERT}/\overline{OTI}$	$\overline{ALERT}$ - SMBus Alert. Open-Drain output. Over temperature indicator, becomes active low when temperature exceeds either internal or external temperature high limits. $\overline{OTI}$ - SPI Temperature Indicator. The output polarity of this pin can be set to give an active low or active high interrupt when temperature high limits are exceeded.
10	LDAC	Active low control input that transfers the contents of the input registers to their respective DAC registers. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows simultaneous update of all DAC outputs. Alternatively this pin can be tied permanently low.
11	DOUT/ADD	SPI Serial Data Output. Logic Output. Data is clocked out of any register at this pin. Data is clocked out at the falling edge of SCLK. ADD, I <sup>2</sup> C serial bus address selection pin. Logic input. During the first valid I <sup>2</sup> C bus communication this pin is checked to determine the serial bus address assigned to the ADT7316/17/18. Any subsequent changes on this pin will have no effect on the I <sup>2</sup> C serial bus address. A low on this pin gives the address 1001 000, leaving it floating gives the address 1001 001 and setting it high gives the address 1001 010.
12	SDA/DIN	SDA - I <sup>2</sup> C Serial Data Input. I <sup>2</sup> C serial data to be loaded into the parts registers is provided on this input. DIN - SPI Serial Data Input. Serial data to be loaded into the parts registers is provided on this input. Data is clocked into a register on the rising edge of SCLK.
13	SCL/SCLK	Serial Clock Input. This is the clock input for the serial port. The serial clock is used to clock data out of any register of the ADT7316/7317/7318 and also to clock data into any register that can be written to.
14	V <sub>REFCD</sub>	Reference Input Pin for DACs C and D. It may be configured as a buffered or unbuffered input to each or both of the DACs C and D. It has an input range from 0.25 V to V <sub>DD</sub> in unbuffered mode and from 1 V to V <sub>DD</sub> in buffered mode.
15	V <sub>OUTD</sub>	Buffered Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
16	V <sub>OUTC</sub>	Buffered Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.

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### TERMINOLOGY

#### RELATIVE ACCURACY

Relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. Typical INL versus Code plots can be seen in TPCs 1, 2, and 3.

#### DIFFERENTIAL NONLINEARITY

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of  $\pm 1$  LSB maximum ensures monotonicity. This DAC and Temperature Sensor ADC is guaranteed monotonic by design. Typical DAC DNL versus Code plots can be seen in TPCs 4, 5, and 6.

#### OFFSET ERROR

This is a measure of the offset error of the DAC and the output amplifier. (See Figures 4 and 5.) It can be negative or positive. It is expressed in mV.

#### GAIN ERROR

This is a measure of the span error of the DAC. It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

#### OFFSET ERROR DRIFT

This is a measure of the change in offset error with changes in temperature. It is expressed in (ppm of full-scale range)/ $^{\circ}\text{C}$ .

#### GAIN ERROR DRIFT

This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/ $^{\circ}\text{C}$ .

#### DC POWER-SUPPLY REJECTION RATIO (PSRR)

This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in  $V_{\text{OUT}}$  to a change in  $V_{\text{DD}}$  for full-scale output of the DAC. It is measured in dBs.  $V_{\text{REF}}$  is held at 2 V and  $V_{\text{DD}}$  is varied  $\pm 10\%$ .

#### DC CROSSTALK

This is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC. It is expressed in  $\mu\text{V}$ .

#### REFERENCE FEEDTHROUGH

This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (i.e.,  $\overline{\text{LDAC}}$  is high). It is expressed in dBs.

#### CHANNEL-TO-CHANNEL ISOLATION

This is the ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of another DAC. It is measured in dBs.

#### MAJOR-CODE TRANSITION GLITCH ENERGY

Major-code transition glitch energy is the energy of the impulse injected into the analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV secs and is measured when the digital code is changed by 1 LSB at the major carry transition (011...11 to 100...00 or 100...00 to 011...11).

#### DIGITAL FEEDTHROUGH

Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device but is measured when the DAC is not being written to the. It is specified in nV secs and is measured with a full-scale change on the digital input pins, i.e., from all 0s to all 1s or vice versa.

#### DIGITAL CROSSTALK

This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV secs.

#### ANALOG CROSSTALK

This is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping  $\overline{\text{LDAC}}$  high. Then pulse  $\overline{\text{LDAC}}$  low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV secs.

#### DAC-TO-DAC CROSSTALK

This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with  $\overline{\text{LDAC}}$  low and monitoring the output of another DAC. The energy of the glitch is expressed in nV secs.

#### MULTIPLYING BANDWIDTH

The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

#### TOTAL HARMONIC DISTORTION

This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. It is measured in dBs.

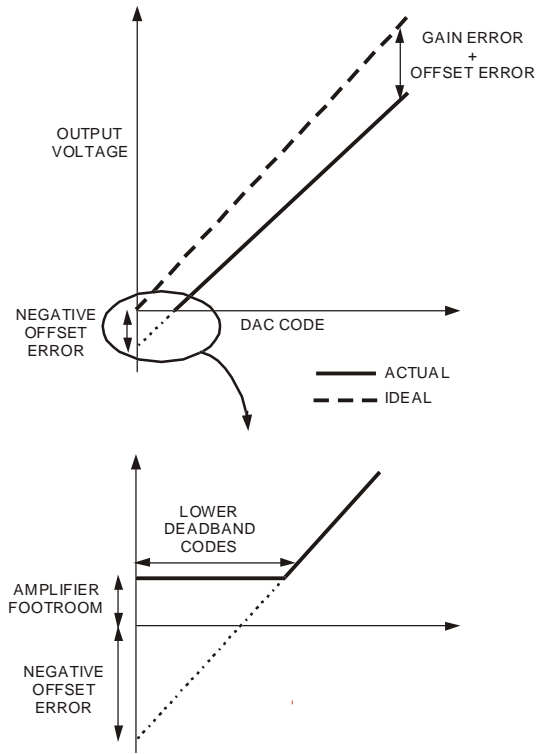


Figure 4. Transfer Function with Negative Offset

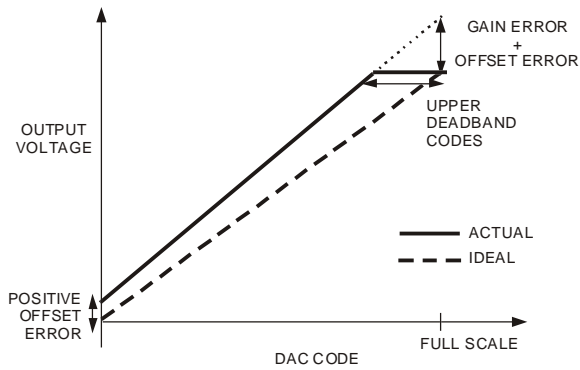
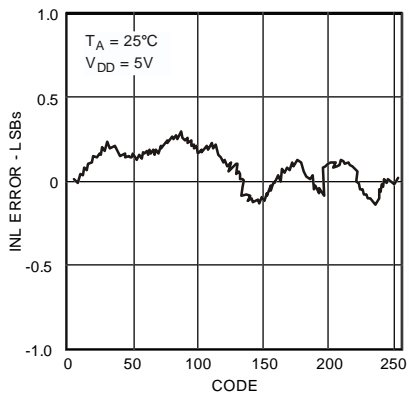


Figure 5. Transfer Function with Positive Offset ( $V_{REF} = V_{DD}$ )

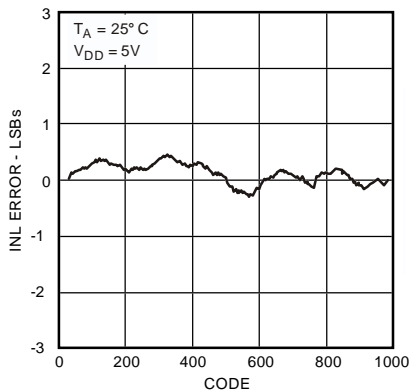


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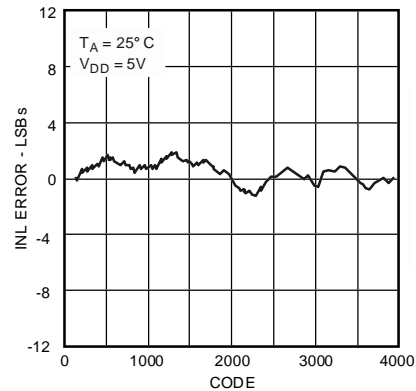
ADT7316/7317/7318



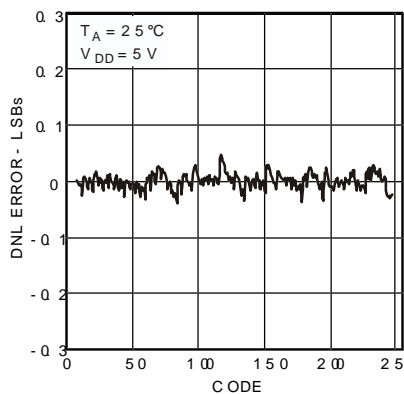
TPC 1. ADT7318 Typical INL Plot



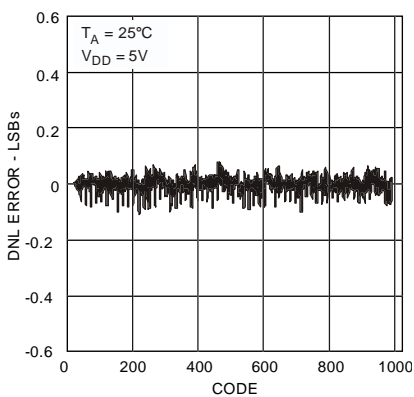
TPC 2. ADT7317 Typical INL Plot



TPC 3. ADT7316 Typical INL Plot

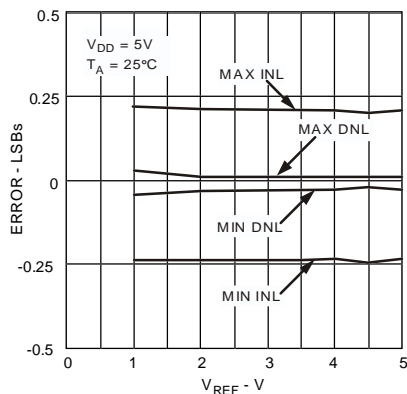


TPC 4. ADT7318 Typical DNL Plot

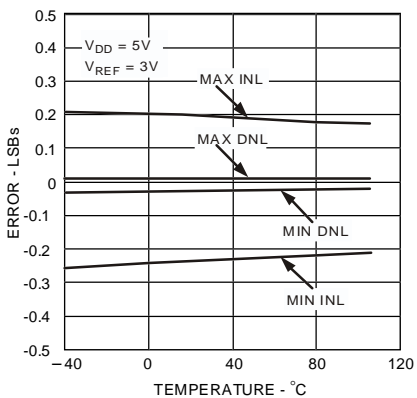


TPC 5. ADT7317 Typical DNL Plot

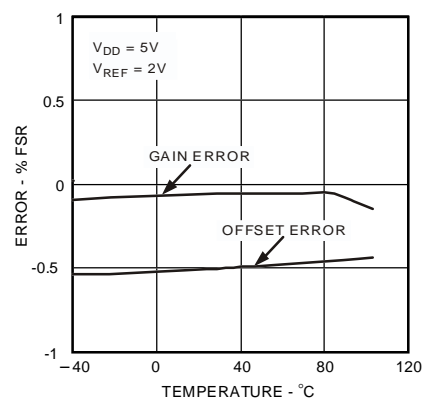
TPC 6. ADT7316 Typical DNL Plot



TPC 7. ADT7318 INL and DNL Error vs  $V_{REF}$



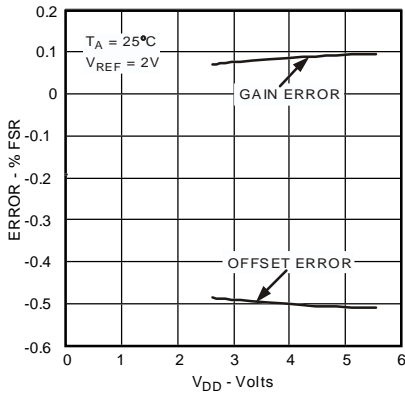
TPC 8. ADT7318 INL Error and DNL Error vs Temperature



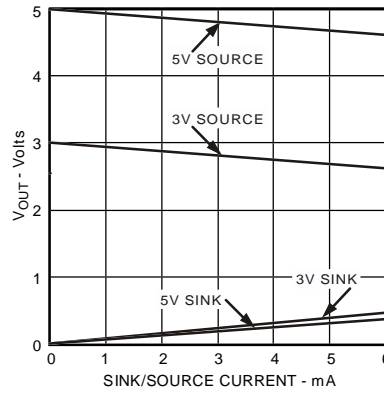
TPC 9. ADT7318 Offset Error and Gain Error vs Temperature

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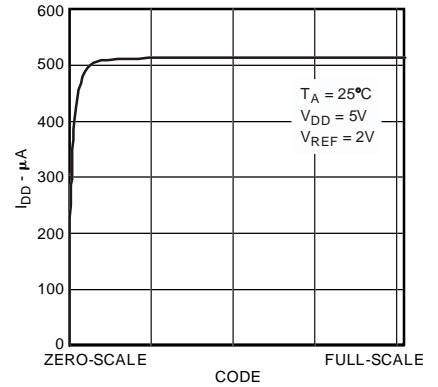
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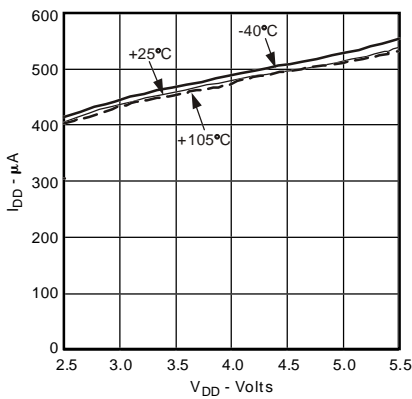
TPC 10. Offset Error and Gain Error vs V<sub>DD</sub>



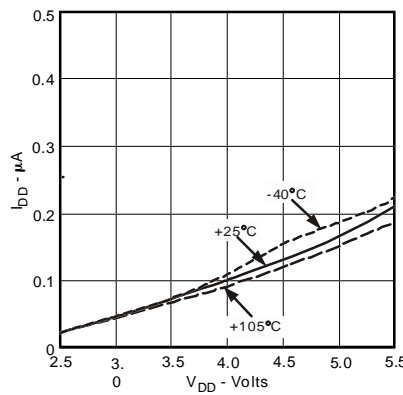
TPC 11. V<sub>OUT</sub> Source and Sink Current Capability



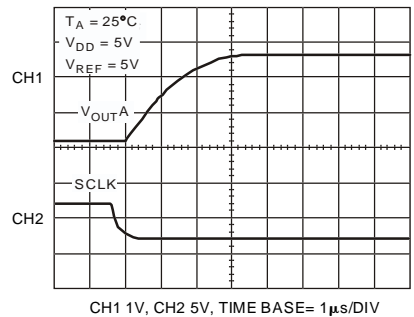
TPC 12. Supply Current vs. DAC Code



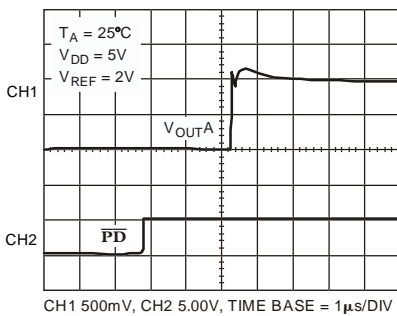
TPC 13. Supply Current vs. Supply Voltage



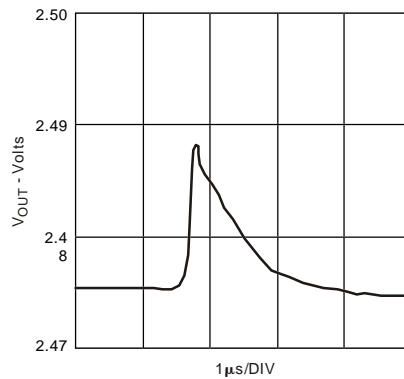
TPC 14. Power-Down Current vs. Supply Voltage



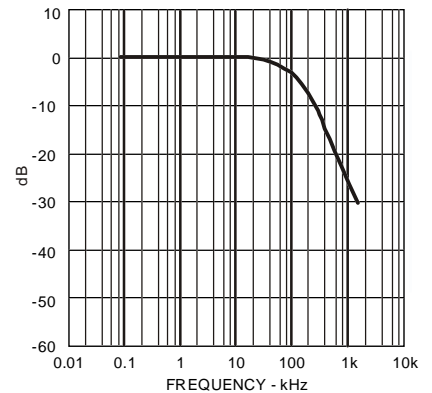
TPC 15. Half-Scale Settling (1/4 to 3/4 Scale Code Change)



TPC 16. Exiting Power-Down to Midscale



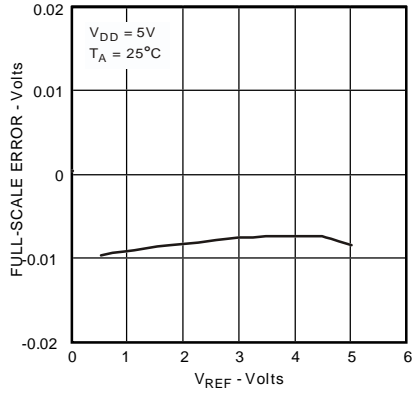
TPC 17. ADT7316 Major-Code Transition Glitch Energy



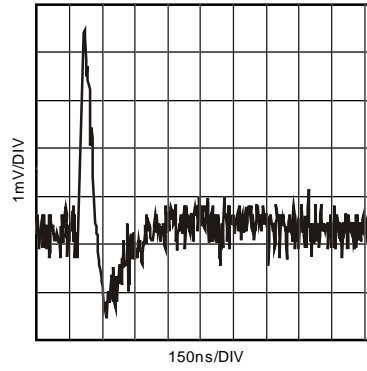
TPC 18. Multiplying Bandwidth (Small-Signal Frequency Response)

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TPC 19. Full-Scale Error vs.  $V_{REF}$



TPC 20. DAC-to-DAC Crosstalk

# ADT7316/7317/7318

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## FUNCTIONAL DESCRIPTION - DAC

The ADT7316/7317/7318 has quad resistor-string DACs fabricated on a CMOS process with a resolutions of 12, 10 and 8 bits respectively. They contain four output buffer amplifiers and is written to via I<sup>2</sup>C serial interface or SPI serial interface. Selection between the two types of interface is done on the first valid serial communication. If the first valid serial communication to the part is I<sup>2</sup>C then the internal interface circuit will be locked to I<sup>2</sup>C communication. The same holds for SPI interfacing.

The ADT7316/7317/7318 operates from a single supply of 2.5 V to 5.5 V and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7V/μs.

DACs A and B share a common reference input, namely V<sub>REFAB</sub>. DACs C and D share a common reference input, namely V<sub>REFCD</sub>. Each reference input may be buffered to draw virtually no current from the reference source, or unbuffered to give a reference input range from GND to V<sub>DD</sub>. The devices have a power-down mode, in which all DACs may be turned off completely with a high-impedance output.

### Digital-to-Analog Section

The architecture of one DAC channel consists of a resistor-string DAC followed by an output buffer amplifier. The voltage at the V<sub>REF</sub> pin provides the reference voltage for the corresponding DAC. Figure 4 shows a block diagram of the DAC architecture. Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{OUT} = \frac{V_{REF} * D}{2^N}$$

where D=decimal equivalent of the binary code which is loaded to the DAC register;

0-255 for ADT7318 (8-Bits)

0-1023 for ADT7317 (10-Bits)

0-4095 for ADT7316 (12-Bits)

N = DAC resolution.

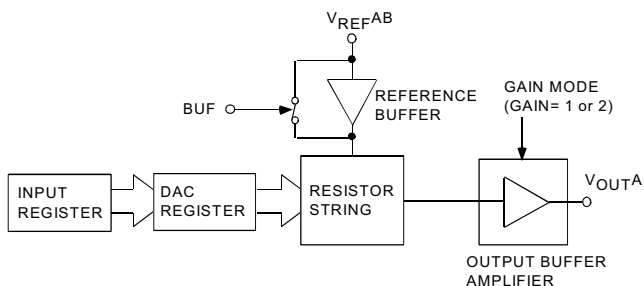


Figure 4. Single DAC channel architecture

### Resistor String

The resistor string section is shown in Figure 5. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at what node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

## DAC Reference Inputs

There is a reference pin for each pair of DACs. The reference inputs are buffered but can also be individually configured as unbuffered. The advantage with the buffered input is the high impedance it presents to the voltage source driving it. However if the unbuffered mode is used, the user can have a reference voltage as low as 0.25 V and as high as V<sub>DD</sub> since there is no restriction due to headroom and footroom of the reference amplifier.

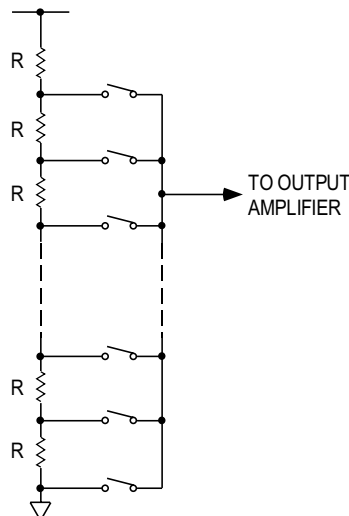


Figure 5. Resistor String

If there is a buffered reference in the circuit, there is no need to use the on-chip buffers. In unbuffered mode the input impedance is still large at typically 90 kΩ per reference input for 0-V<sub>REF</sub> mode and 45 kΩ for 0-2V<sub>REF</sub> mode.

The buffered/unbuffered option is controlled by the configuration register (see data register descriptions).

There is also an option to use the internal temperature reference. This option is controlled by the configuration register.

### Output Amplifier

The output buffer amplifier is capable of generating output voltages to within 1mV of either rail. Its actual range depends on the value of V<sub>REF</sub>, GAIN and offset error. If a gain of 1 is selected (GAIN=0) the output range is 0.001 V to V<sub>REF</sub>.

If a gain of 2 is selected (GAIN=1) the output range is 0.001 V to 2V<sub>REF</sub>. However because of clamping the maximum output is limited to V<sub>DD</sub> - 0.001V.

The output amplifier is capable of driving a load of 2kΩ to GND or V<sub>DD</sub>, in parallel with 500pF to GND or V<sub>DD</sub>. The source and sink capabilities of the output amplifier can be seen in the plot in TPC tbd.

The slew rate is 0.7V/μs with a half-scale settling time to +/-0.5 LSB (at 8 bits) of 6μs.

## FUNCTIONAL DESCRIPTION - Temperature Sensor

The ADT7316/7317/7318 contains a two-channel A to D converter with special input signal conditioning to enable operation with external and on-chip diode temperature sensors. When the ADT7316/7317/7318 is operating nor-

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mally, the A to D converter operates in a free-running mode. The analog input multiplexer alternately selects either the on-chip temperature sensor to measure its internal temperature, or a external temperature sensor. These signals are digitized by the ADC and the results stored in the Internal and External Temperature Value Registers.

The measured results are compared with the Internal and External, High, Low and the temperature limits are stored in on-chip registers. Out of limit comparisons generate flags that are stored in the Status Register and one or more out-of limit results will cause the ALERT/OTI output to pull low.

Theoretically, the temperature sensor and ADC can measure temperatures from  $-128^{\circ}\text{C}$  to  $+127^{\circ}\text{C}$  with a resolution of  $0.25^{\circ}\text{C}$ . However, temperatures below  $T_{\text{MIN}}$  and above  $T_{\text{MAX}}$  are outside the operating temperature range of the device, so internal temperature measurements outside this range are not possible. Temperature measurement from  $-128^{\circ}\text{C}$  to  $+127^{\circ}\text{C}$  is possible using an external sensor.

Temperature measurement is initiated by a couple of methods. The first method uses an internal clock count-down of 20ms and then a conversion is performed. The internal oscillator is the only circuit that's powered up between conversions and once it times out, every 20ms, a wake-up signal is sent to power-up the rest of the circuitry. A monostable is activated at the beginning of the wake-up signal to ensure that sufficient time is given to the power-up process. The monostable typically takes  $4\ \mu\text{s}$  to time out. It then takes typically  $25\ \mu\text{s}$  for each conversion to be completed. The temperature is measured 16 times and internally averaged to reduce noise. The new temperature value is loaded into the Temperature Value Register and ready for reading by the I<sup>2</sup>C or SPI interface. The user has the option of disabling the averaging by setting a bit in one of the configuration registers. The ADT7316/7317/7318 defaults on power-up with the averaging enabled.

A temperature measurement is also initiated every time the oneshot method is used. This method requires the user to write to the Oneshot register when a temperature measurement is needed. Writing to the Oneshot register will start a temperature conversion directly after the write operation. The track/hold goes into hold approximately  $4\ \mu\text{s}$  (monostable time-out) and a conversion is then initiated. Typically  $25\ \mu\text{s}$  later the conversion is complete. As with the previous method, the temperature is measured 16 times and internally averaged to reduce noise. The Temperature Value Register is then loaded with a new temperature value. If averaging is disabled for the automatic method then it subsequently applies to the Oneshot method also.

### MEASUREMENT METHOD

#### INTERNAL TEMPERATURE MEASUREMENT

The ADT7316/7317/7318 contains an on-chip bandgap temperature sensor, whose output is digitized by the on-chip ADC. The temperature data is stored in the Internal Temperature Value Register. As both positive and negative temperatures can be measured, the temperature data is

stored in two's complement format, as shown in Table 1. The thermal characteristics of the measurement sensor could change and therefore an offset is added to the measured value to enable the transfer function to match the thermal characteristics. This offset is added before the temperature data is stored. The offset value used is stored in the Internal Temperature Offset Register.

#### EXTERNAL TEMPERATURE MEASUREMENT

The ADT7316/7317/7318 can measure the temperature of one external diode sensor or diode-connected transistor.

The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about  $-2\text{mV}/^{\circ}\text{C}$ . Unfortunately, the absolute value of  $V_{\text{be}}$ , varies from device to device, and individual calibration is required to null this out, so the technique is unsuitable for mass-production.

The technique used in the ADT7316/7317/7318 is to measure the change in  $V_{\text{be}}$  when the device is operated at two different currents.

This is given by:

$$\Delta V_{\text{be}} = KT/q \times \ln(N)$$

where:

K is Boltzmann's constant

q is charge on the carrier

T is absolute temperature in Kelvins

N is ratio of the two currents

Figure 6 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors, but it could equally well be a discrete transistor.

If a discrete transistor is used, the collector will not be grounded, and should be linked to the base. If a PNP transistor is used the base is connected to the D- input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D- input and the base to the D+ input.

We recommend that a 2N3906 be used as the external transistor.

To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D- input. As the sensor is operating in a noisy environment, C1 is provided as a noise filter. See the section on layout considerations for more information on C1.

To measure  $\Delta V_{\text{be}}$ , the sensor is switched between operating currents of I and N x I. The resulting waveform is passed through a lowpass filter to remove noise, thence to a chopper-stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a DC voltage proportional to  $\Delta V_{\text{be}}$ . This voltage is measured by the ADC to give a temperature output in 8-bit two's complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

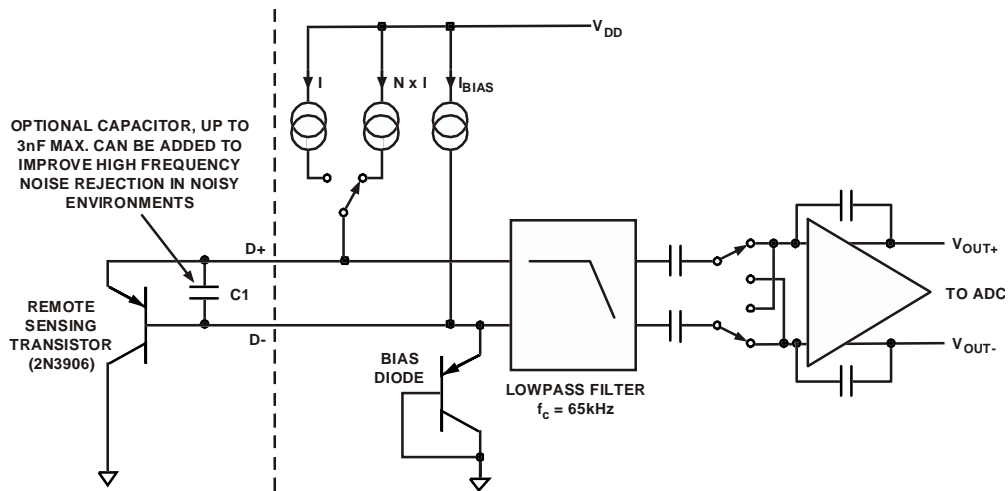


Figure 6. Signal Conditioning for External Diode temperature Sensors

**TEMPERATURE VALUE FORMAT**

One LSB of the ADC corresponds to 0.25°C. The ADC can theoretically measure a temperature span of 255 °C. The internal temperature sensor has a practical low value limit of -40 °C due to device maximum ratings. It is possible to measure the full temperature span using the external temperature sensor. The temperature data format is shown in Tables 1.

The result of the internal or external temperature measurements is stored in the temperature value registers, and is compared with limits programmed into the Internal or External High and Low Registers.

**TABLE 1. Temperature Data Format (Internal and External Temperature)**

Temperature	Digital Output
-40 °C	11 0110 0000
-25 °C	11 1001 1100
-10 °C	11 1101 1000
-0.25 °C	11 1111 1111
0 °C	00 0000 0000
+0.25 °C	00 0000 0001
+10 °C	00 0010 1000
+25 °C	00 0110 0100
+50 °C	00 1100 1000
+75 °C	01 0010 1100
+100 °C	01 1001 0000
+105 °C	01 1010 0100

Temperature Conversion Formula:

1. Positive Temperature = ADC Code/4
2. Negative Temperature = (ADC Code\* - 512)/4

\*DB9 is removed from the ADC Code

**ADT7316/7317/7318 REGISTERS**

The ADT7316/17/18 contains registers that are used to store the results of external and internal temperature measurements, high and low temperature limits, set output DAC voltage levels, configure and control the device. A description of these registers follows, and further details are given in Tables 2 to 11.

**Table 2. List of ADT7813 Registers**

RD/WR Address	Name	Power-on Default
3Eh	Manufacturer's ID	41h
3Fh	Die Revision Register	00h
7Eh	Test 1 Register	00h
7Fh	Test 2 Register	00h
00h	One Shot Register	00h
01h	Configuration Register 1	00h
02h	Configuration Register 2	00h
03h	DAC ( $\overline{LDAC}$ ) Mask Register	00h
04h	Mask Register	00h
05h	Internal Temperature Offset Register	00h
06h	External Temperature Offset Register	00h

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07h	Internal Temp. High	28h
08h	Internal Temp. Low	00h
09h	External Temp. High	28h
0Ah	External Temp. Low	00h
0Bh	DAC A High Register	00h
0Ch	DAC A Low Register (ADT7316/17 only)	00h
0Dh	DAC B High Register	00h
0Eh	DAC B Low Register (ADT7316/17 only)	00h
0Fh	DAC C High Register	00h
10h	DAC C Low Register (ADT7316/17 only)	00h
11h	DAC D High Register	00h
12h	DAC D Low Register (ADT7316/17 only)	00h
13h	Interrupt Status Register	00h
14h	Int. Temp. Value Register (8 MSBs)	00h
15h	Int. Temp. Value Register (2 LSBs)	00h
16h	Ext. Temp. Value Register (8 MSBs)	00h
17h	Ext. Temp. Value Register (2 LSB)	00h

**MANUFACTURER'S ID REGISTER (8-BITS)**

This register contains the company identification number for this chip.

**DIE REVISION REGISTER**

This register is divided into the four lsbs representing the Stepping and the four msbs representing the Version. The Stepping contains the manufacturers code for minor revisions or steppings to the device. The Version is the ADT7316/17/18 version number. Since the ADT7316/17/18 is the first part in this family, it's version number is 0000b.

**TEST 1 AND TEST 2 REGISTERS**

These registers are used by the manufacturer for testing purposes. Writing to these registers during normal operation may lead to erroneous events

**ONE-SHOT REGISTER**

The One-Shot Register is a write only register. It is used to initiate a single temperature conversion and comparison cycle when the ADT7316/17/18 is in standby mode, after which the device returns to standby. This is not a data register as such and it is the write operation that causes the one-shot conversion. The data written to this address is irrelevant and is not stored.

**INTERRUPT STATUS REGISTER**

This 8-bit read only register reflects the status of any of the interrupts that can cause the  $\overline{\text{ALERT}}/\overline{\text{TI}}$  pin to go active.

Table IV. Status Register (Write)

Bit	Name	Function
7	IHigh	1 when Int. High Temp. is exceeded
6	ILow	1 when Int. Low Temp. is exceeded
5	EHigh	1 when Ext. High Temp. is exceeded
4	ELow	1 when Ext. Low Temp is exceeded
3	Open	1 when Ext Sensor is open circuit

**CONFIGURATION REGISTER 1**

This Configuration Register is an 8-bit read/write register that is used to set the operating modes of the ADT7316/17/18. The 5 MSBs are used to set the operating modes, see Table 7. D0, D1 and D2 are used for factory settings and must have zeros written to them during normal operation.

Table VI. Configuration Register 1

D7	D6	D5	D4	D3	D2	D1	D0
TI	PD	REF	$\overline{\text{LDAC}}$	$\overline{\text{LDAC}}$	N/A	N/A	N/A
0*	0*	0*	0*	0*	0*	0*	0*

\*Default settings at Power-up.

Table VII. Configuration Register 1 Settings

Bit	Function
D7 TI	0 = Temperature Indicator $\overline{\text{ALERT}}/\overline{\text{TI}}$ Enable 1 = Temperature Indicator $\overline{\text{ALERT}}/\overline{\text{TI}}$ Disable
D6 PD	This bit is used to power down the DAC and temperature sensor circuits. In powerdown mode the serial interface is still active and the user is capable of communicating with any register. 1 = Powerdown mode , 0 = Power-up mode
D5 REF	1 = External, 0 = Internal

D4	D3	Function
0	0	LSB write to the DAC register generates $\overline{\text{LDAC}}$ which updates the single addressed DAC only.
0	1	LSB write to the DAC register generates $\overline{\text{LDAC}}$ which updates the 2 DACs (in pairs of DACs A&B or DACs C&D due to buffer limitations).
1	0	LSB write to the DAC register generates $\overline{\text{LDAC}}$ which updates all four DACs simultaneously.
1	1	$\overline{\text{LDAC}}$ generated from LDAC Register (4 Bits, 1 per DAC)

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## CONFIGURATION REGISTER 2

This Configuration Register is an 8-bit read/write register that is used to set the operating modes of the ADT7316/17/18. The 4 MSBs are used to set the operating modes, see Table XX. D0, D1, D2 and D3 are used for factory settings and must have zeros written to them during normal operation.

**Table xx. Configuration Register 2**

D7	D6	D5	D4	D3	D2	D1	D0
G	Buf_AB	Buf_CD	Pol	AR	AI	N/A	N/A
0*	0*	0*	0*	0*	0*	0*	0*

\* Default settings at Power-up

**Table xx. Configuration Register 2 Settings**

Bit		Function
D7	Gain	This bit changes the output range of all four DACs. 0 = Output range of 0 V to $V_{ref}$ 1 = Output range of 0 V to $2V_{ref}$
D6	Buf_AB	This bit controls whether the internal or external reference to DACs A and B is buffered or unbuffered. 0 = Unbuffered Int/Ext $V_{ref}$ 1 = Buffered Int/Ext $V_{ref}$
D5	Buf_CD	This bit controls whether the internal or external reference to DACs C and D is buffered or unbuffered. 0 = Unbuffered Int/Ext $V_{ref}$ 1 = Buffered Int/Ext $V_{ref}$
D4	Polarity	This bit controls the output polarity of pin 1 (ALERT/TI). 0 = Active low ALERT/TI 1 = Active high ALERT/TI
D3	Alert Reset	Reset the $\overline{\text{ALERT/TI}}$ pin if set to 1. The next temperature conversion will have the ability to activate the ALERT/TI function. The bit status is not stored, thus this bit will be "0" if read.
D2	Auto	Setting this bit to a 1 enables the Address Pointer to be auto-incremented when reading from or writing to the registers in Table xx. 0 = Auto-Increment disabled 1 = Auto-Increment enabled

**DAC ( $\overline{\text{LDAC}}$ ) MASK REGISTER**  
USE ????????

## MASK REGISTER (R/W)

This register can be used to mask out any of the interrupts that can cause  $\overline{\text{ALERT/TI}}$  to go active and can also mask out the capability of the  $\overline{\text{LDAC}}$  signal to update the

DACs. Bit 4 is reserved and writing to this bit will have no affect.

**Table X. Interrupt Mask Register**

D7	D6	D5	D4	D3	D2	D1	D0
IH*	EH*	Open*	0*				$\overline{\text{LDAC}}^*$

\* Default setting is 0.

Setting D5 to D7 to a 1 will mask out the interrupts represented by these bits. IH represents the interrupt caused by Internal  $T_{HIGH}$  register. EH represents the interrupt caused by External  $T_{HIGH}$  register. Open represents the interrupt caused by an open circuit on D+ and D-.

**Table VII.  $\overline{\text{LDAC}}$  Register**

Bits	Function
D3	Enables/disables $\overline{\text{LDAC}}$ to update DAC A
D2	Enables/disables $\overline{\text{LDAC}}$ to update DAC B
D1	Enables/disables $\overline{\text{LDAC}}$ to update DAC C
D0	Enables/disables $\overline{\text{LDAC}}$ to update DAC D

Setting D0 to D3 to a 1 disables the  $\overline{\text{LDAC}}$ . Example by setting the register to a value of 1010 (0Ah), this disables the  $\overline{\text{LDAC}}$  in updating DACs A and C.

## INTERNAL TEMPERATURE VALUE REGISTER (8 MSBS)

This Internal Temperature Value Register is a 8-bit read-only register which stores the temperature reading from the internal temperature sensor in twos complement format. This 8 MSBs of the internal temperature reading is stored in this register.

**Table xx. Internal Temperature Value Register (First Read)**

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2

## INTERNAL TEMPERATURE VALUE REGISTER (2 LSBS)

This Internal Temperature Value Register is a 8-bit read-only register which stores the temperature reading from the internal temperature sensor in twos complement format. The 2 LSBs of the internal temperature reading is stored in this register.

**Table xx. Internal Temperature Value Register (Second Read)**

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	0	0	0	0	0	0



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### EXTERNAL TEMPERATURE VALUE REGISTER (8 MSBS)

This External Temperature Value Register is a 8-bit read-only register which stores the temperature reading from the external temperature sensor in twos complement format. The 8 MSBs of the external temperature reading is stored in this register.

**Table xx. External Temperature Value Register (First Read)**

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2

### EXTERNAL TEMPERATURE VALUE REGISTER (2 LSBS)

This External Temperature Value Register is a 8-bit read-only register which stores the temperature reading from the external temperature sensor in twos complement format. The 2 LSBs of the external temperature reading is stored in this register.

**Table xx. External Temperature Value Register (Second Read)**

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	0	0	0	0	0	0

### INTERNAL T<sub>HIGH</sub> REGISTER

The Internal T<sub>HIGH</sub> Register is an 8-bit read/write register which stores the upper limit that will activate the ALERT/TI output. Therefore if the value in the Temperature Value Register is greater than the value in the T<sub>HIGH</sub> Register, then the ALERT/TI pin is activated (that is if ALERT/TI is enabled in the Configuration Register). As it is an 8-bit register the temperature resolution is 1°C.

**Table VIII. Internal T<sub>HIGH</sub> Register**

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B6	B5	B4	B3	B2	B1	B0

### INTERNAL T<sub>LOW</sub> REGISTER

The Internal T<sub>LOW</sub> Register is an 8-bit read/write register which stores the lower limit that will deactivate the ALERT/TI output. Therefore if the value in the Temperature Value Register is less than the value in the T<sub>LOW</sub> Register, the ALERT/TI pin is deactivated (that is if ALERT/TI is enabled in the Configuration Register). As it is an 8-bit register the temperature resolution is 1°C.

**Table X. Internal T<sub>LOW</sub> Register**

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B6	B5	B4	B3	B2	B1	B0

### EXTERNAL T<sub>HIGH</sub> REGISTER

The External T<sub>HIGH</sub> Register is an 8-bit read/write register which stores the upper limit that will activate the ALERT/TI output. Therefore if the value in the Temperature Value Register is greater than the value in the T<sub>HIGH</sub> Register, then the ALERT/TI pin is activated (that is if ALERT/TI is enabled in the Configuration Register). As it is an 8-bit register the temperature resolution is 1°C.

**Table X. External T<sub>LOW</sub> Register**

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B6	B5	B4	B3	B2	B1	B0

### EXTERNAL T<sub>LOW</sub> REGISTER

The External T<sub>LOW</sub> Register is an 8-bit read/write register which stores the lower limit that will deactivate the ALERT/TI output. Therefore if the value in the Temperature Value Register is less than the value in the T<sub>LOW</sub> Register, the ALERT/TI pin is deactivated (that is if ALERT/TI is enabled in the Configuration Register). As it is an 8-bit register the temperature resolution is 1°C.

**Table X. External T<sub>LOW</sub> Register**

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B6	B5	B4	B3	B2	B1	B0

### DAC A HIGH REGISTER

This 8-bit read/write register contains the digital data for DAC A to convert to an analog representation. As the ADT7318 has only an 8-bit DAC this register is all that is need for it's DAC A. But in the case of the ADT7316 (12-Bit) and ADT7317 (10-Bit) this register contains the 8 MSBs of the DAC A word.

**Table xx. DAC A High Register**

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B6	B5	B4	B3	B2	B1	B0

### DAC A LOW REGISTER (ADT7316/17 ONLY)

This 8-bit read/write register conatins the LSBs of the DAC A word. In the case of the ADT7317 the 2 LSBs are stored here and for the ADT7316 the 4 LSBs are stored here.

**Table xx. ADT7317 DAC A Low Register**

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	0	0	0	0	0	0

**Table xx. ADT7316 DAC A Low Register**

D7	D6	D5	D4	D3	D2	D1	D0
B3	B2	B1	LSB	0	0	0	0

# ADT7316/7317/7318

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## DAC B HIGH REGISTER

This 8-bit read/write register contains the digital data for DAC B to convert to an analog representation. As the ADT7318 has only an 8-bit DAC this register is all that is need for it's DAC B. But in the case of the ADT7316 (12-Bit) and ADT7317 (10-Bit) this register contains the 8 MSBs of the DAC B word.

Table xx. DAC B High Register

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B6	B5	B4	B3	B2	B1	B0

## DAC B LOW REGISTER (ADT7316/17 ONLY)

This 8-bit read/write register conatins the LSBs of the DAC B word. In the case of the ADT7317 the 2 LSBs are stored here and for the ADT7316 the 4 LSBs are stored here.

Table xx. ADT7317 DAC B Low Register

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	0	0	0	0	0	0

Table xx. ADT7316 DAC B Low Register

D7	D6	D5	D4	D3	D2	D1	D0
B3	B2	B1	LSB	0	0	0	0

## DAC C HIGH REGISTER

This 8-bit read/write register contains the digital data for DAC C to convert to an analog representation. As the ADT7318 has only an 8-bit DAC this register is all that is need for it's DAC C. But in the case of the ADT7316 (12-Bit) and ADT7317 (10-Bit) this register contains the 8 MSBs of the DAC C word.

Table xx. DAC C High Register

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B6	B5	B4	B3	B2	B1	B0

## DAC C LOW REGISTER (ADT7316/17 ONLY)

This 8-bit read/write register conatins the LSBs of the DAC C word. In the case of the ADT7317 the 2 LSBs are stored here and for the ADT7316 the 4 LSBs are stored here.

Table xx. ADT7317 DAC C Low Register

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	0	0	0	0	0	0

Table xx. ADT7316 DAC C Low Register

D7	D6	D5	D4	D3	D2	D1	D0
B3	B2	B1	LSB	0	0	0	0

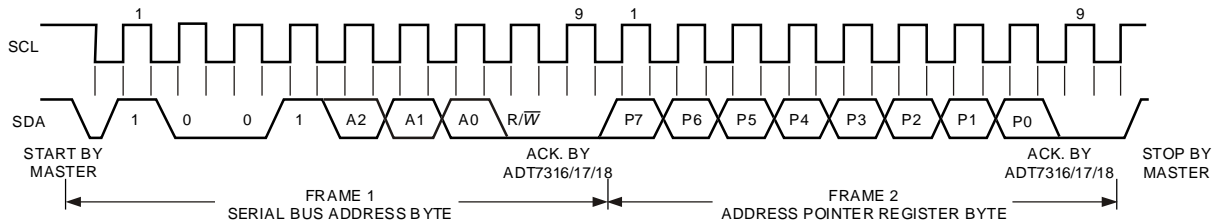


Figure xx. I<sup>2</sup>C - Writing to the Address Pointer Register to select a register for a subsequent Read operation

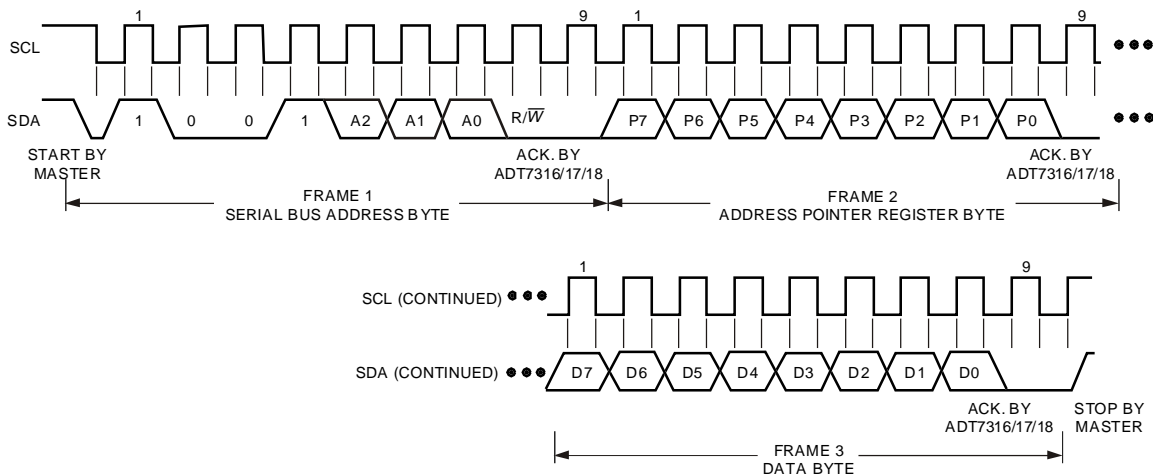


Figure xx. I<sup>2</sup>C - Writing to the Address Pointer Register followed by a single byte of data to the selected register

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## DAC D HIGH REGISTER

This 8-bit read/write register contains the digital data for DAC D to convert to an analog representation. As the ADT7318 has only an 8-bit DAC this register is all that is needed for its DAC D. But in the case of the ADT7316 (12-Bit) and ADT7317 (10-Bit) this register contains the 8 MSBs of the DAC D word.

Table xx. DAC D High Register

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B6	B5	B4	B3	B2	B1	B0

## DAC D LOW REGISTER (ADT7316/17 ONLY)

This 8-bit read/write register contains the LSBs of the DAC D word. In the case of the ADT7317 the 2 LSBs are stored here and for the ADT7316 the 4 LSBs are stored here.

Table xx. ADT7317 DAC D Low Register

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	0	0	0	0	0	0

Table xx. ADT7316 DAC D Low Register

D7	D6	D5	D4	D3	D2	D1	D0
B3	B2	B1	LSB	0	0	0	0

## ADT7316/7317/7318 SERIAL INTERFACE

There are two serial interfaces that can be used on this part, I<sup>2</sup>C and SPI. The first valid serial communication protocol selects the type of interface. The following sections describe in detail how to use these interfaces.

### I<sup>2</sup>C SERIAL INTERFACE

Like all I<sup>2</sup>C-compatible devices, the ADT7316/7317/7318 has a 7-bit serial address. The four MSBs of this address for the ADT7316/7317/7318 are set to 1001. The three LSBs are set by pin 11, ADD. The ADD pin can be configured three ways to give three different address options; low, floating and high. Setting the ADD pin low gives a serial bus address of 1001 000, leaving it floating gives the address 1001 001 and setting it high gives the address 1001 010.

The serial bus protocol operates as follows:

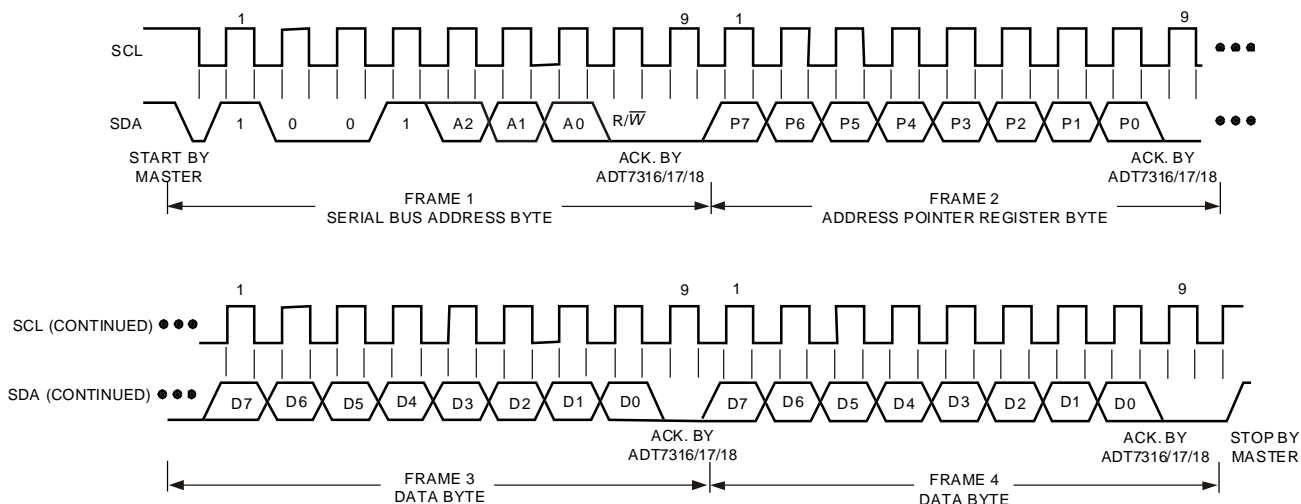


Figure xx. I<sup>2</sup>C - Writing to the Address Pointer followed by two data bytes to two Registers with Auto-Increment enabled

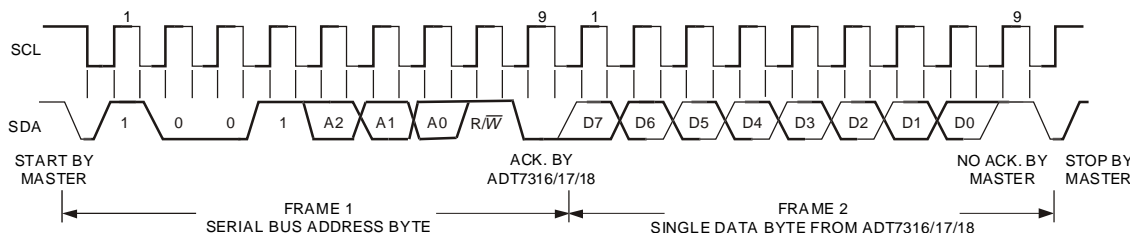


Figure xx. I<sup>2</sup>C - Reading a single byte of data from a selected register

# ADT7316/7317/7318

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1. The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SDA whilst the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next 8 bits, consisting of a 7-bit address (MSB first) plus a R/W bit, which determines the direction of the data transfer, i.e. whether data will be written to or read from the slave device.

The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle whilst the selected device waits for data to be read from or written to it. If the R/W bit is a 0 then the master will write to the slave device. If the R/W bit is a 1 the master will read from the slave device.

2. Data is sent over the serial bus in sequences of 9 clock pulses, 8 bits of data followed by an Acknowledge Bit from the receiver of data. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a STOP signal.

3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will pull the data line high during the low period before the 9th clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation, because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

## WRITING TO THE ADT7316/7317/7318

Depending on the register being written to, there are three different writes for the ADT7316/7317/7318.

### Writing to the Address Pointer Register for a subsequent read.

In order to read data from a particular register, the Address Pointer Register must contain the address of that register. If it does not, the correct address must be written to the Address Pointer Register by performing a single-byte write operation, as shown in Figure x. The write operation consists of the serial bus address followed by the address pointer byte. No data is written to any of the data registers. A read operation is then performed to read the register.

### Writing a single byte of data to a Register.

All registers are 8-bit registers so only one byte of data can be written to each register. Writing a single byte of data to one of these Read/Write registers consists of the serial bus address, the data register address written to the Address Pointer Register, followed by the data byte written to the selected data register. This is illustrated in Figure x.

### Writing multiple bytes of data to Registers in sequence

In order to write multiple bytes of data in one write operation the AI bit in Configuration 2 Register must be set to 1. This particular write operation allows data to be written to registers with sequential addresses without having to load the Address Pointer Register each time a register is being written to. The write operation consists of the serial bus address, the address of the first register to be written to, followed by the data bytes for each register, as shown in Figure xx. After each register has been loaded with its data byte, the Address Pointer register increments until all input data bytes have been loaded or until it reaches the last read/write register in Table xx, DAC D Low Register. The Address Pointer Register will not loop around to the top of the Register Table.

## READING DATA FROM THE ADT7316/7317/7318

Reading data from the ADT7316/7317/7318 can be done in at least a one byte operation and up to a maximum of a

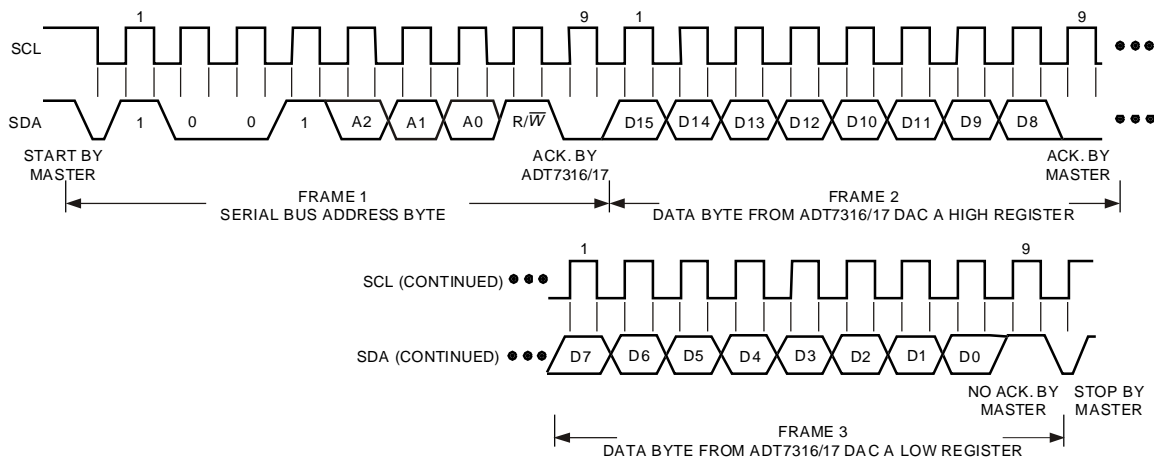


Figure xx. I<sup>2</sup>C - Reading Temperature Value from DAC A High Register and DAC A Low Register

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xx byte operation. Reading back the contents of the one register is a single byte read operation as shown in Figure x. The register address previously having been set up by a single byte write operation to the Address Pointer Register. If the AI bit in Configuration 2 Register is set to 0 and once the register address has been set up, any number of reads can be subsequently done from that register without having to write to the Address Pointer Register again. If you want to read from another register then you will have to write to the Address Pointer Register again to set up the relevant register address.

If the AI bit is set to 1 then it is possible to read data from a number of registers whose addresses are in sequence. A two byte read operation is shown in Figure x. The same rules apply for a two byte read as a single byte read except that the Address Pointer Register is incremented after each register is read.

### SMBUS ALERT

The ADT7316/7317/7318 ALERT output is an SMBus interrupt line for devices that want to trade their ability to master for an extra pin. The ADT7316/7317/7318 is a slave only device and uses the SMBUS ALERT to signal the host device that it wants to talk. The SMBUS ALERT on the ADT7316/7317/7318 is used as an over temperature indicator.

The ALERT pin has an open-drain configuration which allows the ALERT outputs of several I<sup>2</sup>C devices to be wired-AND together when the ALERT pin is active low. Use D4 of the Configuration 2 Register to set the active polarity of the ALERT output. The power-up default is active low. The ALERT function can be disabled or enabled by setting D7 of Configuration 1 Register to a 1 or 0 respectively.

The host device can process the ALERT interrupt and simultaneously access all SMBUS ALERT devices through the alert response address. Only the device which pulled the ALERT low will acknowledge the ARA (Alert Response Address). If more than one device pulls the ALERT pin low, the highest priority (lowest address) device will win communication rights via standard I<sup>2</sup>C arbitration during the slave address transfer.

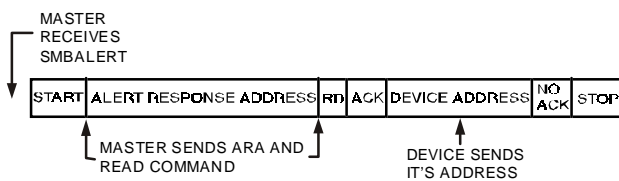


Figure xx. Use of SMBALERT

1. SMBALERT pulled low
2. Master initiates a read operation and sends the Alert Response Address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose ALERT output is low responds to the Alert Response Address and the master reads its device address.

4. Once the ADT7316/17/18 responds to the ARA, it will reset its ALERT output, provided that the error condition that caused the ALERT no longer exists. If the SMBALERT line remains low, the master will resend the ARA again and so on until all devices whose ALERT outputs were low have responded.

The ALERT output becomes active when the value in the Temperature Value Register exceeds the value in the T<sub>HIGH</sub> Register. It is reset when a write operation to the Configuration 2 Register sets D3 to a 1 or when the temperature falls below the value stored in the T<sub>LOW</sub> Register.

The ALERT output requires an external pull-up resistor. This can be connected to a voltage different from V<sub>DD</sub> provided the maximum voltage rating of the ALERT output pin is not exceeded. The value of the pull-up resistor depends on the application, but should be as large as possible to avoid excessive sink currents at the ALERT output, which can heat the chip and affect the temperature reading.

### SPI SERIAL INTERFACE

The SPI serial interface of the ADT7316/7317/7318 consists of four wires, CS, SCLK, DIN and DOUT. The CS is used to select the device when more than one device is connected to the serial clock and data lines. The SCLK is used to clock data in and out of the part. The DIN line is used to write to the registers and the DOUT line is used to read data back from the registers.

The part operates in a slave mode and requires an externally applied serial clock to the SCLK input. The serial interface is designed to allow the part to be interfaced to systems that provide a serial clock that is synchronized to the serial data.

There are two types of serial operations, a read and a write. Command words are used to distinguish between a read and a write operation. These command words are given in Table xx.

Table xx. SPI COMMAND WORDS

WRITE	READ
90h (1001 0000)	91h (1001 0001)
92h (1001 0010)	93h (1001 0011)
94h (1001 0100)	95h (1001 0101)

### Write Operation

Figure xx. shows the timing diagram for a write operation to the ADT7316/7317/7318. Data is clocked into the registers on the rising edge of SCLK. When the CS line is high the DIN and DOUT lines are in three-state mode. Only when the CS goes from a high to a low does the part accept any data on the DIN line. If the Address Pointer Register has its auto-increment enabled then from Figure xx. the register address gives the first register that will be written to. Subsequent data bytes will be written into sequential writable registers. Thus after each data byte has been written into a register, the Address Pointer Register auto increments its value to the next available register. If the auto-increment is disabled and more than one data byte has been sent to the part in the write operation then

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the part will ignore all data bytes after the first one. To overwrite the contents of a register another write operation will have to be performed.

**Read Operation**

Figures xx to xx show the timing diagrams necessary to accomplish correct read operations. To read back from a register you first have to write to the Address Pointer Register with the address of the register you wish to read from. This operation is shown in Figure xx. Figure xx shows the procedure for reading back a single byte of data. The read command is first sent to the part during the first 8 clock cycles, during the following 8 clock cycles the data contained in the register selected by the Address Pointer register is outputted onto the DOUT line. Data is outputted onto the DOUT line on the rising edge of SCLK. Figure xx. shows the procedure when reading data from two sequential registers. Multiple data reads is only possible if the auto-increment for the Address Pointer Register has been enabled. If the auto-increment is disabled then the second data byte in Figure xx. will contain the same as the first data byte because it would have come from the same register.

**$\overline{OTI}$  Interrupt**

The  $\overline{OTI}$  pin can be used to signal an over temperature event. If the temperature in either the Internal or External Temperature Value Registers exceeds the  $T_{HIGH}$  (Internal or External) Registers then the  $\overline{OTI}$  line goes active. Of course nothing happens if the  $\overline{OTI}$  Interrupt is disabled, D7 of Configuration Register 1. The  $\overline{OTI}$  interrupt will be cleared when the temperature goes below the value in the  $T_{LOW}$  (Internal or External) registers, depending on whether the internal or external temperature sensor caused the interrupt. The  $\overline{OTI}$  interrupt can also be cleared by setting D3 of Configuration Register 2.

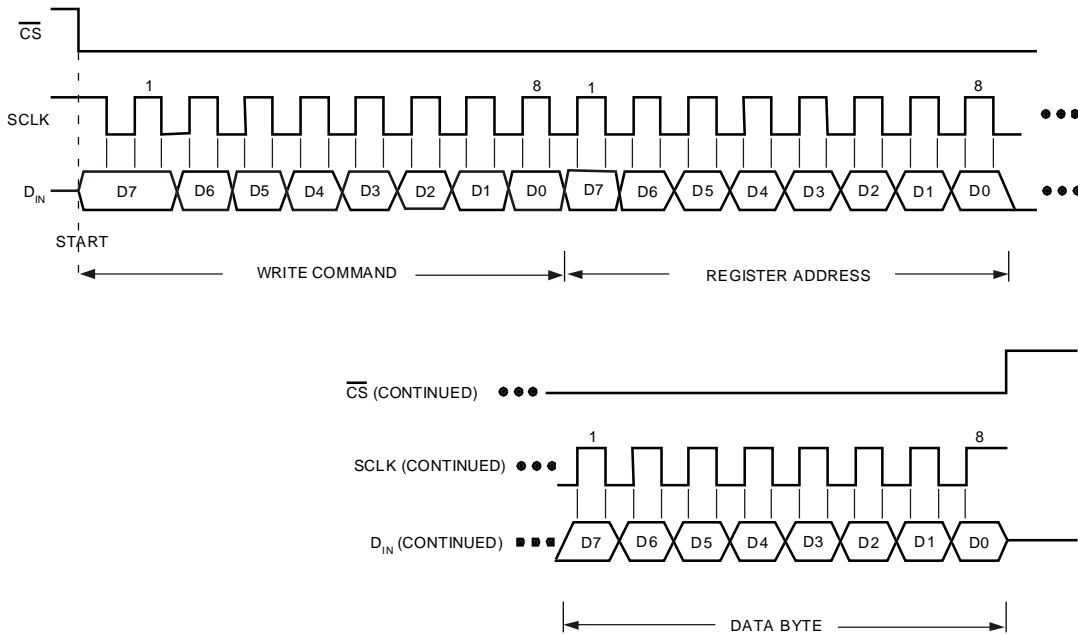


Figure xx. SPI - Writing to the Address Pointer Register followed by a single byte of data to the selected register

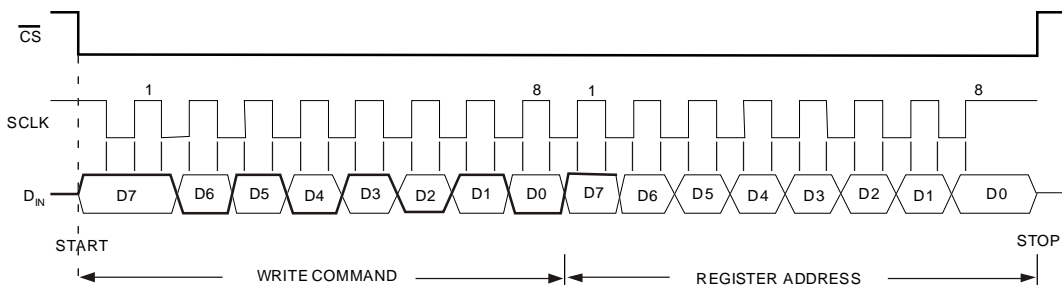


Figure xx. SPI - Writing to the Address Pointer Register to select a register for a subsequent read operation

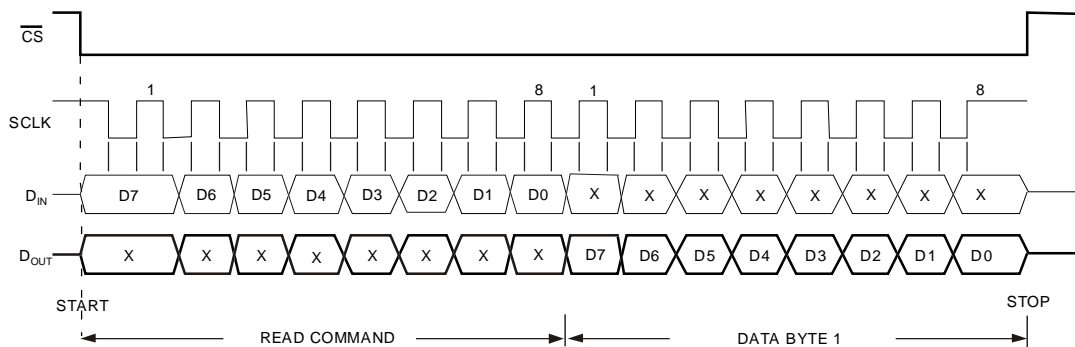


Figure xx. SPI - Reading a single byte of data from a selected register

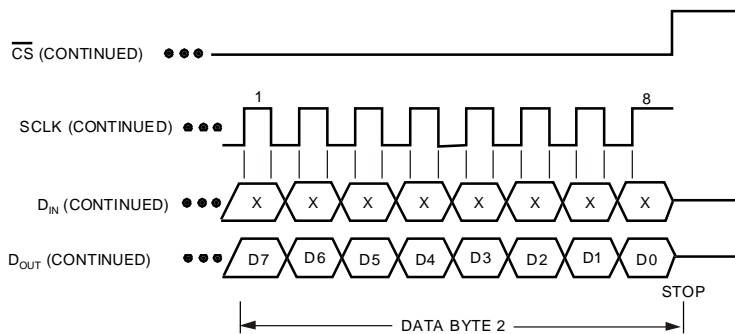
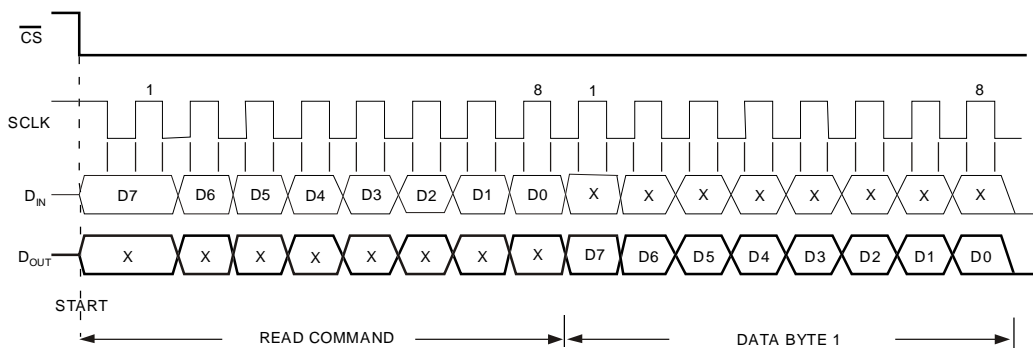


Figure xx. SPI - Reading a two bytes byte of data from a two sequential registers

**Outline Dimensions**  
 (Dimensions shown in inches and mm )  
**16-Lead QSOP Package**  
**(RQ-16)**

