TOSHIBA

PRELIMINARY

TMPR3922U 32-bit MIPS® RISC Microprocessor

Description

The TMPR3922U 32-bit MIPS® RISC processor is a single-chip integrated digital Application Specific Standard Product (ASSP) for use with such devices as Hand-held PCs (HPC), PalmPCs, TV Set-Top Boxes (STB), DVD players, Webphones, Auto PC devices, and Windows®-based terminals (WBT).

The TMPR3922U is an enhanced version of the TMPR3912U 32-bit MIPS RISC microprocessor. The TMPR3922U integrates a high-performance, low power TX39 family processor core with necessary support logic and added peripheral support modules to present a complete personal digital assistant (PDA) solution.

The TMPR3922U supports the Microsoft® Windows CE v2.0 operating system, as well as, external color display capability with a liquid crystal display (LCD) controller.

Microprocessor Features

- Built-in TLCS3920 Processor Core
  - Developed based on the MIPS RISC R3000A architecture
  - Instruction cache 16kB and Data cache 8kB
  - Five-stage pipeline: Fetch, Decode, Execute, Memory access, and Register write
  - Incorporates single-cycle DSP function Multiply-Accumulate (MAC) for functions such as soft modem, high-performance data and fax protocols
  - Integrated Translation Lookaside Buffer (TLB) which maps 4k/16k/64k/128k/256k/1M/4M Byte page
- Maximum Operating Frequency: 133MHz
- Power Supply: 3.3V (I/O)/ 2.5V (internal operation)
- CPU clock stop mode
- Power-down modes for individual peripherals
- Standby current: 10µA (typical)
- Package: 208-pin plastic LQFP

On-Chip Peripheral Features

- Integrated Power Management Unit
- Multiple DMA channels
- Clock generator
  - Built-in 16x frequency phase locked loop (PLL)
- Write buffer
  - Four channel support
- Interrupt and I/O Modules
- Timer Module
- Bus Interface Unit (BIU)
  - Memory controllers for DRAM (EDO), SDRAM, SRAM, ROM, Flash memory, and PCMCIA
- System Interface Unit (SIU)
  - Multiple-channel 32-bit DMA controller
  - Independent channel for SIB to/from codecs, serial port, IrDA, and general purpose Universal Asynchronous Receiver/Transmitter (UART)
- Concentration Highway Interface (CHI) Module
  - Interfacing support to external full-duplex time-division-multiplexed (TDM) communication peripherals
  - Supports ISDN line and other serial PCM/TDM serial devices
- IR Module
  - Supports IR consumer, IrDA, and IR FSK communication modes, and carrier detect
- Serial Interconnect Bus (SIB) Module
- Serial Peripheral Interface (SPI) Module
- UART Module
  - Two full-duplex UARTs

Development Tool Support

A wide range of development tools for the TX39 family are available from Toshiba and third-party partners including support software, reference kits, and all the necessary technical support and training needed for design applications.

Language Tools

- Compilers
  - Green Hills Software
  - Cygnus
  - Microsoft Visual C++ 5.0
  - Microsoft Windows CE Toolkit for Visual C++ 5.0

Operating Systems

- Microsoft Windows CE
- µITRON

Reference Platform

- A complete development system and reference kit for Windows CE v2.0 applications is available from Toshiba

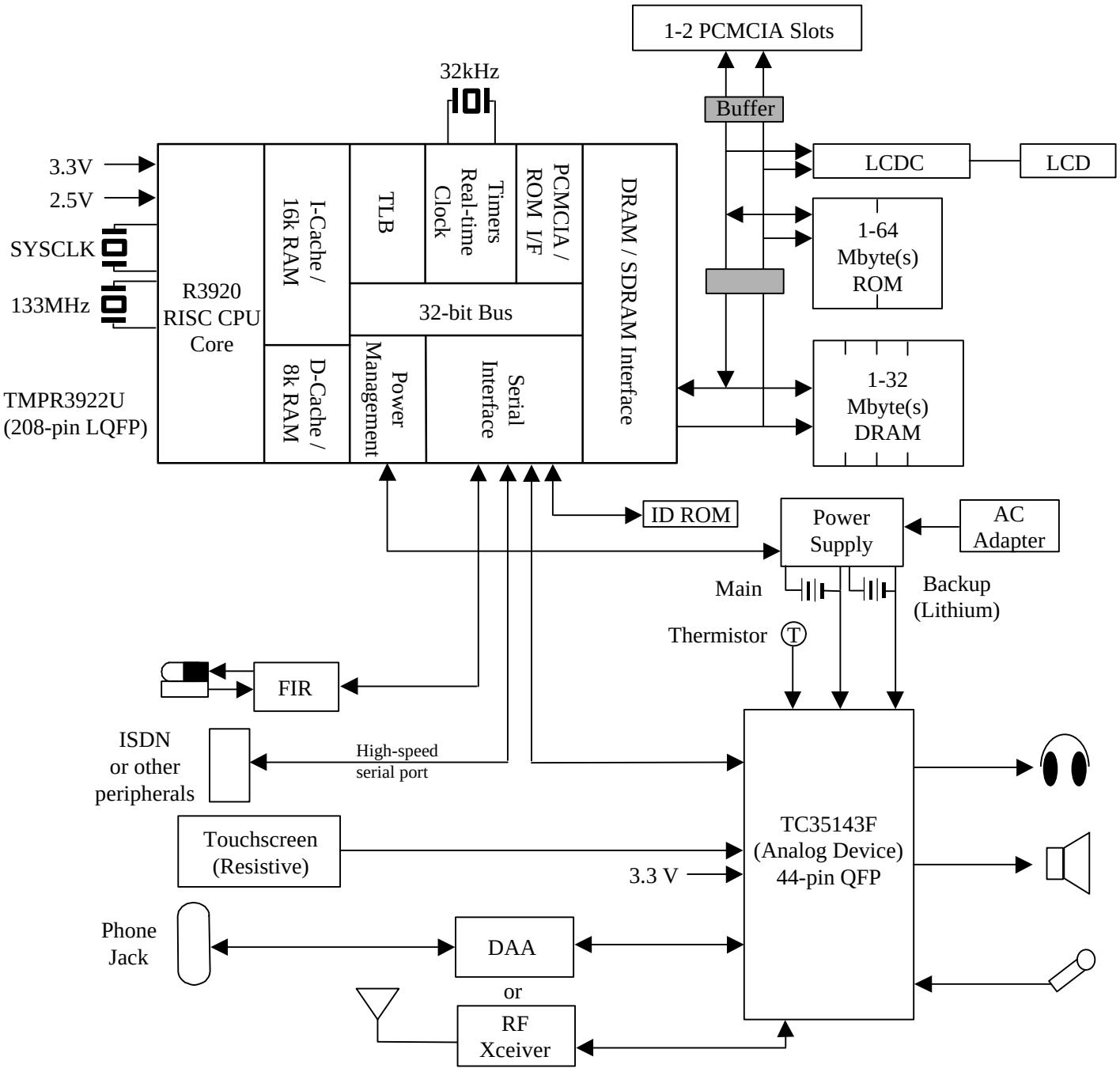

Figure 1. TMPR3922U System Block Diagram

Electric Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DDH},	TBD	V
	V_{DDL}, V_{DDLS}	TBD	V
Input voltage	V_{IN}	V_{SS} –0.5 to V_{DDH} +0.5	V
Storage temperature	T_{STG}	–55 to 125	°C
Maximum dissipation (T_A = 70°C)	P_D	1	W

NOTE: Using at specifications higher than the maximum ratings can cause permanent damage. For normal operation, use under the recommended operating conditions. Exceeding the recommended operating conditions may affect the reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply voltage	V_{DDH}		3.0	3.3	3.6	V
	V_{DDL}, V_{DDLS}		2.3	2.5	2.7	V
Operating temperature	T_{OPR}		0	–	70	°C

DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating current	I_{DD}	V_{IN} = V_{DDH} or V_{SS}, V_{DDH} = MAX, V_{DDL}=V_{DDLS} = MAX, I_{OH}=I_{OL}= 0 mA, fin(6)= 10MHz	–	TBD		MA
Static current	I_{DDS}	V_{IN} = V_{DDH} or V_{SS}, V_{DDH} = 3.3V, V_{DDL} = 2.5V, V_{DDLS} = 0V, I_{OH} = I_{OL}= 0 mA, SLEEP mode & RTC stop mode	–	TBD		mA
	I_{DDS}	V_{IN} = V_{DDH} or V_{SS}, V_{DDH} = 3.3V, V_{DDL} = 2.5V, V_{DDLS} = 0V, V_{DDLS} = I_{OL}= 0 mA, SLEEP & RTC Running mode	–	TBD		mA
Input Leakage current	I_{IN}	V_{IN} = V_{DDH} or V_{SS}		TBD		mA
Input voltage (1)	V_{IH1}	V_{DDH} = 3.6V		TBD		V
	V_{IL1}	V_{DDH} = 3.0V		TBD		V
Input voltage (2)	V_{IH2}	V_{DDH} = 3.6V		TBD		V
	V_{IL2}	V_{DDH} = 3.0V		TBD		V
Output voltage (3)	V_{OH1}	V_{DDH} = 3.0V, I_{OH} = -4mA		TBD		V
	V_{OL1}	V_{DDH} = 3.0V, I_{OL} = -4mA		TBD		V
Output voltage (4)	V_{OH2}	V_{DDH} = 3.0V, I_{OH} = -8mA		TBD		V
	V_{OL2}	V_{DDH} = 3.0V, I_{OL} = -8mA		TBD		V
Output voltage (5)	V_{OH3}	V_{DDH} = 3.0V, I_{OH} = -16mA		TBD		V
	V_{OL3}	V_{DDH} = 3.0V, I_{OL} = -16mA		TBD		V
Input current (Pull-down resistor)	I_{IHP}	V_{DDH} = MAX VIN = V_{DDH}		TBD		µA

(1) SYSCLKIN, **(2)** Other inputs, **(3)** D[31;0], RAS0*, RAS1*, DCS0*, DCKE*, DQMH, DQML, DREQ*, DGRNT*, BC32K, VDAT[3:0], CP, LOAD, DF, FRAME, DISPON, VIDDONE, PWRCS, TXD, RXD, CS3-O*, CHIFS, CHICLK, CHIDOUT, CHIDIN, IO[6;0], SPICLK, SPIOUT, SPIIN, SIBSYNC, SIBDOUT, SIBMCLK, SIBCLK, RXPWR, IROUT, CARD1WAIT*, CARD2WAIT*, MIOX[2:0], **(4)** A[12:0], ALE, RD*, WE*, CAS3-O*, CARDREG*, CARDIOWR*, CARD1CSL*, CARD1CSH*, CARD2CSL*, CARD2CSH*, **(5)** DCLKOUT, **(6)** MBUSCLK, MBUSDATA

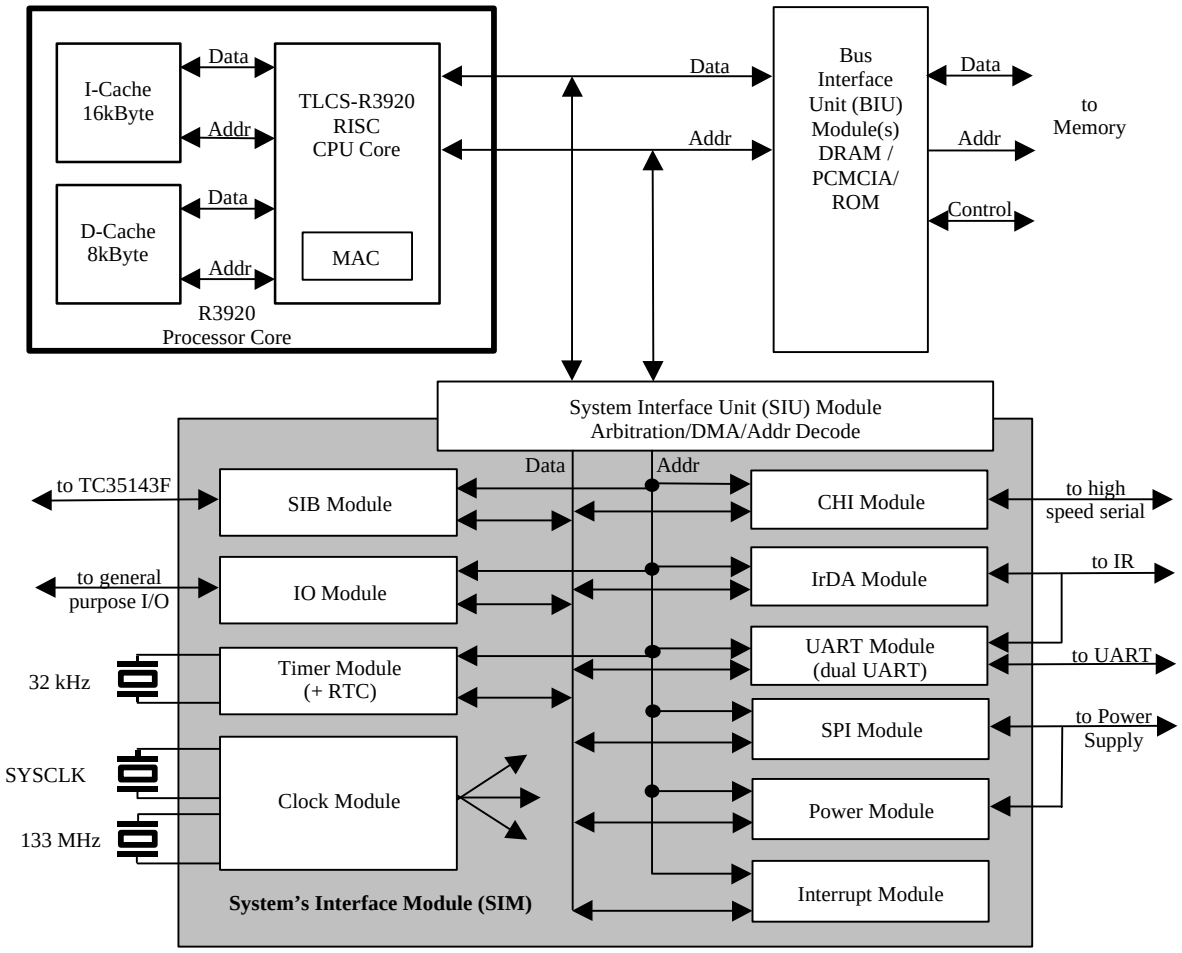

Figure 2. TMPR3922U Internal Block Diagram

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