NEC

VR4310
64-Bit MIPS RISC Microprocessor for Windows CE

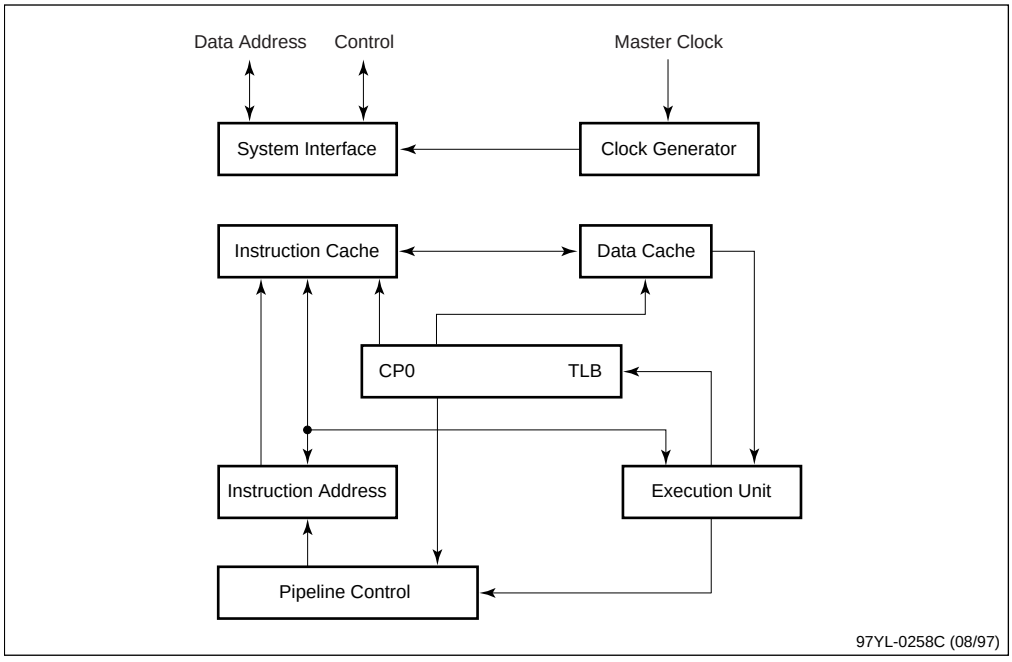
Product Brief

February 1998

Description

The 64-bit VR4310™ (µPD30210) RISC microprocessor is one of NEC's VR Series™ families supporting Windows® CE-based embedded consumer applications. Designed around the popular MIPS® architecture, the VR4310 processor has an internal operating frequency of either 100 MHz, 133 MHz, or 167 MHz at 3.3 volts. Its CPU has an optimized five-stage pipeline, 16K instruction cache, 8K data cache, memory management unit, floating-point arithmetic unit (FPU), and clock generator, and is compatible with MIPS I, II, and III instruction set architectures (ISAs). Based on the advanced 0.28-micron (drawn) process technology, the VR4310 uses 50% of the power that its predecessor, the VR4300™, uses at the same frequency. The VR4310 is also one of the most powerful processors available to support Windows CE, which makes it ideal for many performance-intensive tethered applications.

Block Diagram



Ordering Information

Part Number	Operating Frequency	Package
µPD30210GD-100-MBB	100 MHz	120-pin plastic QFP (28 x 28 mm)
µPD30210GD-133-MBB	133 MHz	
µPD30210GD-167-MBB	167 MHz	

Execution Unit

- 64-bit register file
- 64-bit integer/mantissa data bus
- 12-bit exponent data bus

Coprocessor 0

- Exception processing unit with system control coprocessor registers
- Memory management unit that converts virtual addresses into physical addresses and verifies memory access of kernel, supervisor, and user memory segments
- Seven page sizes: 4K, 16K, 64K, 256K, 1M, 4M, and 16M (VSIZE = 40 and PSIZE = 32)
- Translation lookaside buffer with 32 entries, each mapped to an even or odd frame buffer page

Pipeline Control

- Occurrence of cache misses
- Flash buffer full
- Multicycle instructions
- Occurrence of system exceptions

Floating-Point Arithmetic Unit

- Integrated into CPU's integer arithmetic unit
- Supports both 32-bit (single-precision) and 64-bit (double-precision) IEEE 754 floating-point arithmetic

Instruction Address

- PC incrementer
- Branch address adder
- Conditional branch address selector

16K Instruction Cache

- Direct map
- Virtual index address
- Physical tag cache

No hardware is provided to check generation of a cache alias due to virtual address. Each line consists of 8-word data, a 20-bit tag, and a valid line bit. The cache data interface is 64 bits wide. Cache parity is not supported.

8K Data Cache

- Direct map
- Virtual index address
- Physical tag write-back cache

Each cache line consists of 4-word data, a 20-bit tag and valid line bit, and a write-back bit and its bit parity. Two cache lines correspond to one physical line. Data is read from the cache in one cycle and written to the cache in two cycles. Cache parity is not supported.

System Interface

- Multiplexed 32-bit address/data bus
- Clock signal
- Interrupt request
- Control signal

Clock Generator

Generates four clocks from MasterClock input

- PClock: frequency is set using DivMode(1.0) signals at cold reset
- SClock: system interface clock (internal)
- TClock: output clock reference for external agent; same frequency as MasterClock, except in low-power mode where operating frequency = one-fourth of normal. Low-power mode is set using the status register RP bit; PClock and SClock frequencies are dynamically switched by this means.

The VR4310 uses a phase-locked loop (PLL) to suppress skew between the input clock and internal clock.

High Performance

- 60 SPECint92, 45 SPECfp92, 133 MIPS (100 MHz)
- 80 SPECint92, 60 SPECfp92, 176 MIPS (133 MHz)
- 100 SPECint92, 75 SPECfp92, 221MIPS (187 MHz)

Low Power Consumption

- 0.9 W (typ.) at 100 MHz
- 1.2 W (typ.) at 133 MHz
- 1.5 W (typ.) at 167 MHz

Supply Voltage

- 3.3 volts ±10%

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